

# ***MIL-STD-1553***

## **Cantec**

8 Strathearn Ave., Unit 18  
Brampton, Ontario  
Canada L6T 4L9  
Telephone: (416) 791-5922  
Fax: (416) 791-7940

DAVID GROAL



# **ILC DATA DEVICE CORPORATION**

## ***Designer's Guide***

THIRD EDITION



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# **MIL-STD-1553 DESIGNER'S GUIDE**

THIRD EDITION



**ILC DATA DEVICE  
CORPORATION**

105 Wilbur Place, Bohemia, New York 11716  
(516) 567-5600 • FAX: (516) 567-7358

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# MIL-STD-1553 DESIGNER'S GUIDE

## THIRD EDITION

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The publisher thanks the U.S. Air Force Systems Command for use of "MIL-STD-1553 Multiplex Applications Handbook" in producing this Designer's Guide.

MIL-STD-1553 has become the standard its proponents had hoped it would be. As one of the first companies to provide a line of standard products to serve the needs of this specification, DDC began a program of offering seminars to explain the nuances of 1553 and related similar specifications. As a result of these presentations, and the ensuing question and answer sessions, it became apparent that some sort of broad text that thoroughly explored the spec and its implementation was needed. This Designer's Guide is an attempt to satisfy that need.

In its generation we have drawn from several sources, but primarily from:

1. "MIL-STD-1553 Multiplex Applications Handbook"
2. Our own seminar notes and experiences
3. Our friends and customers

Material from all three sources was used freely with editing to keep the material within budgetary constraints.

The Designer's Guide is aimed at the design engineer confronted with a 1553 interface requirement. It assumes he has read the full spec (MIL-STD-1553B) at least once and so has some limited familiarity with the bus in general but has questions on the details.

Section II was taken straight from the "MIL-STD-1553 Multiplex Applications Handbook". It is included to provide two things: 1) a complete copy of MIL-STD-1553B as a reference, and 2) a section by section commentary on the whys and wherefores of the spec. There is some duplication of material in Sections I and II, but this was considered preferable to constant referencing back and forth. To rewrite either section to accommodate the other would not have been worth the effort. Each section more or less stands alone.

We would like to thank the U.S. Air Force for allowing us to use portions of their Handbook. It is the most complete manual on MIL-STD-1553. We also accept full responsibility for any errors that may have crept in or important material that may have been omitted.

We have tried to refrain from crass commercialism in the main body of the technical discussion. However, a combination of poor taste and an honest desire to dominate the market has resulted in a whole section devoted entirely to our products. It is our hope that, with our broad line of offerings from transformers to complete RTU's, all user needs can and will be met.

We sincerely hope this Designer's Guide will prove useful as a working and a reference source. We have made every effort to insure it is correct, but still hope that you will not hesitate to call our attention to errors, oversights, omissions, or other suggestions that would improve the Designer's Guide.

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P.S. This new second edition has been updated to include additional material on systems integration issues, stores management issue, Notice 1 and Notice 2 to the standard and copies of the SAE-AE-9 RT Validation Test Plan and RT Production Test Plan. We hope this additional material will make the book even more useful to the MIL-STD-1553 community.

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The bus controller's main function is to provide a means for the transfer of data between the bus and the bus controller. The bus controller is the only source of data in the system. The system uses a common bus architecture.

The bus controller consists of a central processing unit (CPU) and a bus controller unit (BCU). The CPU is responsible for the control of the system and the BCU is responsible for the transfer of data between the bus and the CPU. The BCU is also responsible for the transfer of data between the bus and the system. The BCU is also responsible for the transfer of data between the bus and the system.

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## I. DESIGNER'S NOTES

## INTRODUCTION

MIL-STD-1553, Aircraft Internal Time Division Command/Response Multiplex Data Bus, is a military standard (presently in revision B) which has become one of the basic tools being used today by the DoD for integration of weapon systems. The standard describes the method of communication and the electrical interface requirements for subsystems connected to the data bus. The 1 Mbps serial communication bus is used to achieve aircraft avionics (MIL-STD-1553B) and stores management (MIL-STD-1760A) integration. In the future it will be used to extend the systems integration to flight controls, propulsion controls, and vehicle management system (electrical, hydraulic, environmental control, etc.).

Several other documents exist which are related to MIL-STD-1553. MIL-HDBK-1553 describes the implementation practices for this standard including: design considerations, examples of applications, and guidelines for implementations. Portions of MIL-STD-1553 are also the foundation of the proposed DOD-STD-1773 (Fiber-optics), and MIL-STD-1760A (Stores Management). In addition, MIL-STD-1553 is embodied in or referenced by the following international documents: NATO STANAG 3838, ASCC Air Standard 50/2, and UK DEF STAN 00-18 (Part 2)/Issue 1.

This Designer's Guide will provide; 1) a synopsis of the standard and some frequently asked questions and their answers, 2) a specification comparison of the detailed uses of the standard, 3) a review of system design considerations, and 4) a discussion of remote terminal and bus controller designs.

### 1.0 MIL-STD-1553 OVERVIEW

The 1553 standard is organized similar to most military standards with a foreword, scope, referenced document section, definitions, general requirements, the appendix, and a tri-service Notice 2. Notice 2, which supersedes Notice 1, was developed to define which options of the standard are required to enhance tri-service interoperability and to further define some of the open-ended timing variables implied within the standard.

#### 1.1 Key Elements

Some of the key MIL-STD-1553B elements are the bus controller, the embedded remote terminal (a sensor or subsystem that provides its own internal 1553 interface), the stand-alone remote terminal, bus monitor, and two other devices that are part of

the 1553 integration; the twisted shielded pair wire data bus and the isolation couplers that are optional.

**The bus controller's main function is to provide data flow control for all transmissions on the bus.** In this role, the bus controller is the sole source of communication. The system uses a command/response method.

The embedded remote terminal consists of interface circuitry located inside a sensor or subsystem directly connected to the data bus. Its primary job is to perform the transfer of data in and out of the subsystem as controlled by the bus controller. This type of terminal usually does not have bus controller capability. However, if the sensor itself is fairly intelligent, it can become a candidate for the backup bus controller function. Generally, **an intelligent subsystem (i.e., computer based) can become a backup bus controller if a second computer, equal in function to the primary, is unavailable.**

The stand-alone remote terminal is the only device solely dedicated to the multiplex system. It is used to interface various subsystem(s) which are not 1553 compatible with the 1553 data bus system. Its primary function is to interface and monitor transmission in and out of these non-1553 subsystem(s).

The bus monitor listens to all messages, and subsequently collects data from the data bus. Primary applications of this mode of operation include: collection of data for on board bulk storage or remote telemetry; or use within a "hot" or off-line back-up controller to observe the state and operational mode of the system and subsystems.

The fourth item is the data bus itself. The standard defines specific characteristics for the twisted pair shielded cable. Notice 2 tightens these requirements and adds a definition for connector polarity.

The last item to be discussed is the data bus coupler unit that isolates the main bus from the terminals. MIL-STD-1553B allows two types of data bus interface techniques; direct coupling and transformer coupling. Subsystems and 1553 bus elements are interfaced to the main data bus by interconnection buses (called "stubs"). These stubs are either connected directly to the main bus or interfaced via data bus couplers. The data bus couplers contain two isolation resistors (one per wire) and an isolation transformer (with a ratio of 1 to the square root of 2). The purpose of the data bus

couplers is to prevent a short on a single stub from shorting the main data bus. The selection of the value of the resistors, the transformer's turn ratio, and the receiver impedance are such that the stub appears to the main bus as a "clean interface" (i.e. high impedance). This technique reduces the distortion caused on the main data bus by the termination. The characteristics of the data bus couplers are discussed in paragraph 4.2.4. Main buses utilizing direct coupled stubs must be designed to withstand the impedance mismatch of the stubs. This can be reduced by minimizing stub length (less than one foot) and "tuning" the bus by terminal spacing. **Designs not using data bus couplers should be carefully analyzed and tested to determine if waveform distortion is significant enough to cause receiver problems.** The other risk associated with direct coupled stubs is a short on a stub will cause the main bus to fail. The obvious advantage to direct coupled stubs is the elimination of the logistical problems associated with another device and the installation problem of locating these small devices (approximately 1 inch cube) in the aircraft. Today, data bus couplers and line terminating resistors are available in molded packages which can become part of the wiring harness, thus eliminating some of the installation problems. Also, multiple data bus couplers and data bus line terminating resistors are available in single packages, which reduces the number of unique units installed per aircraft.

## 1.2 Message Types

MIL-STD-1553 is a serial data bus based on message transmission. Therefore, considerable emphasis placed on the term "information transfer formats," which describe each of the 10 message types. Within these 10 message types are the formats used to achieve communication, the primary function of the data bus system. **Each message format is made up of control words called command and status. Data words are used to encode communication between system elements.** Both control words and data words are used in system communication as well as data bus system control. These message formats have been subdivided into two groups by 1553B and are shown in figure I-1.1; the "information transfer formats" and the "broadcast information transfer formats." These two groups can be easily segregated because the broadcast group does not conform directly to the common/response philosophy of the other (non-broadcast) message formats. **(This command/response philosophy requires that all error free messages received by a remote terminal be followed by the transmission of a remote terminal status word.** This handshaking process validates error free message completion. Since broadcast message formats are transmitted to multiple receivers, a more detailed scheme is required to validate error free message reception (this method is described in paragraph 1.4.2). Also, since address 31 is

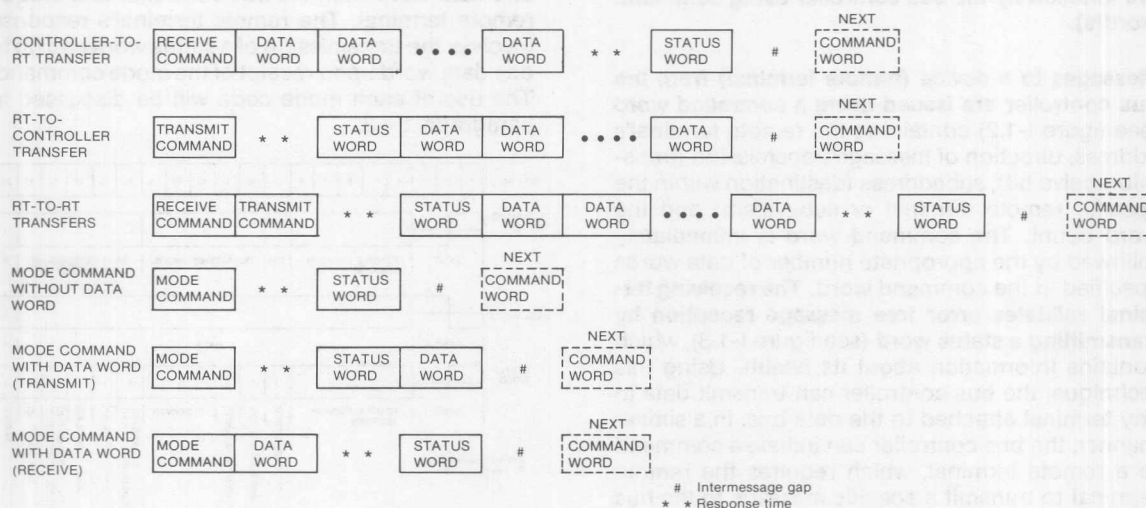


Figure I-1.1 Information Transfer Formats

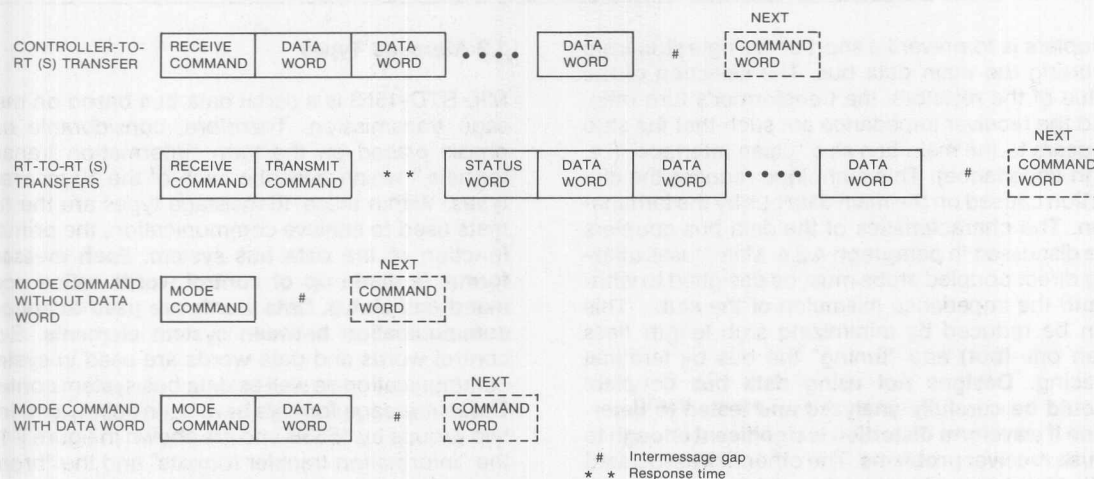


Figure I-1.1 (con't.) Broadcast Information Transfer Formats

used by all terminals receiving a broadcast message, subaddressing needs to be managed on a data bus system basis rather than on a remote terminal basis. The ability to define and use more than 30 subaddresses is discussed in paragraph 3.7.1.

The information transfer formats allow communications between two elements in the data bus system; the bus controller and the remote terminal (RT). In 1553, the bus controller is in control of all communication and it is the sole device allowed to transmit command words. **Notice that all messages are initiated by the bus controller using command word(s).**

**Messages to a device (remote terminal) from the bus controller are issued using a command word** (see figure I-1.2) containing the remote terminal's address, direction of message transmission (transmit/receive bit), subaddress (destination within the specific remote terminal or subsystem), and the word count. The command word is immediately followed by the appropriate number of data words specified in the command word. **The receiving terminal validates error free message reception by transmitting a status word** (see figure I-1.3), which contains information about its health. Using this technique, the bus controller can transmit data to any terminal attached to the data bus. In a similar manner, the bus controller can initiate a command to a remote terminal, which requires the remote terminal to transmit a specific message to the bus controller. This is accomplished using the RT to bus controller message format. Similarly, com-

munication can be established between two unique remote terminals, when the bus controller commands one terminal to receive data and the other terminal to transmit data. Neither the receiving nor the transmitting terminal knows where the message originated or destined. Both will transmit status words in the proper formats. Each status word is evaluated by the bus controller to verify error free message completion. In addition to these three message formats, three control message formats are provided to support data bus system management. These formats are mode code formats allowing the transmission of a command word and up to one data word from the bus controller to a unique remote terminal. The remote terminal's response involves the transmission of a status word and up to one data word upon receipt of the mode command. The use of each mode code will be discussed in paragraph 1.4.2.

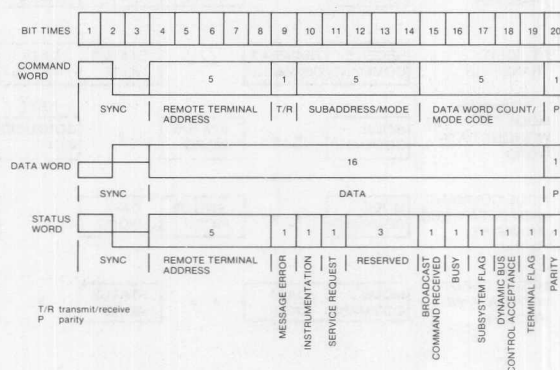


Figure I-1.2 Word Formats



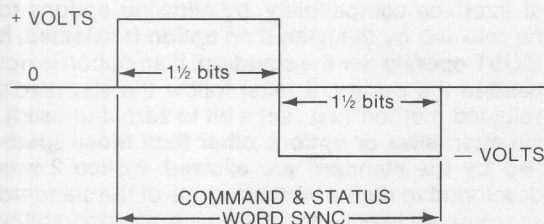


Figure I-1.3 Command and Status Word Sync

Broadcast formats are identical to the non-broadcast formats discussed above, except the bus controller transmits commands using a remote terminal address of "31" (11111), which has been reserved for this function. All remote terminals with the broadcast reception capability will receive this command, validate error free message reception, and establish a status word response, but the transmission of the status word will be suppressed. Obviously, if multiple terminals simultaneously transmitted their status responses a bus "crash" (undetectable message transmissions) would occur. As can be seen by the RT to RT(s) transfer formats (see figure I-1.1), the bus controller can set up a broadcast data reception for all terminals and then command a single terminal (unique address) to transmit. Since the data bus system is required to follow the last valid command, the unique terminal will transmit its status word (which will be ignored by the other terminals) followed by the specified number of data words. **This format allows a subsystem to broadcast its data directly to multiple users.** Broadcast messages can be validated using a transmit status or transmit last command mode code (see paragraph 1.4). Therefore, even broadcast message formats have a command/response approach to message validation, if required by the system design. Notice 2 of the standard allows for the transmission by the bus controller of broadcast mode codes only (whereas Notice 1 forbids all broadcast messages). This will ease the bus controller's overhead in performing such tasks as minor/major frame synchronization.

### 1.3 Word Types

The standard allows for only three types of words as discussed in the previous message format section; command word, status word, and data word. 1553 requires each word to consist of 16 bits of data plus, a sync pattern (3 bit times long), and a one bit parity providing a 20 bit word format. The contents of each word type is shown in figure I-1.2.

**The command word provides the definition of the message format to be transmitted and can only be transmitted by the bus controller.** As seen in the message format section, the command word may be followed by data, another command word, or a response time gap prior to status word transmission by the remote terminal. The command word sync pattern is a unique invalid Manchester waveform which cannot be duplicated by data (see figure I-1.3). The command word sync and the status word sync are identical and the inverse of the data word sync pattern. Therefore, command and status words, which initiate a sequence, can always be distinguished from data word sync patterns.

**The command word address is always the address of the remote terminal being commanded; a bus controller does not have an address while in the active bus controller mode** (backup bus controllers can function as an RT with a unique address or as a bus monitor with no address until they become an active bus controller). The transmit/receive (T/R) bit indicates the direction of flow of data words (i.e., receive means data to be received by the remote terminal). The subaddress-/mode code field has two purposes. When a unique terminal is to receive or transmit data, the subaddress acts as an internal address to point to the type of data desired, the location of a data pointer in memory, subsystem interface, etc. (see paragraphs 3.7.1 and 5.3 for further discussion on subaddressing).

When the subaddress field is 00000 or 11111, it indicates that the next field contains the number of the mode code. The next field (word count/mode number) contains the number of data word(s) in the message or the number of the mode code. Odd parity is established for all words based on the 16 bits of data plus parity bit.

**The data word contains a unique sync (three bit times long), 16 data bits, and a one bit parity. No restrictions are placed on the encoding of the data field, except that the "most significant bit shall be transmitted first."** Once again, parity is odd and established on the 16 bits of data plus the parity bit.

Recently, there have been several efforts to standardize on data word formats for the more commonly used functions. The Army and Navy have recently developed data bases for some avionics equipment. The designer should check the status of these efforts before establishing a unique set of data formats for the system. Section 80 (formerly Chapter 11) of the "MIL-HDBK-1553 Multiplex

sage formats for data bus applications. (See paragraph 3.9 for further discussion on system documentation and Interface Control Documents.)

The status word utilizes the same sync format as the command word. The remote terminal address is placed in the transmitted status word for two reasons; so that the status word can be validated by the bus controller (a remote terminal may also validate the status word address field against that of the command word's during an RT-RT message transfer), and so that the status word will not be misinterpreted by the other terminals as a command word. Any status word transmitted, must contain valid information at all times (i.e. following RT power-up, during initialization, and during normal operation). The message error bit is the only required status bit and it is used to identify messages which do not pass the word or message validation tests of 1553 (1553B paragraph 4.4.1.1 and 4.4.1.2). MIL-STD-1553 requires this bit to be set if a message fails to pass the tests and the status word to be suppressed (NOT to be transmitted). This means that **all messages that are NOT error free will NOT have a responding status word.** This allows the bus controller to time-out on the no status response, thus alerting the bus controller of a failure condition. **To obtain the status word with the error bit set requires a transmit status mode code or transmit last command word mode code to the terminal to retrieve the untransmitted status word (see paragraph 1.4.2).** The only exception is the illegal command option (see paragraph 1.6.3). The instrumentation, service request, broadcast command received, busy, subsystem flag, dynamic bus controller acceptance, and terminal flag bits are all optional and are discussed in paragraph 1.4.1. Notice 2 tightens the requirements for remote terminals employing broadcast recognition, capability of dynamic bus control, RT built-in-test, or subsystem built-in-test, by requiring the use of the bits in the status word associated with these functions. Bit positions 12 through 14 are reserved for future use and must be transmitted as zeros. To obtain usage of these bits requires DoD approval (no approval has been given as of 7/87). The last bit of the status word is the odd parity bit, which is calculated in a similar manner to all other parity bits.

#### 1.4 Options Within the Standard

Since the standard covers a wide variety of designs, flexibility has been achieved without loss

**MUST operate per the standard.** If an option is not used in the design, it must follow the standard's selected method (e.g., set a bit to zero if unused). **No alternative or options other than those specified by the standard are allowed.** Notice 2 was developed to define which options of the standard are required to enhance tri-service interoperability and to further define some of the open-ended timing variables implied within the standard. As stated previously, options are available in the following areas; status word bits, mode codes, data bus redundancy, and coupling techniques.

##### 1.4.1 Status bits

The optional status bits are; instrumentation, service request, broadcast command received, busy, subsystem flag, dynamic bus control acceptance and terminal flag.

**The instrumentation bit in the status field is set to distinguish the status word from the command word.** Since the sync field is used to distinguish the command and status words from a data word, a mechanism to distinguish command and status word is provided by the instrumentation bit. By setting this bit to logic zero in the status word for all conditions and setting the same bit position in the command word to a logic one, the command and status words are identifiable. If used, this approach reduces the possible subaddresses in the command word to 15 and requires subaddress 31 (11111) to be used to identify mode commands (both 11111 and 00000 are allowed). If the instrumentation bit is not used, the bit will remain set to logic zero in the status word for all conditions.

**The service request bit is provided to indicate to the active bus controller that the remote terminal is requesting service.** When this bit in the status word is set to logic one, the active bus controller may take a predetermined action (if only one action can occur) or use the transmit vector word mode command to identify the specified request. The message format for acquiring this is discussed under transmit vector word mode command below.

**For terminals implementing the broadcast option, the broadcast command received bit is set to logic one when the proceeding valid command word was a broadcast command (remote terminals address 31).** Since the broadcast message formats require the receiving remote terminals to suppress their status responses, the broadcast command

receive bit is set to identify that the message was received error free. To allow the bus controller to examine the status word requires the use of the transmit status word mode code or the transmit last command word mode code. The broadcast command received bit will be reset, when the next valid command occurs if it is NOT one of two mode codes; transmit status word or transmit last command word. Therefore, **to analyze the status word after a broadcast message has occurred requires a mode code message to a unique terminal.** The mode code message must be transmitted before any other message transmission to that unique terminal in order to retrieve to proper status word.

**The busy bit in the status word is set to logic one to indicate to the active bus controller that the remote terminal is unable to move data to or from the subsystem in compliance with the bus controller's command.** A busy condition can exist within a remote terminal at any time causing it to be non-responsive to a command to send data or to receive data. This condition can exist for all message formats. In each case, except the broadcast message formats, the active bus controller will determine the busy condition immediately upon status response. In the case of the broadcast message formats, this information will not be known unless the receiving terminals are analyzed using transmit status mode code after the broadcast message. If the status word has the broadcast received bit set, the message was received and the terminal was not busy. Notice 2 to the standard discourages the use and existence of busy condition, as they affect the overall communications flow on the bus, add overhead to the bus controller, and may have adverse effects upon data latency requirements within time critical systems (i.e. flight controls). A busy condition must only occur as the results of a particular command or message received by the terminal and NOT due to an internal periodic function. Thus for a non-failed terminal, the bus controller, with prior knowledge of the RT's characteristics, can determine what actions (commands/messages) will cause an RT to become busy, thus preventing any unnecessary busy conditions.

**The subsystem flag bit is provided to indicate to the active bus controller that a subsystem fault condition exists and that data being requested from the subsystem may be invalid.** The subsystem flag may be set in any transmitted status word. If more than one subsystem is interfaced to the remote terminal the subsystem flag is the ORED results of all subsystems. The only method availa-

ble in 1553B to determine subsystem(s) health is via a normal message. The use of the subsystem flag bit requires considerable system control philosophy. If upon receiving the bit set, the bus controller is to do anything other than stop all communication with the terminal, a detailed protocol is required.

The system protocol must define the message (NOT a mode code) that the bus controller uses to poll the subsystem to determine the reason the bit was set. This polling will provide system application software the knowledge to determine the availability and status of the unit(s). If the unit(s) are usable, the subsystem flag bit must be cleared so that troubleshooting analysis does not occur, until another failure occurs. This can be accomplished using additional messages or upon transmission of the first message. This process usually requires several transmissions during which time the remote terminal is NOT a part of the normal periodic data bus traffic. Obviously, user subsystems must deal with this temporary or permanent loss of this data. **Mode commands can not be used to acquire subsystem built-in-test results.**

**The next bit in the status word is provided to indicate the acceptance of the bus controller's offer to become the next bus controller.** The offer of bus control occurs when the presently active bus controller has completed its established message list and issues a dynamic bus control mode command to the remote terminal that is to be the next potential controller. To accept the offer the potential bus controller sets its dynamic bus control acceptance bit in the status word and transmits the status word. The establishment of who the next potential controller should be is discussed in the system design section (see paragraph 3.2). For Air Force applications, Notice 2 prohibits the bus controller from issuing a dynamic bus mode code, therefore this bit would always be set to zero.

**The terminal flag bit is set to a logic one to indicate a fault within the remote terminal.** This bit is used in conjunction with the three mode code commands; inhibit T/F flag, override inhibit T/F flag, and transmit BIT word. The first two mode code commands deactivate and activate the functional operation of the bit. The transmit BIT word mode code command is used to acquire more detailed information about the terminal's failure. Most MIL-STD-1553B RT chip sets provide BIT word responses indicating the health of the chip. Notice 2 requires implementation of this bit within the status word if the remote terminal is capable of any



form of self test (including what may be performed internal to the various chip sets such as data wrap-around and data comparisons).

#### 1.4.2 Mode Codes

The basic philosophy of the information transfer system is that it operates as a transparent communication link. "Transparent" means that an application's function does not need to be involved with the management of communication. Obviously, the information transfer system requires management that introduces overhead in the data bus system. The command words, status words, status word response gaps, and intermessage gaps are the overhead. Within the command word the **mode codes provide data bus management capability**. The mode codes (see table I-1.1) have been divided into two groups; mode codes without

a data word (00000-01111) and mode codes with a data word (10000-11111). The use of bit 15 in the command word to identify the two types was provided to aid in the decoding process. Also, the use of a single data word instead of multiple data words was adopted to simplify the mode circuitry.

**Generally, with these two types of mode commands, all data bus system management requirements can be met.** Additional overhead is required by the system to maintain RT health, system time control (synchronization), subaddress message mapping, aperiodic message control, initialization/shutdown messages, etc. The determination of whether the command word contains a mode code is accomplished by decoding the subaddress-/mode field (bit times 10-14). This field being either all zero's [00000] or all one's [11111] indicates that the command is a mode code and that the word count/mode code field (bit times 15-19) contain

Table I-1.1 Assigned Mode Codes

Transmit-receive bit	Mode code	Function	Associated data word	Broadcast command allowed
1	00000	Dynamic bus control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit status word	No	No
1	00011	Initiate self-test	No	Yes
1	00100	Transmitter shutdown	No	Yes
1	00101	Override transmitter shutdown	No	Yes
1	00110	Inhibit terminal flag bit	No	Yes
1	00111	Override inhibit terminal flag bit	No	Yes
1	01000	Reset remote terminal	No	Yes
1	01001	Reserved	No	TBD
1	01111	Reserved	No	TBD
1	10000	Transmit vector word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit last command	Yes	No
1	10011	Transmit bit word	Yes	No
0	10100	Selected transmitter shutdown	Yes	Yes
0	10101	Override selected transmitter shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
1 or 0	11111	Reserved	Yes	TBD

Note: TBD — to be determined.



the mode code type. Notice 2 requires that terminals must decode both indicators and that they must not convey different information. (Some earlier designs had used the [00000] indicator for the terminal hardware and the [11111] indicator for subsystem hardware).

Notice 2 also permits the broadcasting of mode codes. While this can reduce bus controller overhead in the areas of frame synchronization, it can have adverse effects upon the system if inadvertently issued (e.g. broadcast of a reset mode code). The system's designer is cautioned to research the implications of the use of the broadcast mode code commands before implementation.

There is no particular reason for the numerical assignment of the mode codes, except for dynamic bus control [00000], which was previously defined in 1553A. The separation of mode commands into two categories (with and without data words) is important to allow for controlled expansion of the standard. By controlling the mode code command number and its definition, commonality between various terminals can be maintained. **All undefined [unused] mode codes are considered illegal commands** (see paragraph 1.6.3 for discussion of illegal command protocol). Notice 2 requires that all remote terminals must implement the following mode codes as a minimum: a) transmit status word, b) transmitter shutdown, c) override transmitter shutdown, and d) reset remote terminal. The bus controller must have the capability of implementing all mode code commands. The message formats associated with mode commands are shown in figure I-1.1.

**The dynamic bus control mode code [00000]** is provided to allow the active bus controller a mechanism (using the information transfer system message formats) to offer a potential bus controller (operating as a remote terminal) control of the data bus. Only the single receiver command (unique address) is allowed to be issued by the active bus controller. The response to this offering of the bus controller is provided by the receiving remote terminal, using the dynamic bus control acceptance bit in the status word. Rejection of this request by the remote terminal requires that the presently active bus controller must continue offering control to other potential controllers, the same controller, or remain in control. When a remote terminal accepts control of the data bus system by setting the dynamic bus control acceptance bit in the status word, control is relinquished by the presently active bus controller and the

potential bus controller can then begin bus control. Note that Notice 2 prohibits the bus controller from ever issuing this mode command for Air Force applications.

Two mode codes are used to **synchronize** the data bus system; synchronize without a data word and synchronize with a data word. Synchronization informs the terminal(s) of an event time, to allow coordination between the active bus controller and terminals. Synchronization information may be implicit in the command word [mode code 00001] or in the data word [mode code 10001] following the command word. If a data word is used, the definition of the bits are the responsibility of the system designer and may contain system information such as timing data, data mapping pointers, etc. Paragraph 3.6 provides a system discussion of the use of the synchronize with data word mode code for remote terminal synchronization and subaddress mapping within a remote terminal for both periodic, aperiodic, and time critical messages.

The **status word** associated with the transmit status word mode code [00010] is identical in format to the status word transmitted with every error free message. However, this is one of two mode codes, which do not change the state of the status word. Therefore, the status word returned with this mode code represents the status word of the previous message NOT the status of the mode code message. Paragraph 5.2 provides a discussion on the affects of back to back transmission of this mode code. This mode code gives the bus controller the ability to analyze problems associated with the previous message. Using this approach, a bus controller can organize the communication with a terminal to obtain error analysis data.

**The initiate self-test mode command [00011]** is provided to initiate built-in-test (BIT) circuitry within a remote terminal. The mode code is usually followed, after sufficient time for test completion, by a **transmit BIT word mode command [10011]** yielding the results of the test. Notice 2 specifies that the RT receiving this mode code must complete its test and have the results ready within 100 milliseconds. The purpose of establishing an upper limit to the amount of time required to perform a reset is that the bus controller, with this prior knowledge, is aware of the maximum amount of time that the controller will be "off-line" or busy, and may cease further communications with this terminal until such time has elapsed. This prevents the bus controller's software from continuously

message formats provided for the initiate self-test mode command allow for both individual requests and multiple requests (broadcast). Notice that **the initiate self-test mode command is associated with the 1553 multiplex hardware only** and NOT with the interfacing subsystem. Paragraph 5.2 discusses the problem of separating subsystem self test and health status messages from RT tests in terminals with embedded RTs.

**The transmit BIT word mode command [10011] provides the BIT results available from a terminal,** as well as the status word. Typical BIT word information for both embedded and stand-alone remote terminals include encoder-decoder failures, analog transmitter/receiver failures, terminal control circuitry failures, power failure, subsystem interface failures, and protocol errors (e.g., parity, Manchester, word count, status word errors, and status word exceptions). The internal contents of the BIT data word are provided to supplement the appropriate bits already available via the status word. Notice that the transmit BIT word within the remote terminal **" . . . shall not be altered by the reception of a transmit last command or transmit status word mode code"** received by the terminal. This allows error handling and recovery procedures to be used without changing the error data recorded in this word. **However, the RT will only save the last command and the status code field [of the status word] if the mode code transmit last command or transmit status word are transmitted.** Broadcasting of this command by the bus controller is not allowed. Another point which needs to be mentioned again is that **the function of transmitting RT BIT data " . . . shall not be used to convey BIT data from the associated subsystem[s]."** See discussion on subsystem flag bit in paragraph 1.4.1.

Four mode code commands are provided to control the transmitters associated with terminals in a system. These commands can be sent to a single receiver or broadcasted to multiple users. **The transmitter shutdown mode code [00100]** is used in a dual-redundant bus structure, where the command causes the transmitter associated with the other bus to terminate transmissions. No data word is required for this mode command. **The override transmitter shutdown mode code [00101]** is used in a dual-redundant bus structure where a previously disabled transmitter is enabled. No data word is provided for this mode code. **The selected transmitter shutdown mode code [10100]** is used in a multiple (greater than two) redundant bus

transmitter to terminate transmissions on its bus. A data word is used to identify the selected data bus. **The override selected transmitter shutdown mode code [10101]** is used in a multiple (greater than two) redundant bus structure where the command allows the selected transmitter to transmit on its bus when commanded. The format of the data word associated with these two mode commands is NOT controlled by the standard and must be defined by the systems designer. Another method of overriding the transmitter shutdown mode codes [00100 and 10100] is to issue a reset mode code to the terminal.

**Note that the standard or Notice 2 does not imply that issuance of either the transmitter shutdown or the selected transmitter shutdown mode codes will cause the associated receiver to also be shutdown. If the receiver does not "shutdown", then the system's designer should be aware that the terminal may still be receiving and processing data (on the shutdown bus). Therefore, the bus controller should remove the terminal from the active periodic communications list.**

The inhibit terminal flag mode code [00110] **is used to set the terminal flag bit to zero in the status word.** When issued, the status word indicates an UNFAILED condition regardless of the actual failure state of the terminal. **This mode code is primarily used to prevent continued interrupts and error handling analysis when the failure has been noted and the system reconfigured as required. Commanding this mode code prevents further failures from being reported, which normally would be reported using the terminal flag in each subsequent status word response. The message format associated with this mode code allows for both single and multiple receivers to be commanded. No data word is required with this mode code.** Note that the terminal flag, which is used to indicate an RT fault condition is limited to the remote terminal NOT any subsystem faults. (See the previous discussion on initiate self test and transmit BIT word mode codes.)

The override inhibit terminal flag mode command [00110] **negates the inhibit function thus allowing the T/F flag bit in the status response to report the present condition of the terminal. This mode code can be transmitted by the active bus controller to both single and multiple receivers. There is no data word associated with this mode code.** This mode code could be used to analyze all the faults that exist in a remote terminal, since the inhibit terminal

may need code with which to communicate since its implementation.

**The reset remote terminal mode code [01000]** causes the addressed terminal(s) to reset themselves to a power-on initialized state. This mode code may be transmitted to an individual remote terminal or to multiple remote terminals (broadcast). Notice 2 requires that all terminals receiving this command shall complete their reset function within 5 milliseconds following the transmission of their status word (non-broadcast message). This mode code provides a means to "start-over" at a known point. It may be the last thing the error handling software tries before giving up on a terminal.

**The transmit vector word mode code [10000]** is associated with the service request bit in the status word and is used to determine specific service being required by the terminal. The service request bit and the transmit vector word mode command provide the only means available for the terminal to request the scheduling of an asynchronous message, if more than one service request exists per terminal. If a remote terminal contains only a single service request, the bus controller may be "smart enough" to perform the request without the transmit vector mode code data word to point to the location of the commands within the bus controller to perform the service. The message format for this single receiver operation contains a data word associated with the terminal's response. Figure I-1.4 illustrates the message formats associated with this mode command. **Since a service request is handled at the convenience of the bus controller and NOT the remote terminal's, a remote terminal design feature is required to queue multiple service requests until they can be serviced by the bus controller.** The transmission of the transmit vector word mode code by the bus controller does not necessarily release the remote terminal to set the service request bit for a new request. There are several methods that can be used to resolve this handshake problem. Whatever the solution chosen by the systems designer, it should be applied to all terminals in the system. Thus, it's a system design issue which should be addressed in the multiplex system specification. Solutions that are acceptable to most designers are; after transmission of the transmit vector word code allow new service request codes, and use of the synchronize without data word mode code command to release the RT to set a new service request. However, the first method has the potential of losing a critical request if the transmit vector word is

counter this problem, previous designs have used the second method to release the service request queue. The transmission of the synchronize without data word mode code after proper receipt of the transmit vector mode code frees the terminal's service request bit at the expense of an extra transmission.

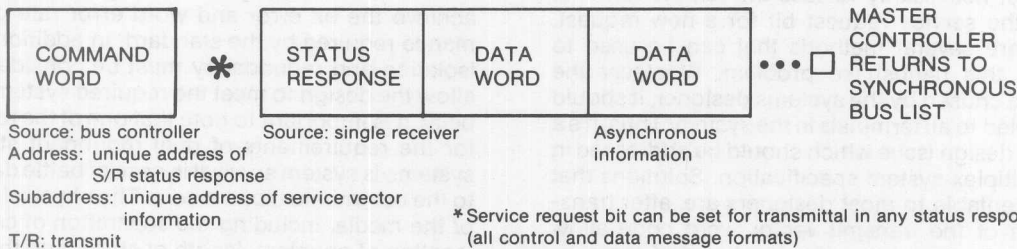
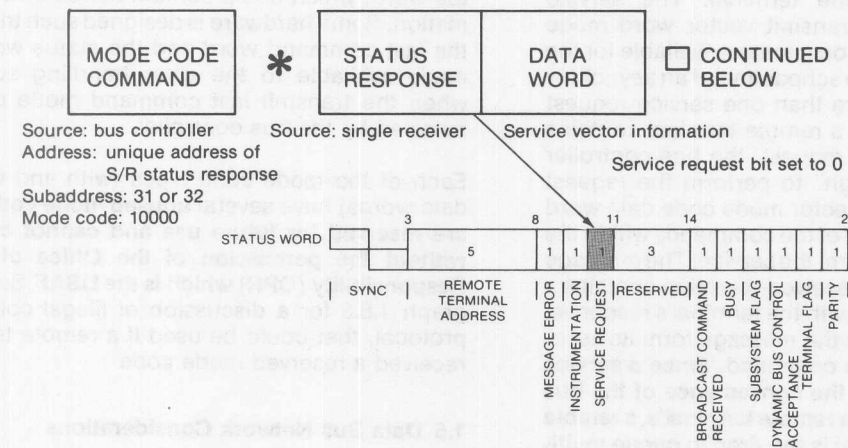
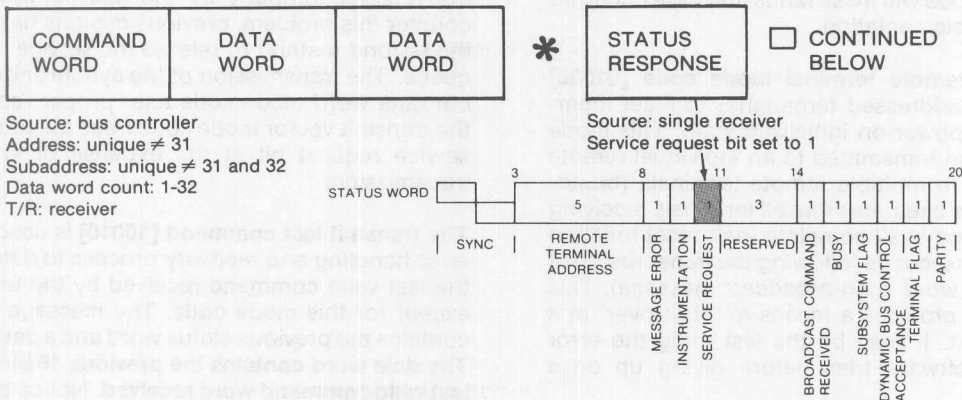
**The transmit last command [10010]** is used in the error handling and recovery process to determine the last valid command received by the terminal, except for this mode code. The message format contains the previous status word and a data word. **The data word contains the previous 16 bits of the last valid command word received.** Notice that this mode command will not alter the state of the receiving terminal's status word. This fact allows this mode command to be used in error handling and recovery operations without affecting the status word, which could contain added error information. Some hardware is designed such that both the last command word and the status word are made available to the error handling software when the transmit last command mode code is received by the bus controller.

Each of the mode code types (with and without data words) have several **unused mode codes that are reserved for future use and cannot be used without the permission of the Office of Prime Responsibility (OPR) which is the USAF.** See paragraph 1.6.3 for a discussion of illegal command protocol, that could be used if a remote terminal received a reserved mode code.

## 1.5 Data Bus Network Considerations

One of the most significant considerations facing the data bus system designer and integrator is the definition of the data bus network. The bus network must be designed for signal integrity to achieve the bit error and word error rate performance required by the standard. In addition, fault isolation and redundancy must be considered to allow the design to meet the required system reliability. It is important to note that one of the reasons for the requirements of dual redundant standby systems is system survival in case of battle damage to the communications media. The physical layout of the media, including the separation of cabling, location of couplers, length of stubs, and the connection of the media to the terminals are of importance not only from a maintainability point of view, but also regarding system operation, survivability, fault isolation, and systems security. The following

Single Receiver Only — Bus Controller to Remote Terminal\*



\* Service request bit can be set for transmittal in any status response (all control and data message formats)

\* Response time delay or gap  
☐ End of message delay or gap

Figure I-1.4 Transmit Vector Word Transfer Format



discussion provides a summary of MIL-STD-1553B requirements that have significant effects on the design.

### 1.5.1 MIL-STD-1553B Bus Network Requirements

Table I-1.2 is a summary listing of the data bus

coupling requirements contained in 1553B. The characteristics of the twisted-shielded pair cable have been relaxed from 1553A to allow selection of cable types from a variety of manufacturers. It has been shown that minor variations from the specified cable characteristics do not significantly affect the system performance. Today it is possible

Table I-1.2 Summary of Data Bus and Coupling Requirements

Parameter	MIL-STD-1553B
Transmission line	
Cable type	Twisted-shielded pair
Capacitance (wire to wire)	30 pF/ft, maximum
Twist	Four per foot (0.33/in), minimum
Characteristic impedance ( $Z_0$ )	70 to 85 ohms at 1.0 MHz
Attenuation	1.5 dB/100 ft at 1.0 MHz, maximum
Length of main bus	Not specified
Termination	Two ends terminated in resistors equal to $Z_0 \pm 2\%$
Shielding	75% coverage minimum
Cable coupling	
Stub definition	Short stub < 1 ft Long stub > 1 to 20 feet (may be exceeded)
Coupler requirement	Direct coupled — short stub; transformer coupled — long stub (ref. fig. I-1.7)
Coupler transformer	
Turns ratio	1:1.41
Input impedance	3,000 ohms, minimum (75 kHz to 1.0 MHz)
Droop	20% maximum (250 kHz)
Overshoot and ringing	$\pm 1.0V$ peak (250-kHz square wave with 100-ns maximum rise and fall time)
Common mode rejection	45.0 dB at 1.0 MHz
Fault protection	Resistor in series with each connection equal to $(0.75 Z_0) \pm 2.0\%$ ohms
Stub voltage	1.0V to 14.0V p-p, I-I, minimum signal voltage (transformer coupled); 1.4V to 20.0V, p-p, I-I, minimum signal voltage (direct coupled)



to obtain high quality cabling from various manufacturers which meet all the requirements of the standard. Notice 2 tightens the shielding requirements to 90.0 percent coverage for the cable and 360 degree shielding with 75.0 percent coverage for connector junctions, cable terminations, and bus-stub junctions.

A great deal of concern is attributed to the cable network requirements including; bus length, coupling and stubbing. MIL-STD-1553B does not specify a maximum main bus length, because the cable length, number of terminals and length of stubs are all subject to trade-offs and must be considered in the design for reliable system operation. To help understand these problems a generalized multiplex bus network configuration is shown in figure I-1.5. The main bus is terminated at each end of the cable with the characteristic impedance to minimize reflections caused by transmission line mismatch. With no stubs attached, the main bus looks like an infinite length transmission line with no disturbing reflections. When the stubs are added to connect terminals the bus is loaded locally and a mismatch occurs which can result in reflections. The degree of mismatch and resulting signal distortion is a function of the absolute impedance  $[Z]$  presented by the stub and terminal impedance. **To minimize signal distortion it is desirable to maintain a high stub reflected impedance into the main bus.** At the same time the impedance needs to be low so that adequate signal power will be delivered to the receiver. A trade-off and compromise between these conflicting requirements is necessary to achieve the specified signal-to-noise ratio and system error rate performance. In addition to these trade-offs, careful consideration must be made in the determination of the type of connector used to connect the terminal to the bus. This consideration should include the required integrity, isolation, and shielding (Notice

2 requires 300 degrees of shielding with a minimum of 75% coverage from the cable to the connector). Other issues which need to be addressed include the location and type of connector (concentric, twinax, etc.), and if the data bus connectors will be stand-alone or included with other signals in a multi-contact connector. As a minimum, the two buses (A and B) should be brought into the terminal via separate connectors for isolation purposes.

**Two methods for coupling a terminal to the main bus are defined in 1553B, transformer coupling and direct coupling** (see figure I-1.6). Transformer coupling is usually used with long stubs (1 to 20 ft.) and requires a coupler box or in-line molded coupler, separate from the terminal, located at the junction of the main bus and stub. Direct coupling is usually limited to stubs of less than 1 ft. In transformer isolated stubs, fault isolation resistors are included to provide protection for the main bus in case of a short circuit in the stub or terminal. The transformer characteristics defined in 1553B and listed in table I-1.2 provides a compromise for the signal level and distortion characteristics delivered to the terminals. The transformer turns ratio (1:1.41) provides beneficial impedance transformations for both terminal reception and transmission. **Notice 2 states that for Navy applications, terminals shall have both transformers and direct coupled stubs available, whereas for Army and Air Force applications, only transformer coupled stubs are required.**

### 1.5.2 Data Bus Network Analysis

A plot of the calculated first-order-magnitude stub absolute impedance  $[Z]$  versus stub length is presented in figure I-1.7. As indicated, the improvement of stub load impedance is a result of impedance transformation that is proportional to

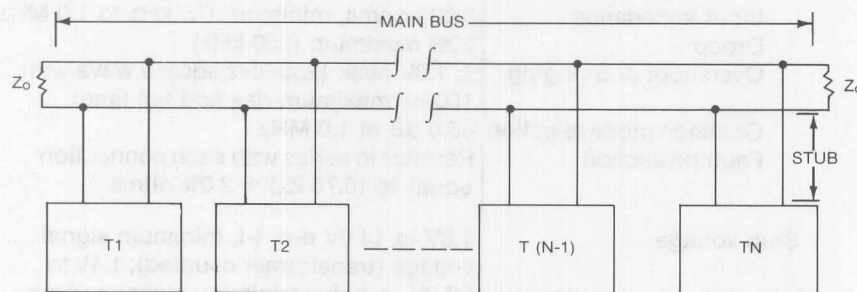


Figure I-1.5 Data Bus Network

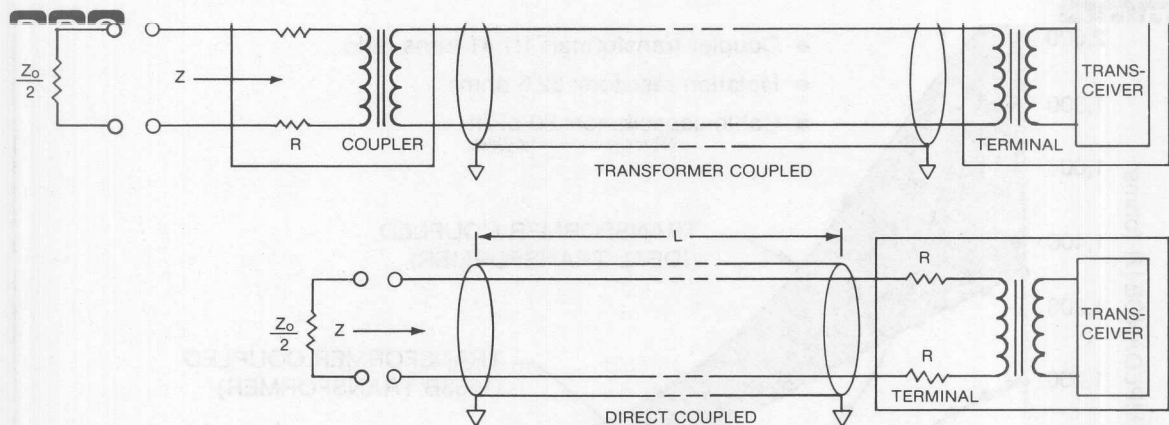


Figure I-1.6 Transformer Coupled and Direct Coupled Stubs

the square of the turns ratio, assuming an ideal transformer. The band of curves for the transformer-coupled case indicated by the darkened area between the curves results from assuming various values of transformer shunt impedance. The lower band is the curve using a transformer with the minimum impedance specified in 1553B. The upper bound is for an ideal transformer with very high impedance. All values of stub impedance are magnitude values for a 70-ohm cable with 30 pF/ft capacitance and are calculated for 1,000 ohms terminal input impedance, with the exception of the upper direct-coupled curve. This curve is based on the 1553B specified terminal input impedance of 2,000 ohms. It can be seen from these curves that stub impedance values are increased generally by use of the transformer, which provides at least a 2 to 1 improvement for the longer (greater than 10 ft.) stubs. The curves also show the importance of the transformer characteristics for maintaining the expected improvement.

As indicated above, the 1:1.41 transformer also provides ideal termination of the stub for transmission of signals from the terminal to the main bus. Impedance at the main bus is:

$$Z_B = \frac{Z_0}{2} + 2R$$

where,

$$R = 0.75 Z_0$$

$$Z_B = 0.5 Z_0 + 1.5 Z_0 = 2 Z_0 \text{ ohms}$$

$Z_0$  is the characteristic impedance of the data bus

and  $Z_R$  is the reflected impedance from the bus to the stub. Therefore, the transformer impedance transformation is:

$$Z_R = \frac{Z_B}{(1.41)^2} = \frac{2Z_0}{2} = Z_0$$

Therefore, the coupling transformer specified in 1553B provides the characteristics desired for reducing reflections and maintaining signal levels for systems where long stubs are required.

**Direct coupling can be used for stub connections of 3 ft or less if terminal input impedance is maintained at the specified value.**

Many configurations can be built reliably if careful attention is paid to the number, length and location of the stubs on the main bus. **It is highly desirable to test a proposed network using a computer simulation and a laboratory test setup.** The computer-generated data bus simulation provides more flexibility during the early design stages. The laboratory mockup with proper lengths of main bus and stubs is the final test of a good design.

## 1.6 The Most Frequently Asked Questions Concerning MIL-STD-1553

In an effort to help designers understand MIL-STD-1553, this section discusses some of the more frequently misunderstood portions of 1553 systems. Since 1553 is a standard and not a specification, it establishes requirements, which are

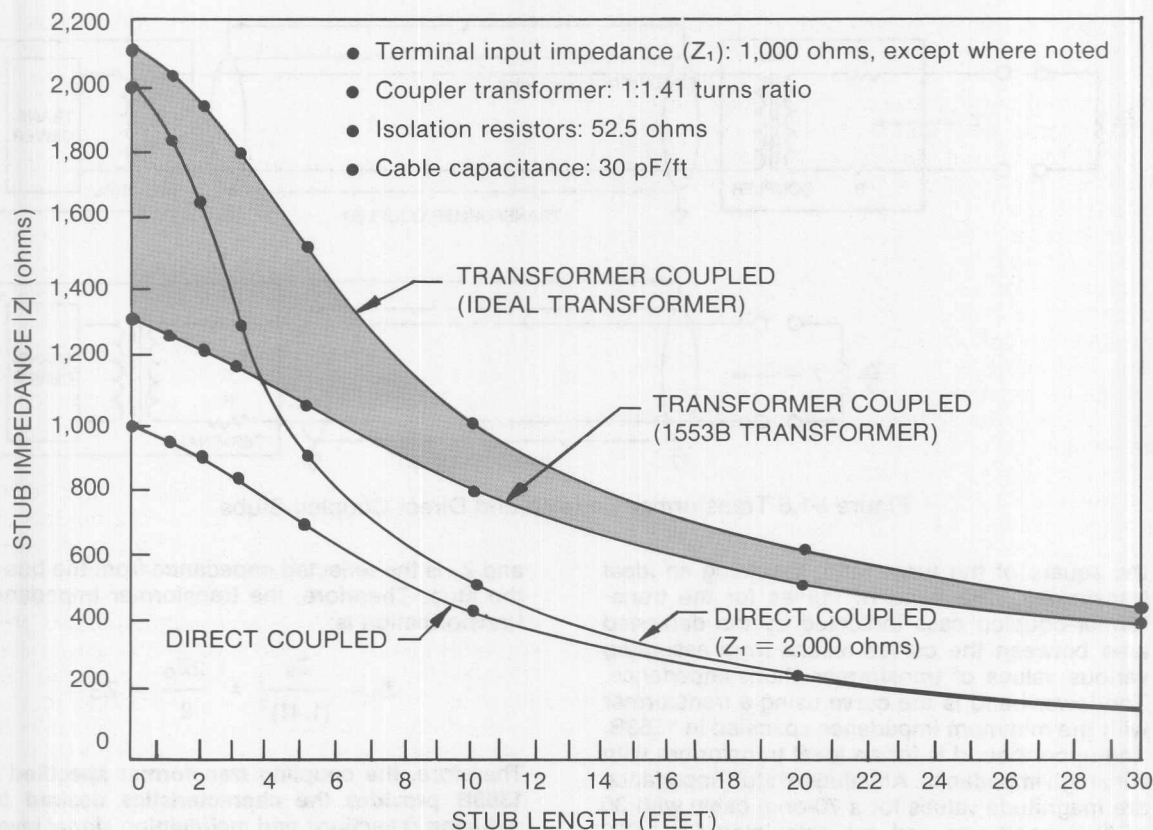


Figure I-1.7 Stub Impedance Versus Length

often hard to understand, and since the standard does not provide application guidance, questions arise. In order to solve this problem, the military has developed the "MIL-HDBK-1553 Multiplex Applications Handbook" to help convey the meaning of the standard and some lessons learned. In addition, industry and the government have jointly prepared a series of test plans which help clear up interpretations of the standard by defining how a test will be performed and the expected results. This designer's guide has been prepared to highlight some of the significant aspects for the designer.

#### 1.6.1 When to Transmit a Status Word [1553B paragraph 4.4.3.3 and 4.4.3.4]

The MIL-STD-1553 status word is a vital part of achieving the command/response protocol. **The transmission of a status word by a remote terminal indicates to the bus controller that the previous**

**command or command and data was received without error.** The suppression of the status word (status word not transmitted after reception of a command word) is used to indicate a message error exists if the message was NOT a broadcast message. Broadcast message formats require the status word to be suppressed to prevent a bus crash (multiple terminals transmitting simultaneously). Therefore, status words will always be transmitted for all error free, non-broadcast messages. Several types of errors can exist:

- (1) **If a command word contains an error, the terminal rejects the message and resets,** and starts "looking" for a new valid command word with its unique terminal address or the broadcast address. No status word transmission should occur.
- (2) **If a command word requests data from a sub-address, which is not operational for this terminal, the standard calls this failure an "illegal command".** Two options are available to the terminal designers; a) respond with the normal message

protocol required by the standard with data from a fixed location containing "don't care" data words, or b) design into the terminal the capability to recognize the failure and set the message error bit in the status word and transmit the status word only. **This is the only time when the status word will ever be transmitted with the message error bit set as a response to a non-mode code (normal) message.** If the remote terminal design selects method a) above, usually a common area of 32 data words is set aside and all unused subaddress transmit messages are retrieved from there and all unused subaddress receive messages are deposited there. This technique is called "responding in form". Thus, a garbage-in/garbage-out buffer is provided for all unused subaddresses, which are NOT to be transmitted by or requested by the bus controller in the first place. **The standard also identifies illegal commands as incorrect T/R bit setting and a word count that is not allowed in the terminal.** Since the standard allows the designer the choice of implementing this analysis or not, most designers ignore monitoring for illegal commands (use method a) above rather than implement the analysis. These designers depend on the bus controller NOT transmitting illegal commands see paragraph 1.6.3 also). SEAFAC testing is normally done to the above b) option.

(3) If the command word is a broadcast address 31, the terminal analyzes the message, sets the proper bits in the status word and then suppresses the transmission of the status word.

(4) If the command word is correct and the message contains an error then, the data is rejected, the message error bit is set in the status word and the status word is suppressed.

Therefore, **the suppression of the status word is used to indicate a broadcast message or an error condition.**

### 1.6.2 Superseding Valid Commands [1553B paragraph 4.4.3.2] and Reset Data Bus Transmitter [1553B paragraph 4.6.3.2]

The superseding valid command requirement in MIL-STD-1553B allows communication with a remote terminal that is presently working on a command. To better understand this requirement the data bus system redundancy needs to be considered. Both a single bus system and a dual standby redundant bus system (1553B paragraph 4.6.3) will be discussed.

MIL-STD-1553B states that a superseding command can not occur before time "T" (the response

time between command and status words-maximum 12 microseconds). In any bus system, an error condition exists if there is no response in time "T".

Communications can, therefore, be re-established with the remote terminal, if operational, by transmitting another command on the data bus that the previous command occurred on or any other data bus the terminal is connected to. Using **the superseding valid command requirement, the remote terminal is required to respond to the new command**, hopefully resolving the non-response to the previous command. This new command can be a normal message format or a mode code command.

In dual standby redundant systems, the "Reset Data Bus Transmitter" is a specific paragraph of 1553B (4.6.3.2) which provides specific requirements . . . **"If while operating on a command, a terminal receives another valid command, from either data bus, it shall reset and respond to the new command . . ."** Since another bus is available to the bus controller (i.e., the standby bus), the bus controller can transmit a new command to the remote terminal using the other bus. This allows the bus controller to identify messages containing a data word error, for example, to be retried on the alternate bus before the message is completed on the previous bus. It also allows the approach discussed in the paragraph above for any bus system to be used on either the active or standby bus to hopefully resolve the condition of a non-responding (silent) terminal. Therefore, superseding commands and reset data bus transmitters provide an effective means of recovery. This error management (e.g. retrying or resolving a no response) can be initiated rapidly, thus reducing bus down time (bus inefficiency).

### 1.6.3 Illegal Command [1553B paragraph 4.4.3.4]

As discussed in paragraph 1.6.1, concerning status word transmissions, illegal commands occur when; 1) an error exists in the T/R bit; 2) the subaddress/mode code field is an unused subaddress; or 3) an unimplemented mode code is transmitted. **The command word that contains an illegal condition must first meet all 1553B word validation requirements (1553B paragraph 4.4.1.1) before its illegal nature can be established.** If the command word does not meet these requirements, the remote terminal ignores the command. If the command word is correct, but has an illegal condition,



the standard allows the designers two options: provide NO unique capability in the remote terminal to recognize the condition and respond normally as if there was NOT an illegal command, and respond with the message error bit set in the status word. The first approach is often referred to as "responding in form". This means that the remote terminal uses the normal message protocol response (figure 6 and 7 of 1553B) and the receiving device (bus controller or remote terminal for an RT-RT message) will obtain "garbage" data. The second approach requires some analysis on the part of the remote terminal, but the response is straight forward. A message error has occurred and data should **NOT** be used. The message error alerts the bus controller of the problem. However, this is a system designer's problem which can not be solved by the bus controller. So reporting it helps no one. **Not using the data or having the data cause a remote terminal problem is the key.** This must be solved regardless of the selection of the option to respond with a status word or respond in form as if no illegal command occurred. To understand how this command can cause remote terminal data problems each illegal command will be examined.

(1) The impact of receiving a transmit/receive (T/R) bit set to the inverse of data flow can cause internal confusion and errors within the remote terminal or the system. If the T/R bit indicates the terminal is to transmit data, but the bus controller sends data to the terminal, a problem exists. **The remote terminal will recognize that data words are coming and the T/R is set to transmit and will NOT transmit.** However, the remote terminal must now deal with the incoming data words. Most terminal designs without illegal command detection hardware will still map the data to a designated memory location. This must be considered when mapping data into and out of memory. If detection hardware is available, the status word message error bit will be set and the status word transmitted. When the inverted T/R bit says receive data and no data follows the command word, a real message error exists - too few words and the message error bit will be set in the status word and its transmission will depend on if the detection circuitry is present. If not, the status word will be suppressed.

(2) The reception of a message to an unused subaddress can cause internal remote terminal problems. Most remote terminals are designed to use mapping schemes, which map messages to memory using the T/R bit and the subaddress. Therefore, an illegal command could cause data to

be written into areas of memory used for other functions. In the same way, improper data can be transmitted on the data bus by a remote terminal using an illegal command from an unused subaddress. This information could be anything and if used by a source could cause unknown responses. Therefore, as a minimum the designer should map all unused transmit and receive subaddresses to a common 32 word buffer that could be set to all zeros at initialization. Therefore, the first transmission of an unused subaddress should not affect anyone. After that if both receive and transmit commands arrive for unused subaddresses, the system could have problems. Obviously, additional memory space can be provided to separate receive and transmit unused subaddress memory areas to prevent bad data escaping the terminal. **Remember the bus controller is not allowed to transmit commands requesting or transmitting data from unused subaddresses of remote terminals.**

(3) Illegal commands which request action associated with unused or unimplemented mode codes must also be faced without causing remote terminal errors. These are more easily handled, because most remote terminals use chip sets which have selected when and how they will respond to each illegal mode condition. If you are interested in designing your own remote terminal, the "RT Validation Test Plan" (see Section VI) should be used as a reference guide in determining acceptable performance. **The general philosophy is to "respond in form", in other words, according to the protocol if it was legal.** This might mean bit bucketting data words or generating data words for transmission. If a remote terminal uses no mode codes (remember that Notice 2 requires at least four mode codes), subaddress codes 00000 and 11111 (the mode codes designator) is also not needed and it can be treated as an unused subaddress. Therefore, **even if a remote terminal designer chooses not to implement the option to analyze illegal commands, the design must be able to withstand the existence of these commands without causing the remote terminal internal errors or data bus system problems.**

#### 1.6.4 Invalid Command [1553B paragraph 4.4.3.3]

An invalid command in 1553B occurs when the command word fails to meet the criteria established for the word validation by the standard (1553B paragraph 4.4.1.1). These tests for proper sync, valid Manchester II bi-phase data, and information format of 16 bits plus odd parity are basic to



word they are essential. Since the protocol depends on a command/response action, remote terminals must only respond when "spoken to" (commanded to) by the bus controller. This is accomplished by the address validation (between the particular remote terminal's internal address and the address in the command word). Notice 2 requires that no single point failure in the address selection circuitry may cause a terminal to validate a false address. **To prevent multiple terminal reception or multiple terminals transmitting data, the command word must be correct.** Command word verification involves more than just using the remote terminal's address, it includes all of the 1553 required (4.4.3.5 in 1553B) word checks. Many remote terminal designers, in an effort to get a head start on handling a command word, examine only the address and fail to validate the remainder of the word before accepting it as a command.

#### 1.6.5 Impact of Notice 2 to MIL-STD-1553B

Notice 2 to MIL-STD-1553B, issued 8 September 1986, was developed to define which options within the standard were required to enhance tri-service interoperability of systems. The Notice goes on to further define some of the open-ended timing constraints which were undefined within the standard.

A notice to a standard is applied whenever the standard is referenced or specified. The notice does not apply to previous versions of the standard or applications to which the standard was applied prior to the release date of the notice. Waivers to the notice can be sought using the same technique allowed for the standard.

Notice 2 to MIL-STD-1553B supersedes Notice 1. The primary Notice 2 restrictions to the standard are as follows:

##### (1) Broadcast Message Formats

Broadcast message formats are not restricted from being implemented in hardware. However, use of the broadcast command is limited to mode code commands only. This is a major departure from the Notice 1 restrictions which prohibited broadcast messages altogether. The broadcast option for non-mode code messages may be designed into the remote terminal. If implemented, then the terminal MUST be capable of distinguishing between broadcast and non-broadcast messages to the same subaddress.

The terminal hardware may be designed with any or all mode codes, but the following mode codes must be implemented: transmit status word, transmitter shutdown, override transmitter shutdown, and reset remote terminal. Remote terminals must be designed to recognize both 00000 and 11111 as a designator in the subaddress/mode code field of the command word. The two indicators must not convey different information. Also bus controllers must be designed to support all modes regardless of system usage.

For Air Force applications, the bus controller is prohibited from issuing a dynamic bus control mode code (one of the few exceptions to a total tri-service agreement).

Also timing constraints have been established for two of the mode codes: reset remote terminal, and initiate RT self test. For the reset remote terminal, the terminal must complete its reset function within 5 milliseconds after transmitting its status word to this command. For the initiate self test mode code, the terminal must complete its self test function within 100 milliseconds after transmitting its status word to this command. In both cases, while the terminal is performing the commanded function (reset or self test) the terminal may respond to a valid command by: a) no response on either bus, b) status word transmitted with the busy bit set; or c) normal response. However, any data transmitted as the result of this command **MUST** be valid data.

##### (3) Status Word Bits

The only required status word bit is the message error bit. However, if the terminal employs broadcast recognition, capability of dynamic bus control, RT built-in-test, or subsystem built-in-test, then the bits in the status word associated with these functions are also required.

The busy bits' use (due to existence of busy conditions within a terminal) is **strongly discouraged**. However if these conditions affect the terminal's ability to properly communicate via the bus, then the busy bit is to be used. Setting of the busy bit must be caused by the result of a command to the terminal. The busy bit may also be set as the result of a failure within the terminal or subsystem.

##### (4) Message Formats and Subaddresses

Remote terminals must be capable of the following non-broadcast message formats: RT-BC, BC-RT,

RT-RT (receive and transmit), and mode codes commands without data words. Bus controllers must have the capability to transmit all message formats.

The remote terminal must provide a data wrap-around capability equal to the maximum number of data words its capable of processing for any subaddress. The desired subaddress for this function is 30 [11110]. The purpose of this function is to provide the bus controller the capability to test the data flow through a terminal's front end (1553 hardware), initial subsystem interface (memory buffers), and the data bus media (cabling and bus couplers).

#### (5) RT-RT Timeout

In addition to normal message validation criteria, the remote terminal must timeout (invalidate the message) if the receive command word is not followed by the first data word within  $57 \pm 3$  microseconds. Although this poses few problems for current hardware designs and chip sets, some of the earlier designs would wait "forever" then take the data intended for some other terminal (the transmitting terminal's status word was ignored since it contained a command/status sync).

#### (6) Electrical

The data bus cable characteristics have been tightened in the area of cable shielding (90%), connector/junction shielding (360 degrees at 75%), and impedance (actual to within the range of 70-85 ohms at 1 megahertz). In addition, the polarity for concentric connectors has been defined with the center pin being the high (positive) bus signal and the inter-ring being the low (negative) bus signal. The outer ring is obviously the bus shield.

#### (7) Coupling Stubs

For Navy applications, terminals must have both transformer coupled stub and direct coupled stub connections externally available (either may be used). For Army and Air Force applications, only transformer coupled stubs are required.

The remote terminal must limit spurious output signals during power up or down sequences to  $\pm 250$  mv for transformer coupled stubs and  $\pm 90$  mv for direct coupled stubs.

### 1.6.6 Responses to Non-Implemented Mode Code Commands and Undefined Mode Codes

Table 1 of 1553B and paragraph 4.3.3.5.1.7 define

mode codes while paragraph 4.3.3.6.4 identify the two types of mode codes; without data word and with data word. Table 1 also identifies a group of mode codes as RESERVED. However, table 1 fails to identify all of the binary combinations that can exist in the T/R bit and five bit mode code field. Table I-1.3 expands the 1553B table to include these possibilities. As can be seen 22 of the 64 entries are undefined and are considered INVALID. Notice from the table that these DO NOT include the RESERVED mode codes.

Several terms must be clearly defined in order to proceed with an explanation of the handling of RESERVED mode codes or UNDEFINED mode codes. For convenience, the following definitions are recapitulated with reference to 1553B.

**Valid Words.** (paragraph 4.4.1.1) Every word must meet 4 tests of validity to be declared a valid word. These tests are:

- Valid sync field.
- All bits are encoded as valid Manchester II code.
- The information field has 16 bits + 1 parity bit.
- The parity over the word is odd parity.

A word failing any of these tests would be considered to be invalid.

**Invalid Command.** (paragraph 4.4.3.3) A command that does not have an RT address field that matches the address of the receiving RT or that does not have an address of 11111 if the broadcast option is implemented in the RT, or that fails to satisfy the test for a valid word shall be considered to be an invalid command.

**Invalid data reception.** If any data word that is part of a BC to RT message fails the tests for being a valid word, or if the message transmission is not contiguous, or if the number of data words received is not correct (does not match the command word count field), an invalid data reception has occurred.

**Illegal commands.** (paragraph 4.4.3.4) An illegal command is a valid command word, but which contains a combination of T/R bit, subaddress-/mode field, and data word count/mode code field that has not been implemented in the receiving RT. Notwithstanding a side discussion as to which commands may be considered to be optional, the detection of illegal commands is itself optional.

Now the rules for setting of the message error bit in the status word and when to transmit status or

Table I-1.3 MIL-STD-1553B Mode Command Organization

T/R	MODE CODE	DATA WORD ASSOCIATED	BROADCAST ALLOWED	RESERVED	INVALID
0	00000	UND	UND	UND	YES
0	00001	UND	UND	UND	YES
0	00010	UND	UND	UND	YES
0	00011	UND	UND	UND	YES
0	00100	UND	UND	UND	YES
0	00101	UND	UND	UND	YES
0	00110	UND	UND	UND	YES
0	00111	UND	UND	UND	YES
0	01000	UND	UND	UND	YES
0	01001	UND	UND	UND	YES
0	01010	UND	UND	UND	YES
0	01011	UND	UND	UND	YES
0	01100	UND	UND	UND	YES
0	01101	UND	UND	UND	YES
0	01110	UND	UND	UND	YES
0	01111	UND	UND	UND	YES
0	10000	UND	UND	UND	YES
0	10001	YES	YES	NO	NO
0	10010	UND	UND	UND	YES
0	10011	UND	UND	UND	YES
0	10100	YES	YES	NO	NO
0	10101	YES	YES	NO	NO
0	10110	YES	TBD	YES	NO
0	10111	YES	TBD	YES	NO
0	11000	YES	TBD	YES	NO
0	11001	YES	TBD	YES	NO
0	11010	YES	TBD	YES	NO
0	11011	YES	TBD	YES	NO
0	11100	YES	TBD	YES	NO
0	11101	YES	TBD	YES	NO
0	11110	YES	TBD	YES	NO
0	11111	YES	TBD	YES	NO
1	00000	NO	NO	NO	NO
1	00001	NO	YES	NO	NO
1	00010	NO	NO	NO	NO
1	00011	NO	YES	NO	NO
1	00100	NO	YES	NO	NO
1	00101	NO	YES	NO	NO
1	00110	NO	YES	NO	NO
1	00111	NO	YES	NO	NO
1	01000	NO	YES	NO	NO
1	01001	NO	TBD	YES	NO
1	01010	NO	TBD	YES	NO
1	01011	NO	TBD	YES	NO
1	01100	NO	TBD	YES	NO
1	01101	NO	TBD	YES	NO

T/R	MODE CODE	DATA WORD ASSOCIATED	BROADCAST ALLOWED	RESERVED	INVALID
1	01110	NO	TBD	YES	NO
1	01111	NO	TBD	YES	NO
1	10000	YES	NO	NO	NO
1	10001	UND	TBD	UND	YES
1	10010	YES	NO	NO	NO
1	10011	YES	NO	NO	NO
1	10100	UND	TBD	UND	YES
1	10101	UND	TBD	UND	YES
1	10110	YES	TBD	YES	NO
1	10111	YES	TBD	YES	NO
1	11000	YES	TBD	YES	NO
1	11001	YES	TBD	YES	NO
1	11010	YES	TBD	YES	NO
1	11011	YES	TBD	YES	NO
1	11100	YES	TBD	YES	NO
1	11101	YES	TBD	YES	NO
1	11110	YES	TBD	YES	NO
1	11111	YES	TBD	YES	NO

TBD = "To be Determined" as indicated in 1553B.

UND = "Undefined, not specifically assigned in 1553B.

to suppress transmission of a status word will be reviewed.

Paragraph 4.3.3.5.3.3 states that the message error (ME) bit of a status word shall be set to indicate that:

1. One or more of the data words associated with the proceeding BC-to-RT command (receive command) was not a VALID WORD, or
2. The message transmission was not contiguous per paragraph 4.4.1.2, or
3. The command received was an ILLEGAL COMMAND and the RT has implemented the option for illegal command detection, or
4. There was an INVALID DATA RECEPTION.

Based on paragraphs 4.4.3.1 and 4.4.3.5, a status word response is required if the RT receives a command that is a valid command and if any associated data reception is a valid data reception. Paragraph 4.4.3.3 specifically states that a RT shall not respond to an INVALID COMMAND and paragraph 4.4.3.6 requires the status word response be suppressed for the case of INVALID DATA RECEPTION.

By definition, RESERVED mode codes are represented by command word formats that have been defined in table 1 of 1553B, but which are not to be implemented at present. Consequently, an RT design will not implement these T/R, subaddress-/mode field, and data word/mode code combinations and if the RT receives such a combination, it must regard the command as an ILLEGAL COMMAND per the definition given in the standard. The proper action required, per the standard, is to set the ME bit of the status word and transmit the status word to the bus controller, if the option for illegal command monitoring is being observed.

Notice that there is no restriction on a bus controller not to transmit a RESERVED mode code command. RESERVED mode commands may be defined in the future, in which case receipt of that command would be an absolutely normal occurrence. Simply treating the RESERVED mode commands as an ILLEGAL COMMAND is consistent with the potential for future expansion of mode commands since a pre-existing RT design should not implement the new command created from a RESERVED mode command. The "RT Validation Test Plan" (Notice 1 to MIL-HDBK-1553) supports this discussion.



The UNDEFINED mode code commands present a more difficult situation. If an RT receives an undefined mode command, by default it could treat this command as an ILLEGAL COMMAND from the standpoint of its being a combination of T/R, subaddress/mode, and data word/mode code fields that definitely will not have been implemented by the RT design. But the undefined mode command can be regarded as an ILLEGAL COMMAND only if it is also a valid command. This point raises questions as to how such a command came to be received by the RT. **Since the undefined mode command is not a valid combination of T/R, subaddress/mode field, and data word/mode code field as defined in table 1 of 1553B, it must be presumed that a bus controller would never purposely send such a combination.** The case can be made that some failure mode has to have occurred in order for the command received by the RT to be interpreted as an undefined mode command. Invalid encoding, undetected multiple bit errors, or bus controller failures could be possible sources for the erroneous mode command. It may be surmised that the receipt of an undefined mode command implies that the command could be an INVALID COMMAND. It is also possible that all of the checks for validity of the command word genuinely pass, but that a failure mode in the bus controller has resulted in the transmission of an undefined mode command. As such, it would be proper to regard the command as an ILLEGAL COMMAND and to set the ME bit of the status word register and either transmit or suppress the status word depending on the implementation of the ILLEGAL COMMAND option.

The validity of the command determines whether or not a status response is to be sent. Due to the likelihood that the undefined command is in reality an INVALID COMMAND generated by undetected errors in encoding, **the safest approach to the decision concerning whether or not to transmit the status word would be to suppress transmission of the status word.**

So, depending upon the failure mode that produces an undefined mode command, attributes of either an ILLEGAL COMMAND or an INVALID COMMAND or both may be present. The required response is not clear since the prescribed responses are opposing when comparing an ILLEGAL COMMAND with an INVALID COMMAND. For this reason, this category of command is sometimes referred to an illogical command. By implementing the dominant responses for both an ILLEGAL COMMAND and for an INVALID COM-

MAND, the safest overall response results. **The ME bit of the status word is set to indicate an error and the transmission of the status word is suppressed to prevent violation of the command/response protocol for a potentially INVALID COMMAND.** Suppression of the transmission of the status word in response to the receipt of an undefined/illogical command has the added benefit of distinguishing the associated failure mode from the receipt of a reserved mode command. In any event, diagnosability of errors resulting from the receipt of an improper mode command can be improved by providing bits in the BIT word to expand the encoding of errors.

The "RT Validation Plan" allows two responses; a) treat the condition as an ILLEGAL COMMAND, or b) treat the condition as an INVALID COMMAND. In the first case, the terminal would respond with a status word with no errors set if it did not have ILLEGAL COMMAND detection capability. If the terminal did have ILLEGAL COMMAND detection capability, a status word with the ME bit set would be transmitted only. In the second case, if the INVALID COMMAND was detected, the status response would be suppressed and the ME bit set in the status word. This message error would NOT be recorded by the bus controller unless the next message was a transmit status word mode code or transmit last command word mode code.

### 1.6.7 Two Single Channel Remote Terminals Operating in a Dual Standby Redundant System

A few remote terminal designers have designed subsystems using the channel concept (see figure I-3.7 right side) only to discover that the terminal failed to meet all the 1553B requirements when used in a dual standby redundant data bus network (see 1553B paragraph 4.6.3). 1553B provides certain general capabilities which are influenced when a system is operating in a dual standby redundant network, as most are, compared to a single channel network. Mode codes that convey the operational capability of the entire remote terminal as compared to that of the channel are the most affected; a) transmit status word, b) reset remote terminal, c) transmit last command word, and d) transmit BIT word. Transmit status word mode code provides the message error results of the last message processed by the terminal regardless of which bus (channel - active or standby) the message was received on. The other bits in the status word represent the health of the entire terminal, not just the channel receiving the request. The reset remote terminal mode code also applies



to the entire terminal and NOT just the channel the request was received on. Transmit last command word must come from a register which contains the 16 bit contents of the last command received regardless of the bus received on. The same is true for the terminal's BIT word and vector word, it must reflect the terminal's state and not that of channel. Figure I-3.7 illustrates that too little redundancy is unacceptable just as well as too much isolation is unacceptable.

### 1.6.8 Testing of 1553 Terminals

MIL-STD-1553B terminal testing has been conducted by designers and the US Air Force SEAFAC Laboratories at Wright Patterson AFB. In the past, the proof that a terminal's design was acceptable, required it to pass the SEAFAC Validation Tests. Several years ago, the government recognized that a single laboratory could not test everyone's designs. With the increasing numbers and suppliers of 1553 embedded terminals and the extensive number of chip sets being developed, something had to be done to distribute the testing load while maintaining the highly successful design verification effort.

To this end, the SAE Avionics Systems Division and the government began developing a series of verification and production test plans and procedures which could be conducted by independent laboratories to validate the design approach and provide a basis for production level testing of 1553 terminals. This approach would allow multiple industry sources to be used to verify compliance of a design and provide industry with ground rules for production testing. It was clear from the beginning that remote terminal test plans were required first, followed by bus controller test plans and then system data bus test plans. The initial remote terminal test plans grew out of the test procedures developed and used at SEAFAC. It was obvious from the start that the test plans would set a lower level of definition for "acceptable terminal performance" than existed in the standard. This caused extensive work and coordination between industry and the government. Today (7/87) these test plans are available in preliminary form from the SAE (Society of Automotive Engineering) under the following Aerospace Standard numbers:

AS4111      Validation Test Plan for Aircraft  
Rev. D      Internal Time Division Command/  
3/84      Response Multiplex Data Bus  
Remote Terminals. (See Section VI).

AS4112      Production Test Plan for Aircraft  
Rev.      Internal Time Division Command/  
4/85      Response Multiplex Data Bus  
Remote Terminals. (See Section V).

AS4113      Validation Test Plan for Aircraft  
Rev. F      Internal Time Division Command/  
3/86      Response Multiplex Data Bus  
Controllers.

AS4114      Production Test Plan for Aircraft  
Final Draft      Internal Time Division Command/  
2/87      Response Multiplex Data Bus  
Controllers.

AS4115      Test Plan for the Digital Internal  
Final Draft      Time Division Command/Response  
2/87      Multiplex Data Bus System.

Note that the Validation Test Plan for Remote Terminals (AS4111) has been adapted by the military and released as Notice 1 to MIL-HDBK-1553 Multiplex Applications Handbook.

In the near future, these documents will be approved by the SAE and published as Aerospace Standards. The military is considering placing some of these in future updates of MIL-HDBK-1553 Handbook. Some differences still exist between the SEAFAC test plans and procedures and the SAE documents which must be resolved. In addition, with the release of Notice 2 to MIL-STD-1553B, these documents will be updated by the SAE.

## 2.0 A Comparison of Data Bus Specifications

Today several MIL-STD-1553 data bus systems are in full use. To better understand the slight differences between these systems, this section consists of several tables comparing performance characteristics of MIL-STD-1553B and several aircraft specifications (e.g., A-10, F-16, F-18, and B-52). Most 1553 applications will require an aircraft specification in addition to MIL-STD-1553B to allow the aircraft designer a method of identifying the applicable options of the standard. Prior to MIL-STD-1553B these aircraft specifications provided the appropriate level of detail, since earlier versions of the standard were unclear in several critical design areas. Each of these parameters can be examined on a comparative basis using these tables.

A thorough paragraph by paragraph analysis of MIL-STD-1553B is given in Section II, where differences between A and B and the reasons for various requirements are discussed.

## 2.1 Summary of Data Bus Requirements

Table I-2.1 Summary of Data Bus Requirements

Applications	DoD Avionics
Data Rate	1 MHz
Word Length	20 bits
Number of data bits/word	16
Transmission technique	half-duplex
Operation	Asynchronous
Encoding	Manchester II biphase
Bus Coupling	Transformer
Bus Control	Single or multiple
Transmission media	Twisted pair shielded

## 2.2 Summary of Status Word Protocols

Table I-2.2 Summary of Status Word Protocol for Various Message Errors

Error Condition	Application					
	F-16*A/C	B-52 OAS	A-10	F-18	OH-58D	1553B Notice 2
Data Parity Error	Transmit Status	Suppress Status	Transmit Status	Transmit Status	Suppress Status	Suppress Status
Invalid Data (invalid sync. code, bit count)	Transmit Status	Suppress Status	Transmit Status	Transmit Status	Suppress Status	Suppress Status
No Data Received	Suppress Status	Suppress Status	Suppress Status	Suppress Status	Suppress Status	Suppress Status
Word Count Error	Suppress Status	Suppress Status	Suppress Status	Suppress Status	Suppress Status	Suppress Status

Note that for a broadcast command, the status word is always suppressed. The broadcast command received bit shall not be set if a message error occurs for a broadcast message.

\* F-16A/C message error bit set for data parity error only.

## 2.3 Summary of Status Word Bit Assignments

Table I-2.3 Summary of Status Word Bit Assignments

Status Bits	B-52 OAS	A-10	F-18	F-16 A/C	OH-58D	1553B Notice 2	1553A
Sync	1-3	1-3	1-3	1-3	1-3	1-3	1-3
Terminal Address	4-8	4-8	4-8	4-8	4-8	4-8	4-8
Message Error	9	9	9	9	9	9	9
Instrumentation	NU	10	NU	10	NU	10	u
Data Quality*	NU	NU	NU	11†	NU	NU	u
Service Request	15	NU	10-18‡	NU	11	11	u
Broadcast Received	NU	NU	NU	15	NU	15	u
Busy	16	NU	NU	NU	16	16	u
Subsystem Flag	10-14	NU	NU	NU	17	17	u
Dynamic Bus Control Acceptance	NU	NU	NU	NU	NU	18§	u
Dedicated Function Received*	NU	NU	NU	16	NU	NU	u
Bus Shutdown**	NU	17-18	NU	17-18	NU	NU	u
Reserved	17-18	11-16	NONE	12-14	12-14	12-14	u
Terminal Flag	19	19	19	19	19	19	19
Parity	20	20	20	20	20	20	20

Note: Bits which are not used shall be considered reserved per the application and set to zero.

\* F-16 unique

‡ F-18 unique

\*\* F-16 and A-10 unique

u Undefined

† F-16 uses data parity  
same as message error

§ Not permitted in Air Force  
applications

NU Not Used

## 2.4 Summary of Mode Code Usage

Table I-2.4 Summary of Mode Code Usage

MODE COMMANDS	MODE CODES							
	B-52	A-10	F-18	F-16 A/C	OH-58D	1553B Notice 2	1553A	
WITHOUT DATA								
Dynamic Bus Control	NU	NU	0	NU	NU	0	ND	
Synchronize	NU	NU	NU	1	1	1	ND	
Transmit Status	1	NU	NU	2-31	2	2	ND	
Initiate Self Test	2	NU	NU	NU	3	3	ND	
Transmitter Shutdown	3	NU	NU	NU	NU	4	ND	
Override Shutdown	4	NU	NU	NU	NU	5	ND	
Inhibit T/F	NU	NU	NU	NU	NU	6	ND	
Override Inhibit T/F	NU	NU	NU	NU	NU	7	ND	
Reset RT	NU	NU	NU	NU	NU	8	ND	
DATA FROM TERMINAL								
Transmit Vector	NU	NU	NU	NU	NU	16	ND	
Transmit Last Command	NU	NU	NU	NU	NU	18	ND	
Transmit Bit Word	NU	NU	NU	NU	19	19	ND	
DATA TO TERMINAL								
Synchronize	NU	NU	NU	NU	NU	17	ND	
Selected Shutdown	NU	NU	NU	NU	NU	20	ND	
Selected Override	NU	NU	NU	NU	NU	21	ND	
ILLEGAL MODE CODES	0,5-31	ALL	1-31	NONE	9-15, 22-31	9-15, 22-31	ND	

NU = Not Used

ND = Not Defined

## 2.5 Comparison of Data Bus Characteristics

Table I-2.5 Comparison of Data Bus Characteristics

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
1. Twisted, shielded, jacketed	Yes 4.2.4.1	Yes 4.5.1.1
2. Minimum cable shield coverage	80% 4.2.4.1	75% 4.5.1.1
3. Minimum cable twist	1 twist/in (12 twists/ft) 4.2.4.1	4 twists/ft 4.5.1.1
4. Wire-to-wire distributed capacitance (maximum)	30 pF/ft 4.2.4.1	30 pF/ft 4.5.1.1
5. Characteristic impedance of cable	70 $\pm$ 10% at 1 MHz 4.2.4.2	Nominal 70 to 80 at 1 MHz 4.5.1.2
6. Cable attenuation	1 dB/100 ft at 1 MHz 4.2.4.3	1.5 dB/100 ft at 1 MHz 4.5.1.3
7. Cable length	300 ft maximum 4.2.4.4	Unspecified —
8. Cable termination using a resistance at both ends	Characteristic impedance 4.2.4.6	Nominal characteristic impedance $\pm$ 2% 4.5.1.4
9. Cable stubbing	Transformer coupling for stubs longer than 1 ft but less than 20 ft; direct coupling if stub is less than 1 ft; maximum stub length of 20 ft 4.2.4.5 Figure II-14 page II-41	Transformer coupling or direct coupling allowed; maximum stub length suggested 20 ft  4.5.1.5.1 or 4.5.1.5.2
10. Cable coupling (connector)	Compatible with Amphenol type 31-235 or Trompeter type TEI-14949-E137 receptacles and Amphenol type 31-224 or Trompeter type TEI-14949-PL36 plugs 4.2.4.6	Figures 9 or 10 of 1553B Unspecified —



Table I-2.5 Comparison of Data Bus Characteristics (Continued)

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
11. Cable coupling shielded box	Shielded coupler box 4.2.4.6	75% coverage, minimum 4.5.1.5.1.3 and 4.5.1.5.2.2
12. Coupling transformer turns ratio	Unspecified —	1:141 ± 3% higher turns on isolation resistor side of stub 4.5.1.5.1.1
13. Transformer open circuit impedance	Unspecified —	3,000 ohms over frequency of 75 kHz -1 MHz with 1V RMS sine wave 4.5.1.5.1.1.1
14. Transformer waveform integrity	Unspecified —	Droop not to exceed 20% overshoot and ringing less than ± 1V peak undertest of figure 11 of 1553B 4.5.1.5.1.1.2
15. Transformer common mode rejection	Unspecified —	45 dB at 1MHz 4.5.1.5.1.1.3
16. Fault isolation — Isolation resistor in series with data bus cable (coupler)	$R = 0.75Z_o^* \pm 5\%$ 4.2.5.2	$R = 0.75 Z_o^* \pm 2\%$ 4.5.1.5.1.2
Direct coupled case with the isolation resistor in the RT	Figure II-14 page II-41	$R = 55 \text{ ohms} \pm 2\%$ 4.5.1.5.2.1 Figure 10 of 1553B
17. Impedance across the data bus for any failure of coupling transformer, cable stub, or terminal receiver and transmitter transformer coupling Direct coupling	No less than $1.5 Z_o^*$ 4.2.5.2	No less than $1.5 Z_o^*$ 4.5.1.5.1.2  No less than 110 ohms 4.5.1.5.2.3
18. Stub voltage requirements and input level transformer coupling	**Range of the 0.5V to 10V peak; 1.0V to 20V p-p, I-I 4.2.5.4.1 Figure II-14 page II-41	**Range of 1.0V to 14.0V p-p**, I-I with one fault as stated in 17 above 4.5.1.5.1.4 Figure 9 of 1553B

\* $Z_o$  = cable normal characteristic impedance

\*\*Assumes one fault of a coupling transformer, cable stub, or terminal receiver or transmitter

Table I-2.5 Comparison of Data Bus Characteristics (Concluded)

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
Direct coupling  19. Wiring and cabling for electromagnetic capability	**Range of the 0.5V to 10V peak; 1.0V to 20V p-p, I-I 4.2.5.4.1 Figure II-14 page II-41 MIL-E-6051 4.2.4.7	**Range of 1.4V to 20V p-p, I-I with one fault as stated in 17 above 4.5.1.5.2.3 Figure 10 of 1553B MIL-E-6051 4.5.1.5.3

\*\*Assumes one fault of a coupling transformer, cable stub, or terminal receiver or transmitter

## 2.6 Comparison of Terminal Characteristics

Table I-2.6 Comparison of Terminal Characteristics

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
1. Output level — transformer coupling	$\pm 3.0V$ to $\pm 10V$ peak (6.0V to 20.0V p-p) I-I with no faults; with one fault of a coupling transformer, cable stub, or terminal receiver-transmitter, $\pm 2.25V$ to $\pm 11.25V$ peak (4.5V to 15V p-p) I-I 4.2.5.3.1	With $R_L = 70 \pm 2\%$ , 18.0V to 27.0V p-p, I-I  4.5.2.1.1.1 Figure 12 of 1553B With $R_L = 35 \pm 2\%$ , 6.0V to 9.0V p-p, I-I 4.5.2.2.1.1 Figure 12 of 1553B
Direct coupling		$\pm 25$ ns 4.5.2.1.1.2 Figure 12 of 1553B
2. Output waveform — Zero crossing deviation	$\pm 25$ ns 4.2.5.3.2 Point C, figure II-14 page II-41	$\pm 25$ ns 4.5.2.1.1.2 Figure 12 of 1553B
Rise and fall time (10% to 90%)	$\geq 100$ ns 4.2.5.3.2 Figure 13 of 1553B	100 to 300 ns 4.5.2.1.1.2 Figure 13 of 1553B
Transformer coupling distortion (including overshoot and ringing)	Unspecified	$\pm 900$ -mV peak, I-I 4.5.2.1.1.2 Point A, figure 12 of 1553B
Direct coupling distortion (including overshoot and ringing)	Unspecified	$\pm 300$ -mV peak, I-I 4.5.2.2.1.2 Point A, figure 12 of 1553B
3. Output noise — Transformer coupling	10-mV p-p, I-I 4.2.5.3.3 Point A, figure II-14 page II-41	14-mV, RMS, I-I 4.5.2.1.1.3 Point A, figure 12 of 1553B

Table I-2.6 Comparison of Terminal Characteristics (Continued)

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
Direct coupling		5-mV, RMS, I-I 4.5.2.2.1.3 Point A, figure 12 of 1553B
4. Output symmetry (after 2.5 us of midbit crossing of the last parity bit — Transformer coupling	Unspecified	$\pm 250$ -mV peak, I-I 4.5.2.1.1.4 Point A, figure 12 of 1553B
Direct coupling	Unspecified	$\pm 90$ -mV peak, I-I 4.5.2.2.1.4 Point A, figure 12 of 1553B
5. Input waveform — Maximum zero crossing deviation	Unspecified	$\pm 150$ ns 4.5.2.1.2.1 Point A, figures 9 or 10 of 1553B
6. Input signal response range Transformer coupling	$\pm 0.5$ V to $\pm 10.0$ V peak (1.0V to 20V p-p), I-I 4.2.5.4.1 Point C, figure II-14 page II-41	0.86V to 14.0V p-p, I-I  4.5.2.1.2.1 Point A, figure 9 of 1553B
Direct coupling		1.2V to 20V p-p, I-I 4.5.2.2.2.1 Point A, figure 10 of 1553B
7. Input signal no response range Transformer coupling	Unspecified	0.0V to 0.2V p-p, I-I 4.5.2.1.2.1 Point A, figure 9 of 1553B
Direct coupling	Unspecified	0.0V to 0.28V p-p, I-I 4.5.2.2.2.1 Point A, figure 10 of 1553B



Table I-2.6 Comparison of Terminal Characteristics (Concluded)

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
8. Common mode rejection	$\pm 10.0V$ peak, line-to-ground, dc to 2 MHz 4.2.5.4.2 Point A, figure II-14 page II-41	$\pm 10.0V$ peak, line-to-ground, dc to 2 MHz 4.5.2.1.2.2 or 4.5.2.2.2.2 Point A, figures 9 or 10 of 1553B
9. Input impedance — Transformer coupling	Minimum of 2,000 ohms over a frequency range of 100 kHz to 1 MHz, I-I 4.2.5.4.3 Point C, figure II-14 page II-41	Minimum of 1,000 ohms over a frequency range of 75 kHz to 1 MHz, I-I 4.5.2.1.2.3 Point A, figure 9 of 1553B
Direct coupling		Minimum of 2,000 ohms over a frequency range of 75 kHz to 1 MHz, I-I 4.5.2.2.2.3 Point A, figure 10 of 1553B
10. Noise rejection or error rate — Transformer coupling	Maximum bit error rate of $10^{-12}$ and a maximum incomplete message rate of $10^{-6}$ in a configuration of one bus controller on a 20-ft stub with a minimum of 100 ft of main bus cable between coupling boxes; test is conducted in presence of magnetic field per MIL-STD-462 method RS02 (spike test) with the limits of MIL-STD-461 RS02 4.3.3	Maximum of one part in $10^7$ word error in the presence of additive white gaussian noise of 140-mV RMS over a bandwidth of 1.0 kHz to 4 MHz; input voltage 2.1V p-p, I-I Point A, figure 9 of 1553B, accept/reject Table II-6 page II-46
Direct coupling		4.5.2.1.2.4 Maximum of one part in $10^7$ word error rate in the presence of additive white gaussian noise of 200-mV RMS over a bandwidth of 1.0 kHz to 4 MHz; input voltage 3.0V p-p, I-I Point A, figure 10 of 1553B, accept/reject Table II-6 page II-47 4.5.2.2.2.4

Table I-2.7 Remote Terminal Characteristics

	1553A	1553B Notice 2	A-10	B-52 OAS	F-16 A/C	F-18	OH-58D
1. Terminal Address unique broadcast	■	■ ■	■	■	■	■	■
2. Subaddress/Mode Code Subaddress 0 (mode data) Subaddress 31 (mode data)	■	■ ■	■	■	■	■	■ ■
3. Response Time 4.0-7.0 $\mu$ s 4.0-12.0 $\mu$ s	■	■	■	■	■	■	
4. Transmission Bit Rate Long term Short term	$\pm 0.01\%$ $\pm 0.001\%$	$\pm 0.1\%$ $\pm 0.01\%$					
5. Terminal Fail-Safe Time Out 660 $\mu$ s 660-1000 $\mu$ s 800 $\mu$ s	■	■	■	■	■	■	■
6. No-Response Time Out 6.5 $\mu$ s 14 $\mu$ s 25 $\mu$ s Not Specified	■	■	■	■	■	■	■
7. Coupling Transformer Direct coupled only Transformer only Both	■	■	■	■	■	■	■
8. Transformer Ratio 1:1 $\pm 3\%$ 1:1.41 $\pm 3\%$ Unspecified	■	■	■	■	■	■	■

## 2.8 Transmitter/Receiver Response Voltage Range

Table I-2.8 Transmitter/Receiver Response Voltage Range

<b>Output Level</b> <u>Output Voltage Range (V)</u> 18.0–27.0 p-p, 1-1 6.0–20.0 p-p, 1-1 24.0–26.0 p-p, 1-1 28.0–36.0 p-p, 1-1	<u>RL</u> 70 ohm Unspecified 140 ohm 140 ohm	<u>Application</u> 1553B, Notice 2 1553A A-10, B-52 OAS, F-16A/C F-18
<b>Input Level</b> <u>Input Voltage Range (V)</u> Transformer Coupled 0.86–14.0 p-p, 1-1 1.0–20.0 p-p, 1-1	<u>No Response Range</u>  0.0–0.2v, p-p, 1-1 0.0–0.4v, p-p, 1-1	<u>Application</u>  1553B, Notice 2 A-10, B-52 OAS, OH-58D

1.0–20.0 p-p, 1-1 1.2–8.0 p-p, 1-1 *Not specified for 1553A	0.0–0.7v, p-p, 1-1* 0.0–0.9v, p-p, 1-1	F-18, 1553A F-16A/C
Direct Coupled 1.0–20.0 p-p, 1-1 1.2–8.0 p-p, 1-1 1.2–20.0 p-p, 1-1	0.0–0.7v, p-p, 1-1 0.0–0.9v, p-p, 1-1 0.0–0.28v, p-p, 1-1*	F-18 F-16A/C 1553B, Notice 2
Not Allowed		A-10, B-52 OAS, OH-58D

### 3.0 System Design

The interconnection of subsystems using MIL-STD-1553 can be subdivided into two categories; data bus topology and data bus control. Other areas of concern to the system designer are functional partitioning, redundancy, and data bus analysis. Each of these topics will be discussed in this section.

#### 3.1 Data Bus Topology

The topology of a data bus system is the map of physical connections of each unit to the data bus. **Two types of data bus topologies exist; single level and multiple level (hierarchical). The single level bus topology is the simplest interconnect scheme** and is the most commonly used architecture. In this approach **all terminals are connected to a single level bus** (see figure I-3.1a) or multiple single level buses (see figure I-1.3.1b) each with an equal topology relationship. Notice that this can occur regardless of the data bus redundancy requirements. The use of multiple buses for redundancy in a single level system does not change to type of topology. A more detailed discussion of redundancy follows later in this section.

**Multiple level or hierarchical bus topology is an extension of the single level concept.** If single level buses are interconnected in a certain manner, data on one bus system will pass to another bus system. These buses differ from the multiple bus systems shown in figure I-3.1b, because they are not equal.

Thus, one bus system is subservient to another bus system. This approach can be achieved using several different architectures as seen in figure I-3.2. **Several systems today are using this approach to achieve functional partitioning** (e.g., navigation to/from weapon delivery, avionics to/from stores management, etc.).

All 1553B data bus systems relate or communicate

with each other via two control schemes; equivalent levels of control and hierarchical levels of control. The most common approach is equivalent levels of control. In this approach, coordination is required only when data is transferred. The autonomous operation and individual error handling and recovery schemes remain for each bus. Since this mechanization is the simplest and achieves the greatest separation between data buses, it is widely used.

Hierarchical control schemes are viable and have been developed and analyzed in research applications, but until recently had few applications. With the development and application of MIL-STD-1760A (see paragraph 7.2) hierarchical control will be applied to control a weapons bus from avionics buses or store management system buses. The weapons bus may further control a 1553 protocol type bus within a store (missile or pod) to communicate directly with warheads, navigation, communication, or radar sensors. When these approaches are discussed in the literature, the **bus level inequality is usually expressed as local buses (subordinate - under submission of another bus) and global buses (superior-controller of local buses)**. Regardless of the control scheme selected, each of these methods fit into a single category; multiple levels or hierarchical.

#### 3.2 Data Bus Control

##### 3.2.1 Bus Control Mechanization

The second part of the bus topology description is the control philosophy. Two terms have been used in the literature to describe these control schemes; stationary master and non-stationary master. The stationary master approach to bus control occurs when a single bus controller manages the bus communication for all devices on the data bus. If this bus controller fails, depending on redundancy requirements, a backup bus controller can take over operation of the bus. This takeover procedure

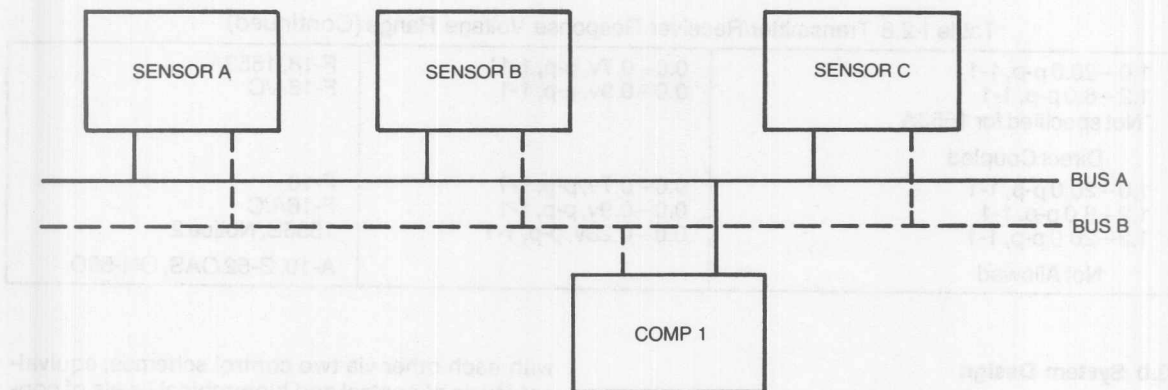


Figure I-3.1a Single Level Bus Topology

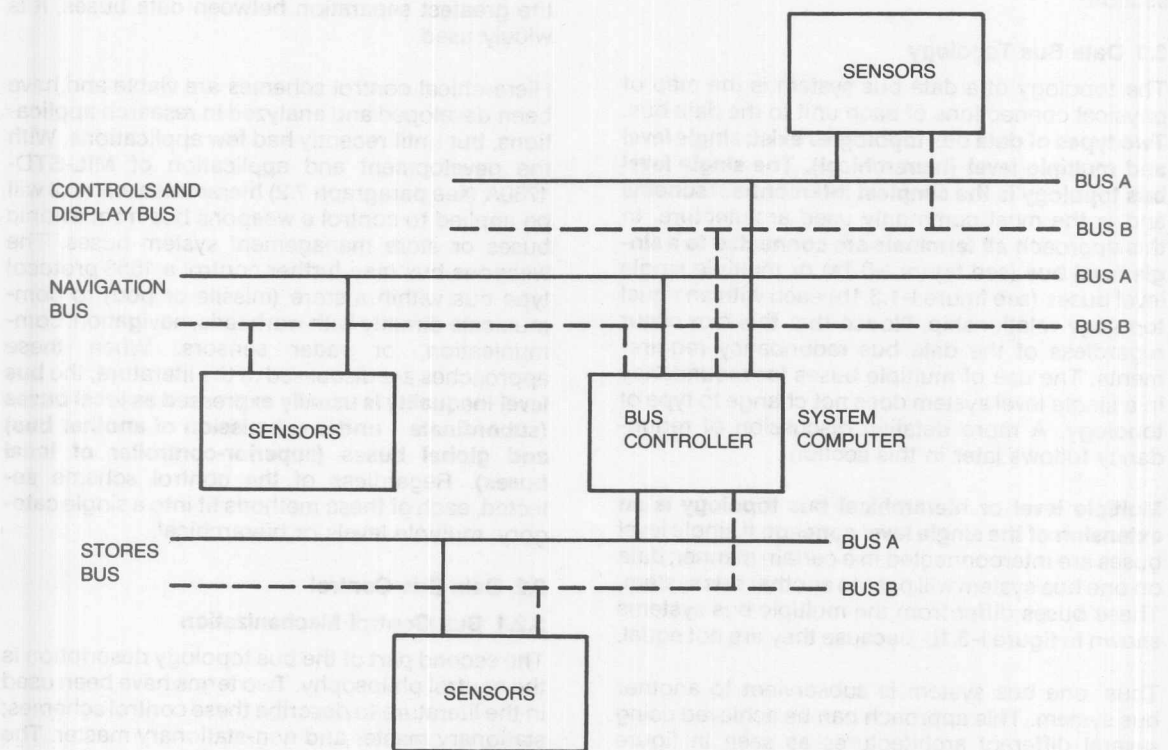


Figure I-3.1b Multiple Single Level Bus Topology



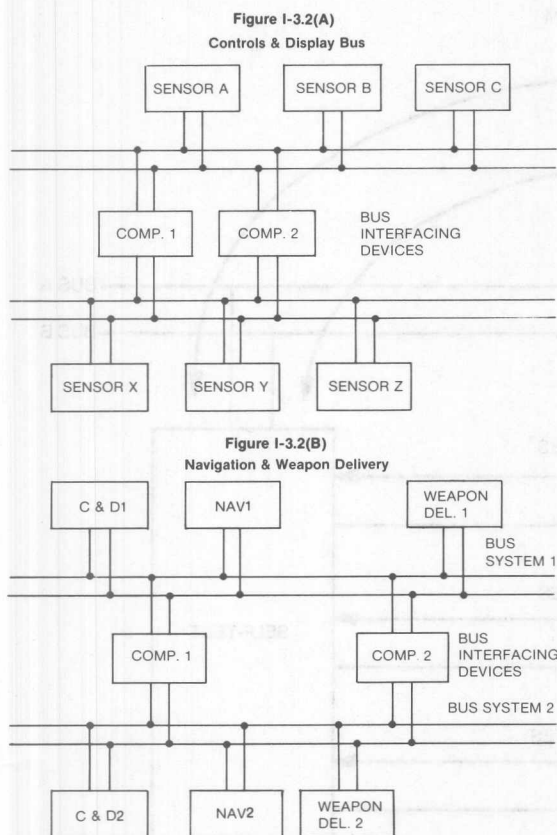


Figure I-3.2 Multiple Level Bus Topology

usually involves several actions involving the data bus, external wiring between the two controllers, and internal self test in both controllers (see figure I-3.3). The use of data bus messages to keep both controllers aware of the others status and health are usually required. Data bus synchronization using clocks or synchronize mode codes also provide the two controllers with usable switchover data. Internal self test software is responsible for identifying faults and removing the faulty unit from operation. Giving power control to the other processor (BC) with proper time delays also resolves conflicts in who should be in control upon initialization. Dedicated discretes with hardware watchdog timers provides yet another measure of switchover monitoring. All or most of these approaches are used today to achieve switchover. The development of a safe and secure method to switch to the backup bus controller is an essential

part of any stationary master control philosophy. When this bus control approach is applied to a single level bus system topology, a single bus controller will be used with a backup bus controller, as necessary. However, in a multiple level topology, stationary master bus controllers are located on each data bus system with a backup controller for each bus as necessary.

An alternative to a stationary master bus control system is a non-stationary master bus control philosophy. In this scheme, multiple bus controllers can control the single data bus system. Therefore, even in a single level topology several bus controllers can exist. Obviously, to allow all of the controllers the capability to control a single system, a method of passing control from one controller to another is essential, because 1553B allows only one controller to be in control at a time. MIL-STD-1553B uses the dynamic bus control mode code to accomplish this task. As discussed in section 1.4.2, the MIL-STD-1553B protocol provides a method for issuing a bus controller offer, thus allowing a potential bus controller to accept or reject control via a bit in the returning status word. The key to non-stationary master operation is to establish the number of controllers required by the application and when to pass control. As in the stationary master system, once control is transferred the operation is identical.

Two methods have been used; time based (producing a system similar to TDMA) and round robin (producing a system with a preordered list of bus controller). More complex schemes have been discussed where dynamically the existing controller polls (using conventional messages) to establish a priority of control and then passes the control to the controller with the greatest need. However, most of these approaches are very complex and require extensive error monitoring to provide confidence that the system as a whole is operational (only a single controller is in operation — no more or no less).

The round robin control mechanization utilizes a fixed order of bus control. This is usually accomplished by assignment of incrementing or decrementing addresses to all potential controllers. Since a potential controller is a remote terminal, when it is not in the controller mode, it responds to its remote terminal address, when the dynamic bus control mode code offer is provided. In these type of designs, the potential bus controller must accept the offer to become the next bus controller.

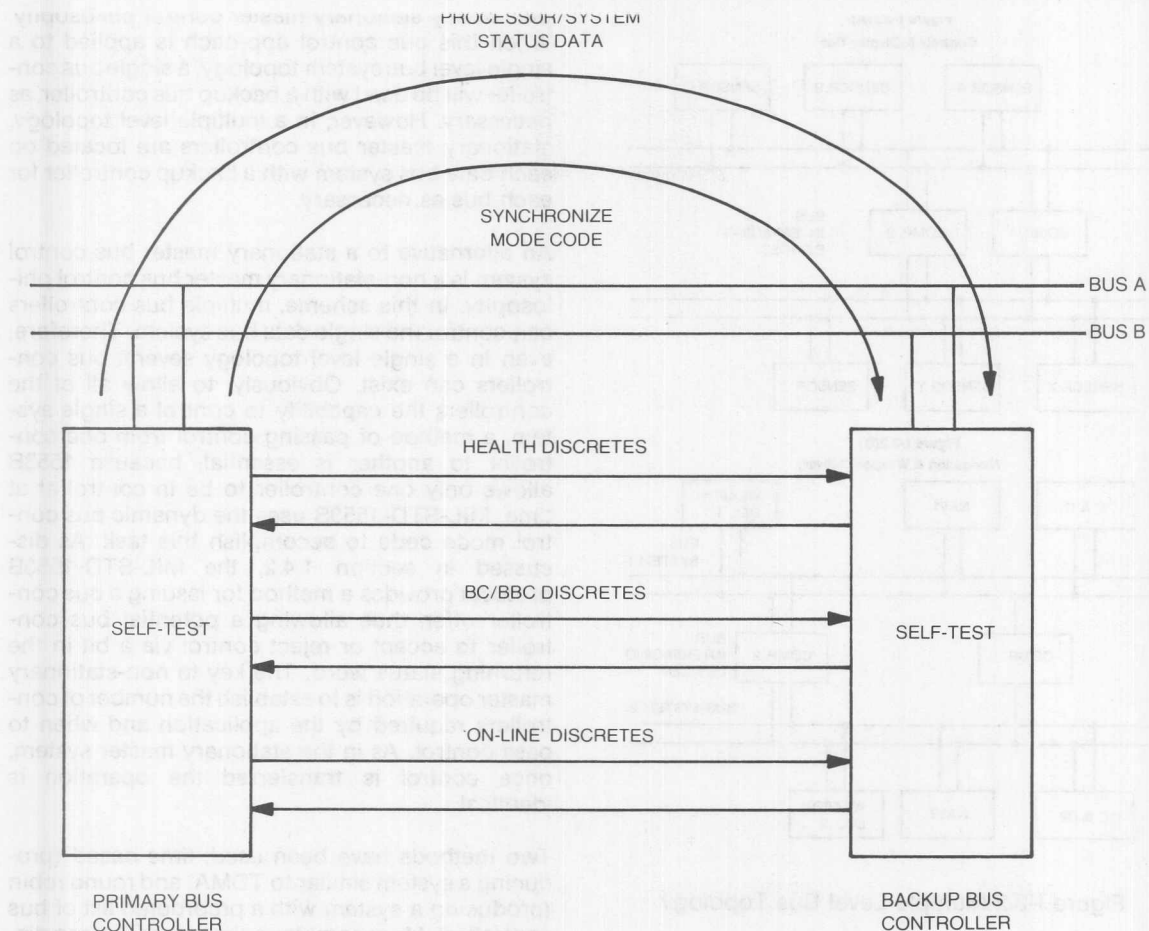


Figure I-3.3 Bus Controller Handshaking

If the new controller has no messages to transmit, it offers control to the next potential controller. Failures of potential controllers are managed by the active controller in one of two ways; automatically going to the next potential controller (requires extra knowledge on how to accomplish this task) or by appealing to a backup controller whose job it is to resolve system problems and relate the results back to all controllers. This provides each controller with the knowledge needed to pass control. Obviously, there are always design trades between increasing intelligence in each potential controller or using a backup (single point failure) source to resolve the system configuration. This same problem also occurs at system startup. It is because of these complexities, that this type of system has had limited acceptance.

However, with the growing use of multiple buses and the need to achieve data exchange between bus systems, this approach is being considered more and more often. Once again MIL-STD-1760A and other applications of multiple bus layers will yield a high degree of intelligence at the global bus level and thus a desire to maintain independence. All these affects will increase the interest of the system designer toward non-stationary master systems at global levels. This approach also has some unique system problems that must be resolved. Since each potential controller controls the bus each update period (maximum update rate of data transmitted in the system) and each controller has different message transmission requirements, bus usage times will differ. This difference will occur between controllers and between

update for a single controller (see figure I-3.4). This shifting of transmission times makes synchronous updates difficult. Any system using this method to achieve integration must be analyzed to determine if it can accept these asynchronous data transfers without time tagging data or paying a heavy penalty in bus usage (efficiency).

The time based mechanization allocates a fixed time for each potential controller to control the data bus. Once the maximum update is known then the period of time between updates can be allocated to individual controllers. The simplest approach is to divide the time equally. However, this may not have any bearing on the controllers need to transmit data during the update period. This is where the system designer must trade controller complexity (different time bases for each potential controller) versus message update needs

and message partitioning between controllers. This method allows the system to achieve synchronous operation at the cost of bus system efficiency if equal or fixed times are maintained. Bus efficiency is thus lowered by allocating fixed times to each potential controller. Obviously, during certain periods the controller will be in control and will have very few requirements (e.g. transmit or receive). Therefore, unused, unrecoverable bus time produces poor efficiency.

### 3.2.2 Error Management

Another aspect of data bus control mechanization is error management. Regardless of approach, an error management approach is required. Two types of failure condition exist; data bus system problems; and subsystem or sensor problems. The method used to identify, determine the cause, and

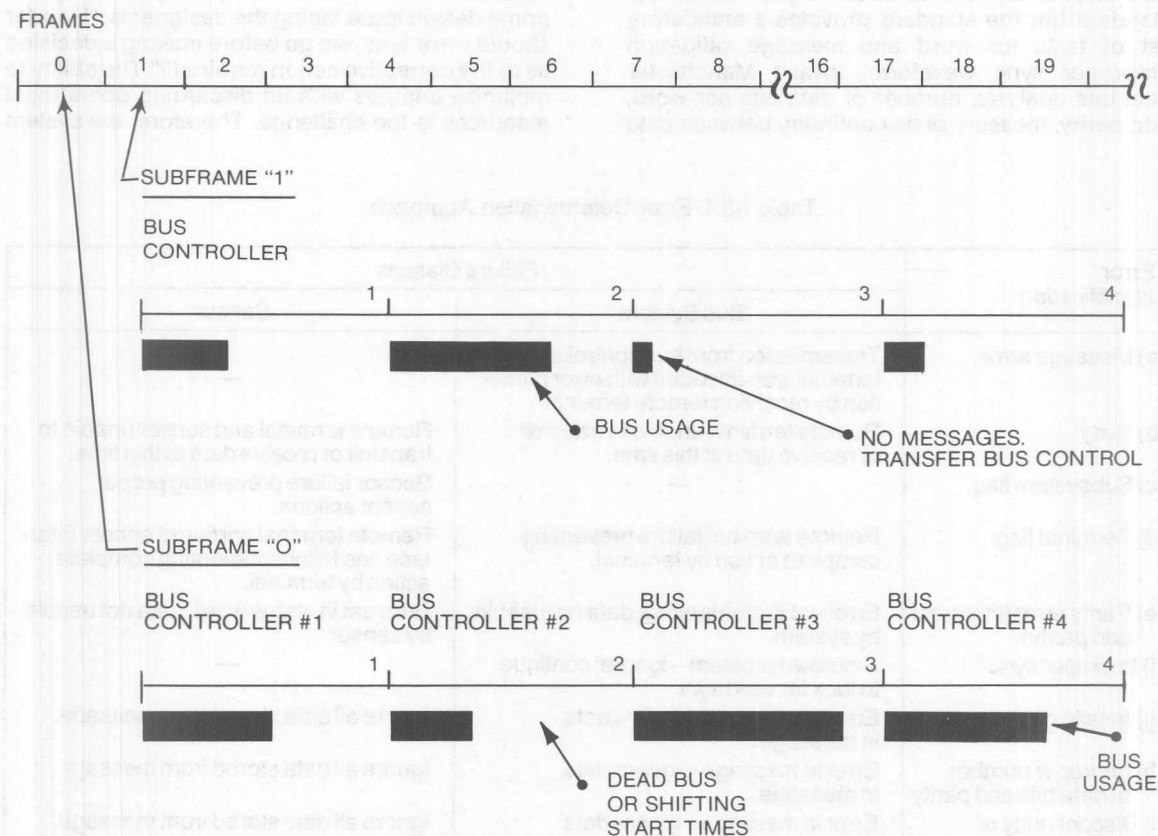


Figure I-3.4 Bus Traffic versus Bus Controllers on a Time Basis

achieve corrective actions are all part of the multi-plex system control requirements.

The data bus system can provide a communication medium to support error analysis associated with failure of sensor(s). Since sensors are quite different, the only capability the data bus system has is to convey the results of sensor built-in-test results or identify a non-communicating sensor. However, the data bus system is totally responsible for managing its own errors, including message failures and core element failures (i.e., bus controller and standalone remote terminals).

The 1553B standard requires correct word and message completion (1553B paragraph 4.4.1.2). These tests plus system level checking allow 1553 core element failure analysis. Some examples of test results and correction techniques are provided in tables I-3.1 and I-3.2. No requirement as to how error analysis is to occur is provided in the standard but the standard provides a mandatory set of tests for word and message validation (improper sync waveform, invalid Manchester data bits analysis, number of data bits per word, odd parity, measure of discontinuity between data

words within a message, and no response by remote terminal to a message error) and an optional set of remote terminal status bits (service request, broadcast command receive, busy, subsystem flag, dynamic bus control acceptance, and terminal flag) to manage the data bus system. The action to be taken depends on the error identification and the error correction desired. All these decisions remain with the system designer. Error identification is the responsibility of all terminals connected to the data bus, while error determinations and correction are the responsibility of the bus controller based on the systems designer approach.

It is the systems designer's responsibility to establish the systems response to each and every error identified by remote terminals or the bus controller. The error handling and recovery approach selected should be general in order to minimize hardware and software complexity. Usually the prime design issue facing the designer is: "How far should error analysis go before making a decision as to the corrective action required?" The ability to minimize analysis without discarding operational resources is the challenge. Therefore, the system

Table I-3.1 Error-Determination Approach

Error Identification	Failure Classes	
	Bus System	Sensor
a) Message error	Transmission from bus controller to terminal was decoded with error condition by receiving remote terminal.	—
b) Busy	Remote terminal unable to transmit or receive data at this time.	Remote terminal and sensor unable to transmit or receive data at this time.
c) Subsystem flag	—	Sensor failure preventing proper sensor actions.
d) Terminal flag	Remote terminal failure preventing complete action by terminal.	Remote terminal portion of sensor interface has failure preventing complete action by terminal.
e) Parity error (incorrect odd parity)	Error set in status word; data not usable by system.	Error set in status word; data not usable by sensor.
f) Improper sync	Unknown problem — ignore; continue to look for valid sync.	—
g) Invalid manchester	Error in message — ignore data in message.	Ignore all data stored from message.
h) Improper number of data bits and parity	Error in message — ignore data in message.	Ignore all data stored from message.
i) Discontinuity of data words	Error in message — ignore data in message.	Ignore all data stored from message.
j) No status word response	Unknown problem — requires further investigation.	



Table I-3.2 Typical Error-Correction Techniques

Error Identification Types	Error Correction Technique
1. Bus system failures a) No status word response b) Message error c) Parity error d) Invalid manchester e) Improper number of data bits and parity f) Discontinuity of data words	Retry message on same/alternate bus n times. Transmit reset remote terminal mode code if retry fails.
g) Busy	Retry message on same bus after a fixed delay time.
h) Terminal flag	If necessary, transmit initiate self-test mode code. Transmit BIT mode code. Analyze failure and determine corrective action, which may involve the following mode code commands: Shut down transmitter (00100 or 10100) Inhibit terminal flag bit (00110) Transmit reset remote terminal mode code if retry fails.
i) Improper sync	Ignore and reset for valid sync.
j) Subsystem flag	Normal data communication messages (address/subaddress) to examine sensor BIT discretes or words.
2. Sensor failure a) Discretes b) BIT data word(s)	Analyze failure and determine system-oriented corrective action.

designer should establish these approaches prior to hardware and software definition. One method to convey these requirements to the hardware and software designer is the control procedure. Control procedures (see figure I-3.5) define the response to all normal and abnormal messages. In addition, control procedures establish how the system is to initialize, reconfigure, synchronize, shutdown, etc. To prepare this level of detail the system must establish the hardware and software partitioning and communicate the specific hardware design required to the hardware manufacturer and the software requirements to the software designer. This is usually accomplished with a detailed hardware specification and a software requirements document. The combination of control procedures and the actual hardware implementation yields sufficient data to develop software requirements. Then the software design accomplishes the system design approach.

The failure response to problems within the core elements of the data bus system include the data bus, the remote terminals, and the primary bus controller must be established prior to implemen-

tation. For the stationary master scheme, the failure of the bus controller causes a fail-safe transfer to the backup controller. This usually begins when the primary bus controller recognizes internal problems and ceases operation. The failure to notify the backup controller of operational capability on a regular basis and the lack of bus traffic alerts the backup controller to the fact that it should attempt to gain control. In addition, hardwired discretes between the primary and backup controller can be used to indicate "who's in control", the terminals health status (a discrete which toggles each frame), and if the terminal is "on-line" (capable of 1553 communication). The first signal is used during system startup to prevent collisions by the two controllers. Later, if the signal is removed by the primary controller, the backup then assumes control. The health indicator is used to verify that the two controllers are executing their software correctly. The command that toggles this line is usually performed after completing a portion of the background built-in-test. Failure to toggle this signal indicates a software problem and that control of the bus should be changed. The last signal ("on-line") is again used during system

A positive method of access control is essential. Figure I-3.3 shows a simple method. See paragraph 3.2.1 for a complete discussion of bus switchover for a stationary master system. Obviously, it is much more complicated with the non-stationary master control schemes. The problem is "who will transfer control to the next potential controller" when the controller presently in charge has failed. As discussed earlier a system monitor is usually required to resolve these and other abnormalities. The design of the monitor then becomes a trade between system autonomy and error analysis and correction.

**The failure of a remote terminal is usually detected by bits set in the status word or the lack of trans-**

investigated using the mode code transmit built-in-test word (BIT). There are no restrictions or definitions concerning the contents of the BIT word. However, the data should convey information which allows the bus controller to take corrective action. If internal redundancy exists within the remote terminal, the ability to use the operational portion of the terminal must be conveyed to the bus controller. Otherwise, the system must reconfigure to replace the failed device if such a system reconfiguration is possible. Since most remote terminals use 1553 chip sets, the designer of the chip set has already established the BIT word format. Some chips allow host (non-chip hardware) to download some health data, others do not. The hardware and system designers should establish what is acceptable for their particular system and select chips appropriately.

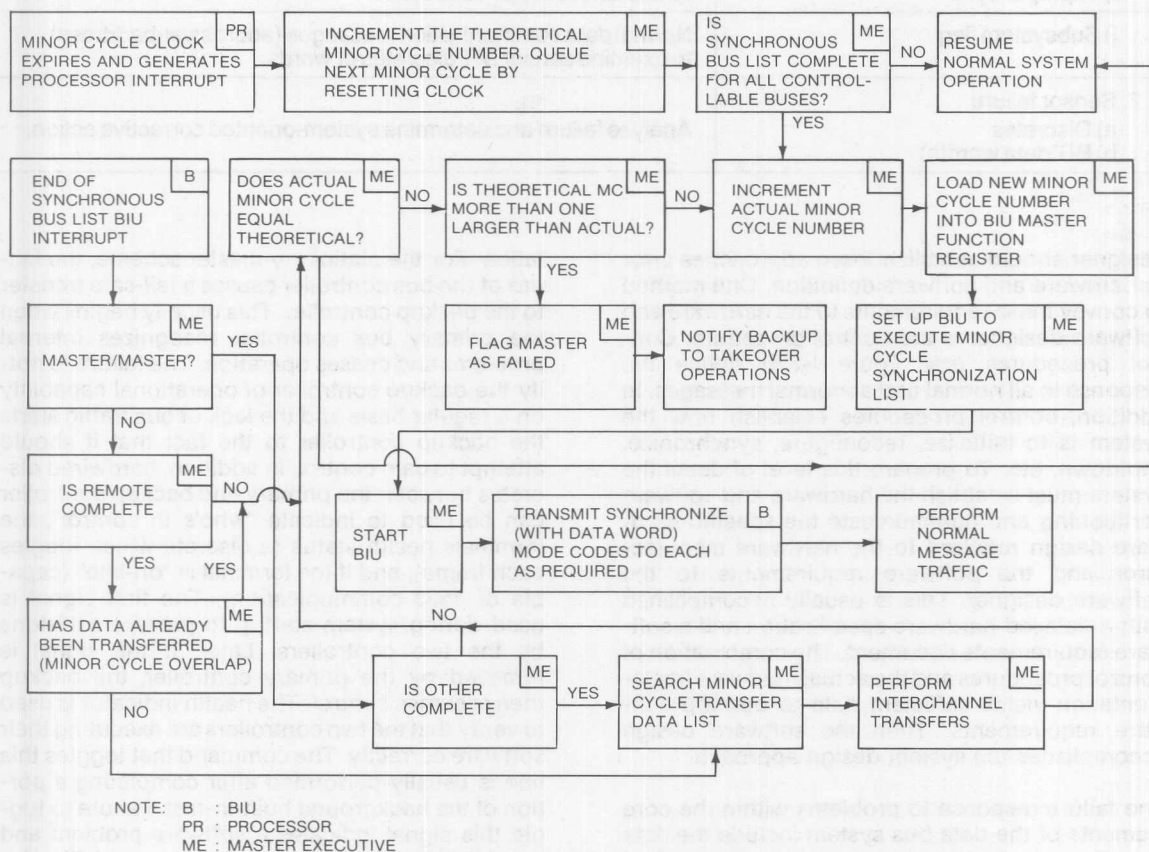


Figure I-3.5 Control Procedures

The other core element is the data bus system. **A data bus system failure is usually recognized by the lack of communication with terminal(s).** In dual or greater redundant data bus systems, alternate data buses can be used to re-establish communication.

### 3.3 Functional Partitioning and Data Bus Element Redundancy

To achieve the proper functional partitioning of a data bus system, requires the system integration knowledge and data bus system architecture experience. This type of integration must be viewed from an overall integrated approach rather than from a conglomeration of individual sensors, subsystems, controls and displays. The data bus system requires detail interface definitions and information flow to begin the orderly integration process. Since most of the integration is achieved using bus controller messages, identification of device to device communication begins the integration process. Before a topology or a control scheme is established a functional flow should be developed (see figure I-3.6). With functional flows, message definitions can begin.

It is at this time that the functional partitioning philosophy must be established if multiple bus systems are to be used. If a single level system is selected, the following discussion concerning partitioning is obviously not relevant. **For multiple bus topologies two philosophies are popular today; partitioning by function (control and display bus, navigation bus, weapon delivery bus) or partitioning by redundancy (separation of similar function — AHRS from INS). These philosophies should not be mixed in a single design.** It is the system designer's choice based on the application since neither philosophy has proven to be better than the other. System partitioning by function seems to be more prevalent today, because of the engineering organizational structure, laboratories, and the need for parallel development. Also the system engineers can best be used if they provide the guidelines and general requirements rather than be responsible for a closely integrated system. **This approach also allows loosely coupled subsystems.** The functional partitioning approach allows direct messages between similar functions (RT to RT) and an easy transfer method to redundant elements, since they exist on the same bus system. However, since all the redundant elements are on one bus system, total bus system failure must be considered. In a dual redundant system this would require a dual failure, which is a remote possibility for mission oriented applications.

Using the redundancy philosophy, similar devices are separated from each other and placed on multiple bus systems. This provides greater autonomy and failure protection. It also creates more traffic between bus systems, if the redundant elements share data or check each other. This method then requires greater time for messages to pass from one bus system to the other and an efficient data passing mechanism is essential for multiple bus systems. Regardless of the method chosen, partitioning begins with functional interconnections leading to message definition. At this point, the selection of the bus controller scheme can be made. **The type of control (stationary or non-stationary) and the level of redundancy of the data bus and bus controller should be established. Generally, redundant bus controllers (active and backup) are used in stationary master systems.** Most non-stationary master systems do not provide redundant controllers because of the extensive use of controllers already. In the event of loss of an important or critical function, the monitor bus controller in a non-stationary master system can assume a limited set of these functions providing a degree of redundancy. **Data bus redundancy is usually dual. MIL-STD-1553B paragraph 4.6.3 states that if dual redundancy is used, the system must operate in an active/standby mode.** However, the system is not restricted to dual redundancy and it can operate at any level of redundancy required to meet system requirements. If a dual redundant system is selected, the active/standby mode can be implemented in at least two ways; individual devices use either bus for communication (selection established by communication of

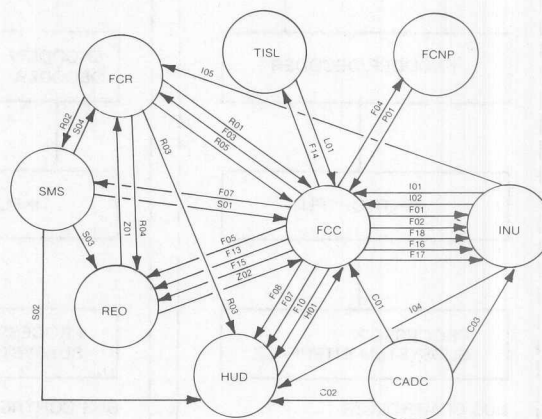


Figure I-3.6 Multiplex Data Bus Functional Block Diagram (Primary Mode)

the bus controller to the remote terminal) or block switch (all devices are communicated with over the same bus until a failure and then all are switched to the redundant bus). **The most common approach is the first one which allows the bus controller to communicate using either bus with any terminal.** Since this method allows the greatest flexibility it is used almost exclusively. This approach does require the bus controller hardware and software to have the capability to distinguish, on a message basis, which bus it is to use.

The block switch mode is a slightly simpler bus controller mechanization, since it is not message or terminal selective, but system selective. However, this method limits flexibility and has not found wide usage.

Remote terminal redundancy is obviously equivalent to data bus system redundancy in the 1553 interface area. The design issue associated with the remote terminal is the extent of redundancy occurring in the circuitry approaching the subsystem side of the interface. Figure I-3.7 describes the functional elements within a remote terminal and shows three different design approaches to redundancy. In the first approach, the analog section is

the only dual redundant section. **This approach is NOT compatible with MIL-STD-1553B dual redundant systems, because the command word validation must be established for each bus to meet the requirements of the standard.** This is accomplished in the second and third approach. The third approach uses completely independent interfaces to the subsystem, while the second approach duplicates only the minimum circuitry necessary to meet the standard. Another design is being used for remote terminals only, which includes two decoders and a single encoder. This method allows a terminal to receive on two buses while using only a single transmitter. This is an acceptable approach, but it has not received wide usage. This will change as more monolithic solutions evolve.

The advantages of the second approach are minimum hardware and good input/output flexibility, while the advantage of the third approach is isolation between channels. **Most interfaces for both remote terminals and bus controllers are built using the second approach.** This approach allows a bus controller to switch buses for retries without additional I/O support, a capability not available in the third approach. The third approach is used in systems requiring greater hardware isolation

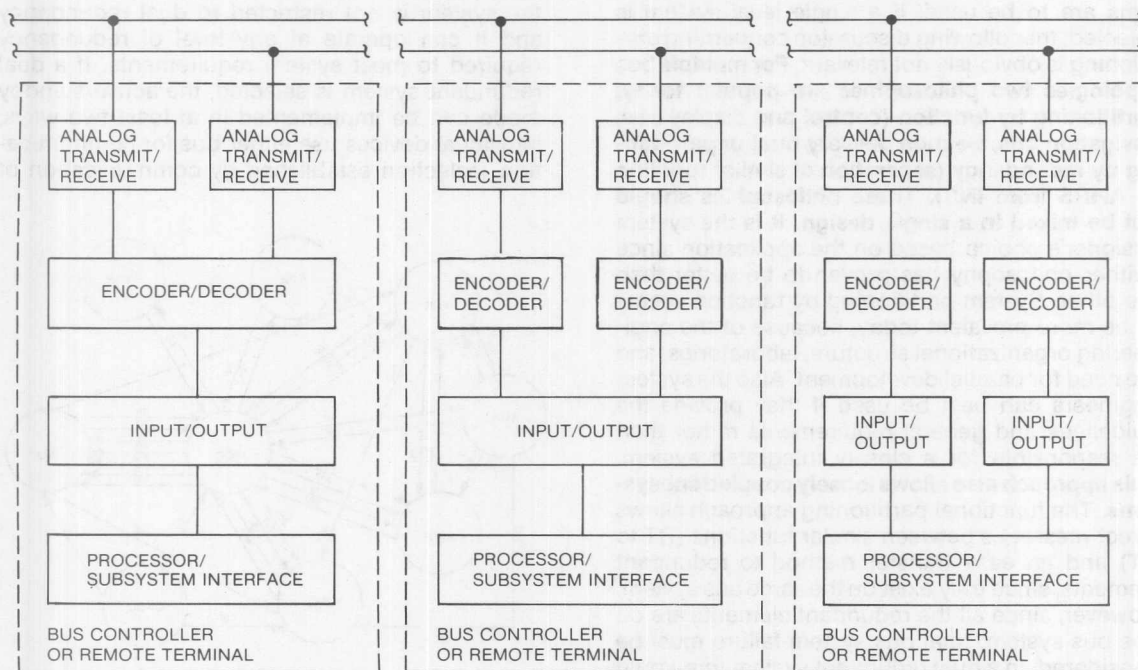


Figure I-3.7 Terminal Bus Interface Redundancy



between the buses (not high control). Care should be taken in using the third approach for active/standby system. The channelization could prevent proper operation of mode codes like transmit last command. If this mode code is received in an active/standby bus system, it must report the last command regardless of which bus it was received on (Single channel chipsets employed in a dual redundant design will not meet this requirement without the addition of external circuitry).

### 3.4 Data and Control Passing in Hierarchical Networks

With the advent of multiple hierarchical networks, it became necessary to pass data from one network to another. At first this was accomplished using the bus controller processor. The B52 Offensive Avionics System shown in figure I-3.8 is an example of early architectures which used the mission computer as the gate between networks. Note that for definition purposes, a GATE (also referred to as a GATEWAY) is used to pass data between similar buses (i.e. a 1553B data bus to a 1760A weapons bus) both based on 1553B; whereas a BRIDGE is used to pass data between dissimilar buses (i.e. a 1553 data bus and a high speed type of bus). In the B-52 example, the control and display bus was connected to the navigation and weapons delivery bus network using two mission computers.

Notice from the figure that one bus network is controlled by the mission computer acting as the primary bus controller while the other mission computer acts as a remote terminal and the backup bus controller. For the other bus network, the roles of the two mission computers are reversed. Data collected in the navigation and weapons delivery system is made available to the control and display network via the remote terminal side of the mission computer. Therefore, the most general example of 1553 gates are single units acting as bus controllers on one network and remote terminals on the other network. However, two other approaches are possible: remote terminals on both networks and bus controllers on both networks. Figure I-3.9 shows each configuration. The least likely architecture is both remote terminals (configuration II). This configuration will be discussed briefly because of its drawbacks. The remote terminals in this configuration receive data asynchronously on each bus network, thus requiring extensive data buffering or inter-bus network synchronization to prevent data contamination. This configuration requires data protection to pre-

vent data reception on one bus network while at the same time the same data is being transmitted on the other bus network. There are hardware and software methods of dealing with this problem, but it requires extra effort to operate smoothly.

The architecture of configuration III is most often seen in modern systems when a bus controller-/processor controls multiple data bus networks in a synchronous fashion. Since control resides within a common computer, synchronization and data mapping control from one network to another is quite easy to accomplish. The most popular method is to operate all bus networks synchronously and globally map data in and out of large memory areas using message pointer tables (see paragraph 3.7.1 on subaddressing) that directs the data arriving from one bus network into a common area which is accessible by the other network for transmission. This reduces or eliminates the internal data movement required to pass messages from one network to the other. In this configuration, navigation data can be passed to stores management networks without the computer moving the data internally. Another primary reason to synchronize the control of the two networks from a single unit is to reduce the data latency time between networks. Since control of both networks resides in one computer, the knowledge of when time critical data has arrived and is available for transmission to other users is always present.

The category I configuration is the most commonly used for a gate in today's architectures because it supports a global network feeding the local networks or visa versa. Today's hierarchical bus network structures are composed of two types of local networks: data source networks and data sink networks. This can best be explained by examining a few examples. If a navigation local bus existed in a hierarchical architecture, its primary function would be to provide source data to other networks. In other words, most of the data generated would have destinations outside the local network. Contrast this with a control and display network. Its function is to sink data from many other networks. Only man-machine control data is likely to be transmitted outside of this local network. As you can tell from the example, no network is completely unidirectional, but data bus traffic will predominate in one direction or the other. Local networks, like these, tend to be remote terminals on global buses in large architectural systems and bus controllers on their local networks.

As a rule of thumb, it is always better to be a bus controller if the unit is a source of data and a

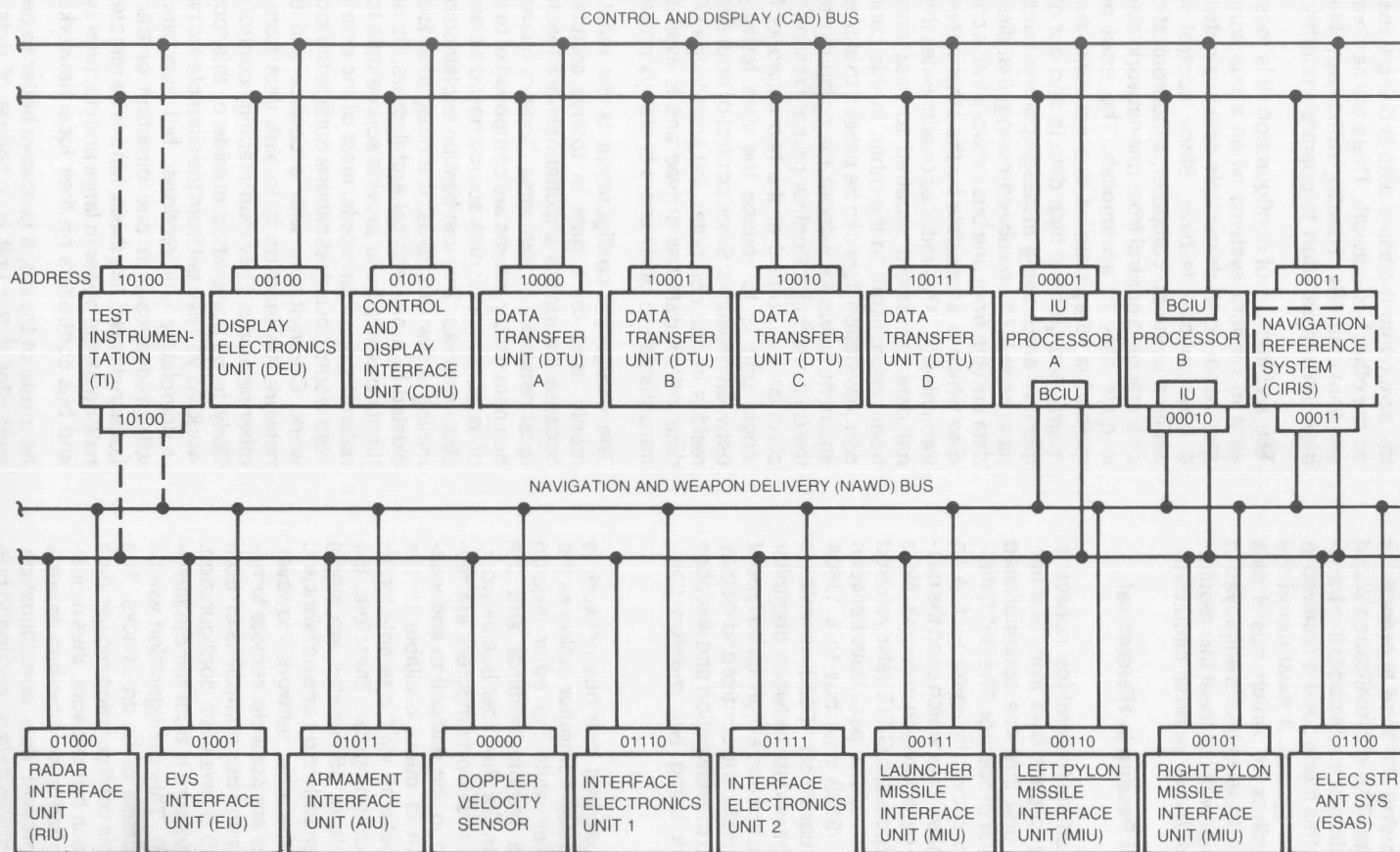


Figure I-3.8 B-52 OAS

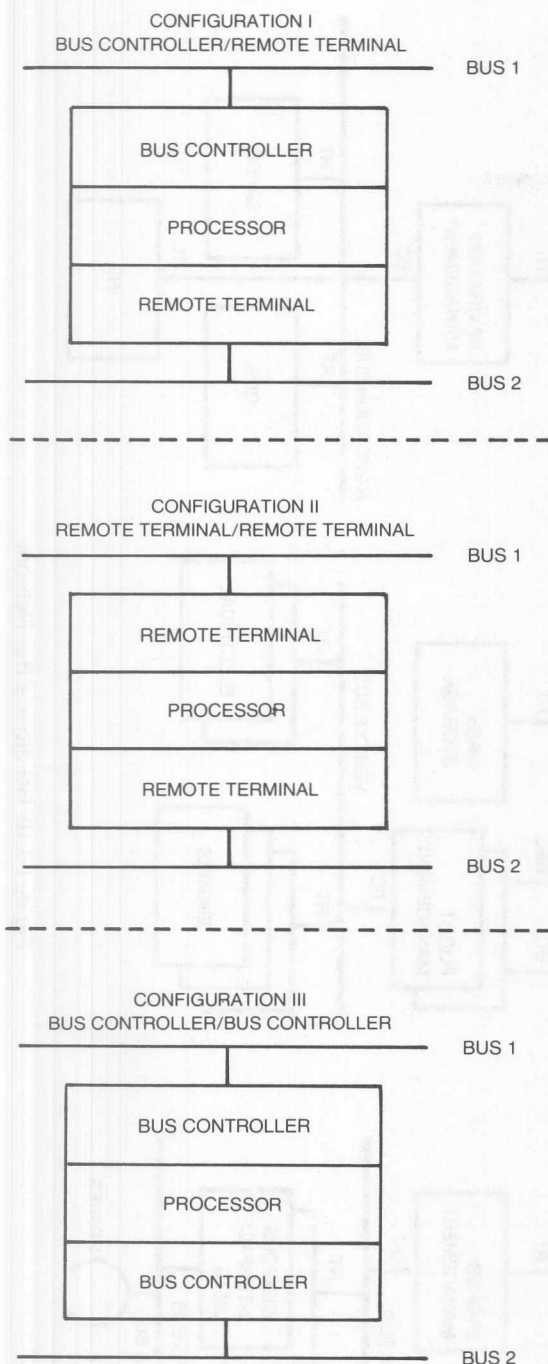


Figure I-3.9 MIL-STD 1553 Gate Configurations

remote terminal if it is a sink of data. Obviously, the benefit of bus control is it allows the subsystems timing control thus providing source data freshness. The counter is also true, if the network is sink oriented, the role of a remote terminal is more than satisfactory. However, often these simple rules are not always practical in the architecture selected. Notice in the example of figure I-3.10. In this example, a mission computer is used to perform control of multiple global buses acting as a configuration III gate, while local buses (both sources and sinks) are configured as configuration II gates. Thus the design of a configuration II gate must be capable of data transfers in either direction. Generally, the data will have a definite direction, primarily in or out of the network, not both.

In the examples discussed so far, a large mission computer was used with its powerful, often processor based input/output section, to perform the functions of a configuration II or III gate. These units built by traditional airborne computer manufacturers often have very capable input/output circuits which can perform either the role of bus controller or remote terminal. However, with the application of MIL-STD-1760A (see paragraph 7.2 for a discussion of the standard) in airborne 1553B networks, the need has developed for simple configuration II gates as shown in the weapons bus of figure I-3.10. The generic weapon interface unit is one of several units connected to the stores bus network as a remote terminal and to the weapons bus network as a bus controller. Many other simple hierarchical architectures may choose the same approach as opposed to complex mission computers. Therefore, a need has developed for a simple, almost hardware intensive, configuration II gate. The function of this device, (see figure I-3.9) is to receive and transmit 1553 data as a remote terminal on a higher level bus and transmit and receive 1553 data on a lower level bus as a bus controller. The features of this gate can vary from a unit as powerful as any gate built within a mission computer to a gate that can only carry out one message at a time from the higher level bus controller. With these extremes in mind and with the type of data flow that will be seen on the lower level bus (periodic or aperiodic), two basic design concepts have evolved in industry: transaction table controllers and peeling controllers. Each of these units will be described along with some of the reasons for determination of which is best for a given application.

The transaction table gate takes its name from the method it uses to perform the bus controller function. Transaction tables are lists of instructions

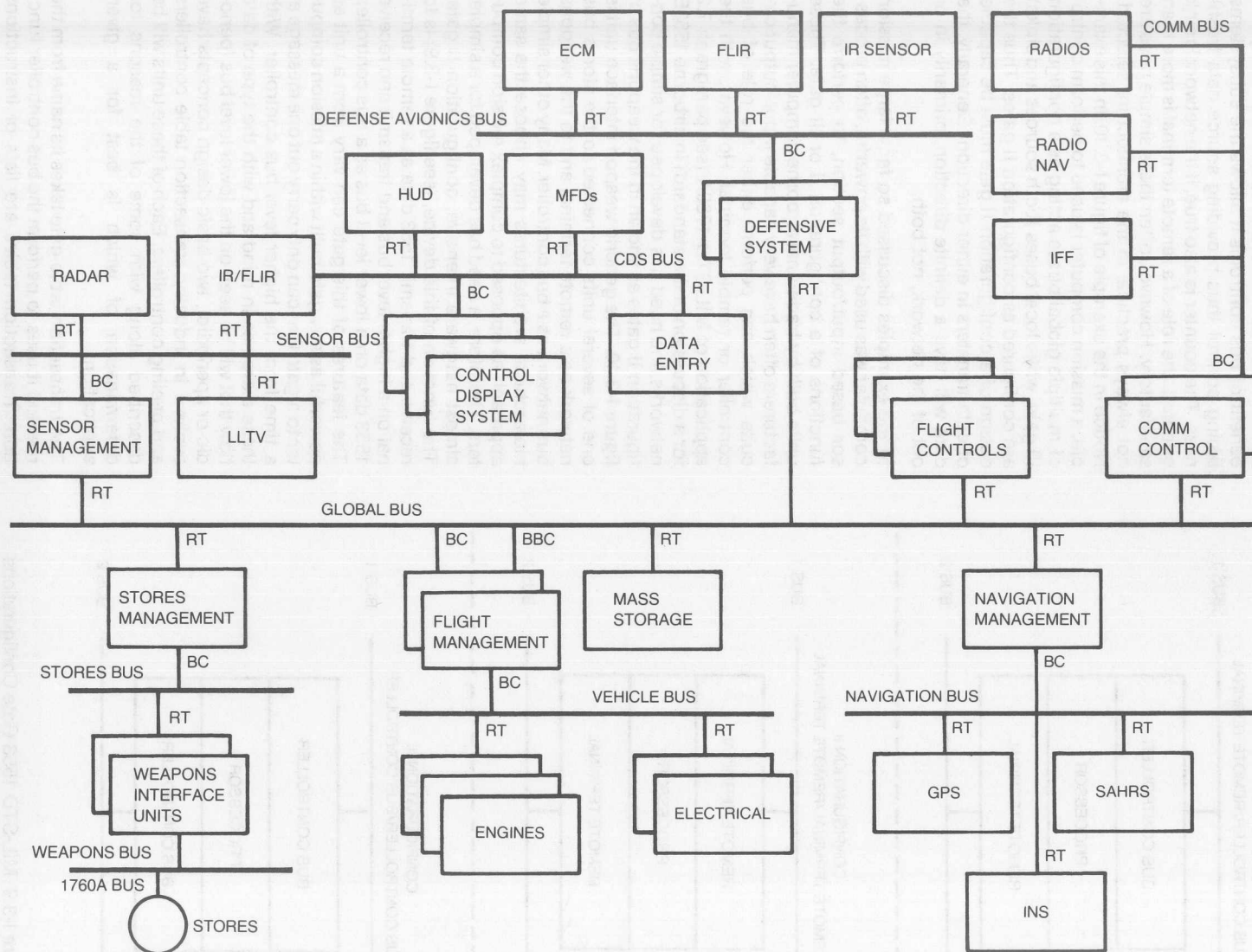


Figure I-3.10 Heirarchical Bus Network



which are downloaded into the gate to direct the hardware to perform typical bus controller functions: transmit messages, receive messages, use mode code commands, skip messages (no-ops), jump from one list of messages to another, start, stop, use bus A or bus B, retry, interrupt on message transmission or reception, etc. All the features of a normal bus controller are built as instructions to the hardware. These called Channel Control Words (CCW) (see paragraph 5.1.1 for basic discussion on bus control and table I-5.1). Since each set of CCWs describes a single message, multiple sets of CCWs linked together form a minor cycle (see figure I-5.1). Since the flexibility exists to string messages together, periodic message strings can be built. Also error handling and recovery techniques are available using a fixed error handling message string. Generally, if a status word is not received or if received with errors, the limited computing capacity in this level of a gate requires error analysis and recovery to be accomplished in the higher level bus controller and passed back to the gate as a new set of CCWs or a change of the existing CCW string (e.g. no-ops messages to a failed unit). The ability to dynamically download changes to the CCW or new CCW strings is also needed to support aperiodic and time critical messages through the gate to the subsystems at the lower level. Because of its construction of tables, this type of gate performs very effectively when periodic traffic predominates the lower level bus network. To support time critical messages, they must be prepositioned or the bus controllers internal message position (instruction address pointer) must be available to the upper level bus controller in order to link in the time critical message. This is an overhead intensive function and should occur on as few occasions as possible. However, it is a very usable controller method and can be performed in a timely manner. All system timing should be met with this approach because it fundamentally is no slower, and often times faster, than the upper level bus controller which initiated the traffic. Time critical messages, such as clock updates and weapons release, can also be performed using transaction table gates supported by a 1553 bus controller on the higher bus network. As can be seen with the use of transaction tables for multiple CCW downloads, aperiodic communications links, normal data traffic, and error recovery procedures, considerable subaddress expansion will be required by the remote terminal (see paragraph 3.7.1.1 for a discussion on expanded subaddressing). Also the local bus performance and data exchange between networks will work smoother if the higher

level and lower level buses are synchronized. Synchronization of the two buses is achievable using 1553B synchronize mode code with the data word command described in paragraph 3.6.

The second method used to meet the configuration II gate is known as peeling. The name is derived from the procedure used to generate instructions to the gate. Each message passed, from the bus controller on the higher level bus, to the gate contains up to two words at the start of the data message which are peeled off the message (not part of the message data content) as instructions to be used by the gate in the processing of the message. Usually, the first word contains mode information (e.g. message type BC-RT, RT-BC, usually not capable of an RT-RT transfer), bus to be used (A or B), retry options, etc.). The second word is the complete command word for the lower level bus. The remaining words of the message constitute the data words of the message (maximum of 30 data words). Note that MIL-STD-1760A (see paragraph 7.2) limits weapons bus messages to 30 words in order to support this gate technique. This approach works well for aperiodic and time critical messages because the message itself contains the data that is to be passed to the lower level bus. The peeling technique is much less effective when trying to get the lower bus to source (transmit) data to the higher bus levels. In order to get data from the lower level to the higher level network, a two word message is transmitted to the gate which becomes the transmit command on the lower bus. At some later time, the higher level bus controller will transmit a new message to the remote terminal (gate) to collect this data. This two step process is somewhat difficult for aperiodic messages, but extremely time consuming for periodic traffic. Figure I-3.11 shows the protocol sequence required to support this technique.

### 3.5 Network Startup and Shutdown

The system designer develops the operational capability of the 1553 network by establishing the options within 1553 which the particular system requires. Then the designer establishes the message mapping requirements and their update rates. Since 1553 was designed to perform primarily with periodic message traffic, each periodic message will have a source, destination, update rate, and periodic position in selected minor frames. However, the reality of 1553 systems is that they must be started and stopped. Since the system usually operates in the periodic too little attention is directed at starting and stopping of the system. Why should this be a problem? In most



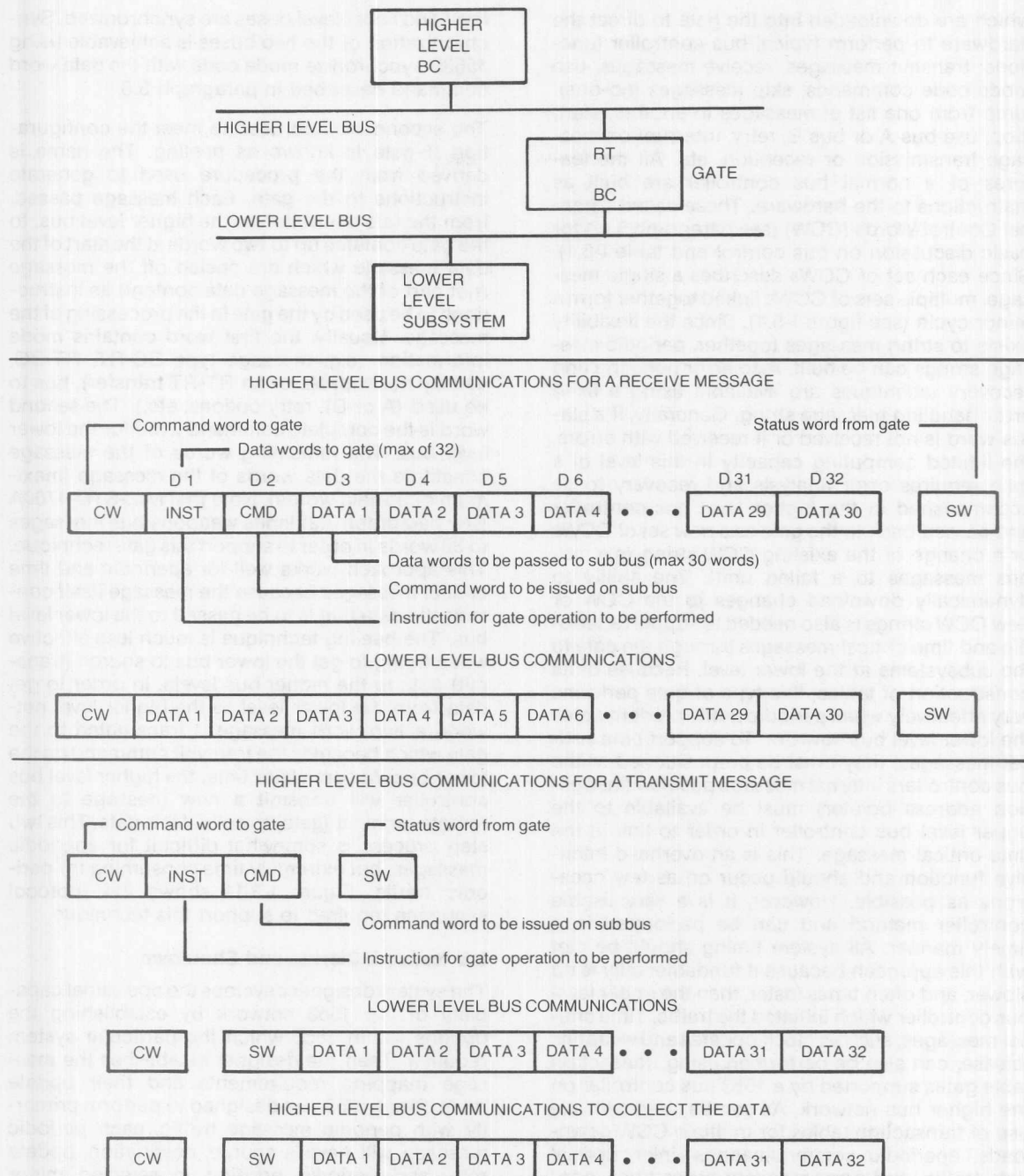


Figure I-3.11 Protocol to Support Peeling Gates

applications power is applied to a few elements, which initialize and then startup others or all units are powered on when their power bus receives power. Asynchronously electrical bus power initialization yields subsystems in various stages of initialization. The problem is identical in shutdown. The error monitoring and control logic of the bus controller utilizes the fact that a terminal is not communicating as a sure sign of trouble. Previous designs have been known to attempt communications with a terminal which was either not powered or had not completed its internal self test and placed itself "on-line". Having failed communications attempts, the bus controller terminal "dead", removed its messages from the periodic lists, and reported the failure to the maintenance program. Therefore, this logic must recognize startups and shutdowns as conditions where periodic messages may not occur due to the subsystem being powered off. Obviously at some point in any 1553 network, periodic communication can not exist successfully because too many messages in the system are missing. The system designer needs to establish the minimum message list necessary to continue to operate a particular periodic network. When a 1553 network is not operating in a periodic fashion, only minimal activity is possible. Aperiodic operations can be used by the bus controller to establish the primary bus controller and to initialize various 1553 subsystems. Initialization usually consists of the following:

- a) initial communication with subsystems to determine their powered on state and health. Usually a unique subaddress which provides subsystem health data is chosen.
- b) some subsystems require extensive initialization including program loads, system parameters, unique subsystem constants, time, etc. These messages are handled aperiodically with the subsystem prior to initiating periodic traffic.
- c) system synchronization (see paragraph 3.6 on synchronization of terminals).

Once a sufficient number of subsystems exist (have been initialized and are "on-line") within the network to begin minimal operation, the bus controller can begin periodic message (minimal list) communications. After periodic communication begins on a network basis, all non-communicating terminals will be dealt with by error handling and recovery logic which usually reports to application software that these subsystems are non-operational and presumed failed. Therefore, entering periodic processing too soon can cause false error

reporting. If the bus controller later conducts a poll of all possible subsystems, late powered devices can be initialized and brought into the network, often upgrading the system to a more capable mode. Prior to periodic communication with these new devices, extensive aperiodic communication may be necessary. This could even be larger than normal startup time, if the subsystem requires knowledge of the present state of the network.

Another important case which needs to be considered is the initial checking and monitoring between the primary and the backup controllers. If one of the methods in which the backup controller determines it should takeover control of the bus is detection of bus dead time (a period of inactivity on either bus usually on the order of several minor frames), then the startup sequence has all the ingredients for a bus collision between the two controllers. To prevent this from occurring, one of two things must be done: a) always power up the primary controller first such that it will have completed its internal tests and will communicate on the bus first, or b) program a software time delay into the backup controller's bus control program such that it will wait a "reasonable" amount of time after it completes its internal self test before attempting to take control of the bus.

Generally, error handling and recovery software deals with startup and shutdown in a different manner than normal operation, due to the apparent error conditions that exist because of asynchronous power control and subsystem warmup. If power control of the network is available within the processor acting as the bus controller, system startup can be a much more coordinated operation. The same is true for shutdown. If this is the case, usually the bus controller is the first system on-line and the last system off-line. This is often very important in military systems which can contain classified data. Often the bus controller executive/application software is responsible for commanding classified data erasure in other subsystems and finally within itself prior to power removal. If the bus controller is not responsible for power control, the startup length will depend on how long it takes the system to reach a minimum capability.

### 3.6 System Synchronization and Protocol

1553 systems are synchronized to allow an orderly processing approach to data arrival and departure. Most systems process data at fixed update rates (i.e. mostly binary rates, however some decimal based systems do exist), where on one cycle input

data messages are received and on the next one or more cycles the processing of that data occurs, and on a future cycle data transmitted. Thus, synchronous operation must be timed to achieve the input, process, and output procedures. If the software in the terminal is to process the data during a certain interval, a flag is required to identify when all the required data has arrived and processing can begin. Most 1553 systems use a synchronize signal to announce (flag) this occurrence. The synchronize signal can be the synchronize with or without data word mode code [00001 or 10001]. If the synchronize without data word mode code is used, only a time "tick" is announced not a specific frame number. Therefore, generally the synchronize with data word mode code is used to convey the event. The smallest increments of time (highest periodic data rate) is usually called a minor cycle or minor frame. Minor cycles are most often initiated by a system timer within the bus controller that interrupts the bus control software and declares "it's time to start a new frame." When this occurs, the bus controller usually completes the message in process and then decides if all of the planned periodic transmissions have been communicated for the present cycle. If not, the minor cycle must be completed or terminated. Systems which fail to complete a particular minor cycle cause terminals to miss their periodic data update. Also if minor cycles continually exceed their allocated time, the system will "jitter" in its periodicity. Both of these problems can cause serious systems problems and solutions need to be built into the system to deal with them. A "rule of thumb" which has been used in several systems is to allow the minor frame to overflow (extend the minor cycle until completed) up to one full minor cycle. After this time, the bus controller should either go on to the next minor frame or relinquish control to the backup bus controller.

A given minor cycle can be described (see figure I-3.12) as the time the system requires to: a) synchronize appropriate remote terminals, b) transmit and receive all periodic communications scheduled for this time interval, c) transmit and receive any aperiodic request generated by the bus controller or remote terminals (via the service request bit in the status word and the transmit vector word mode code), d) transmit or receive background messages (multiple messages exceeding 32 data words occurring over a period of time, i.e. mass transfers and bulk data such as data bases or program loads) which do not require completion this frame, and e) bus controller polling of subsystem status and health messages. Items d) and e) will

occur only on a "time available basis." Notice that the 1553 synchronize with data word mode code example provides a method of synchronizing remote terminals using minor cycle numbers. It also provides a method of updating an internal real time clock with a resolution of 15 bits. Using the data bus to transfer system time can be done if exact time is not required. Resolutions under 100 microseconds are achievable if special hardware is provided in the terminal to store the arrival of the data word and read and save the internal reading of the terminal's clock. With both the received clock word and the internal clock value upon reception, software can reset the clock by the offset or ignore the difference due to the small error that exist. As can be seen in the example data word, (figure I-3.12) a method to achieve subaddress mapping commands is provided (see paragraph 3.7.1 for subaddress mapping discussion). By setting or resetting the time, update minor cycle, and update subaddress mapping bits, the data word can convey up to several encoded actions for a terminal with a single mode code transmission. An example of the events that would occur during a typical minor cycle using the features described above for the synchronize with data word mode code are as follows:

- a) bus controller's real time internal clock interrupts its software indicating that it's "time to start a new minor cycle".
- b) the bus controller software determines that all mandatory messages are completed from the previous minor cycle.
- c) the bus controller transmits a synchronize with data word mode code to N terminals requiring real time clock updates this frame (usually many frames can elapse between clock updates to a given terminal). This can be broadcasted, thus updating all terminals using only a single mode code message.
- d) the bus controller transmits synchronize with data word mode code to all terminals (discrete or broadcast) requiring synchronization. The data word is encoded to indicate minor cycle update, minor cycle number, subaddress mapping data, and the subaddress mapping number. Since the next traffic is periodic messages, the terminal can be designed to accept the same subaddress mapping number for a given minor frame (usually both encoded values are identical).
- e) the bus controller utilizes command words to perform all periodic communications required for this particular minor frame.
- f) if time critical messages must be introduced during the periodic traffic, a synchronize with data word mode code MIGHT be used to a specific

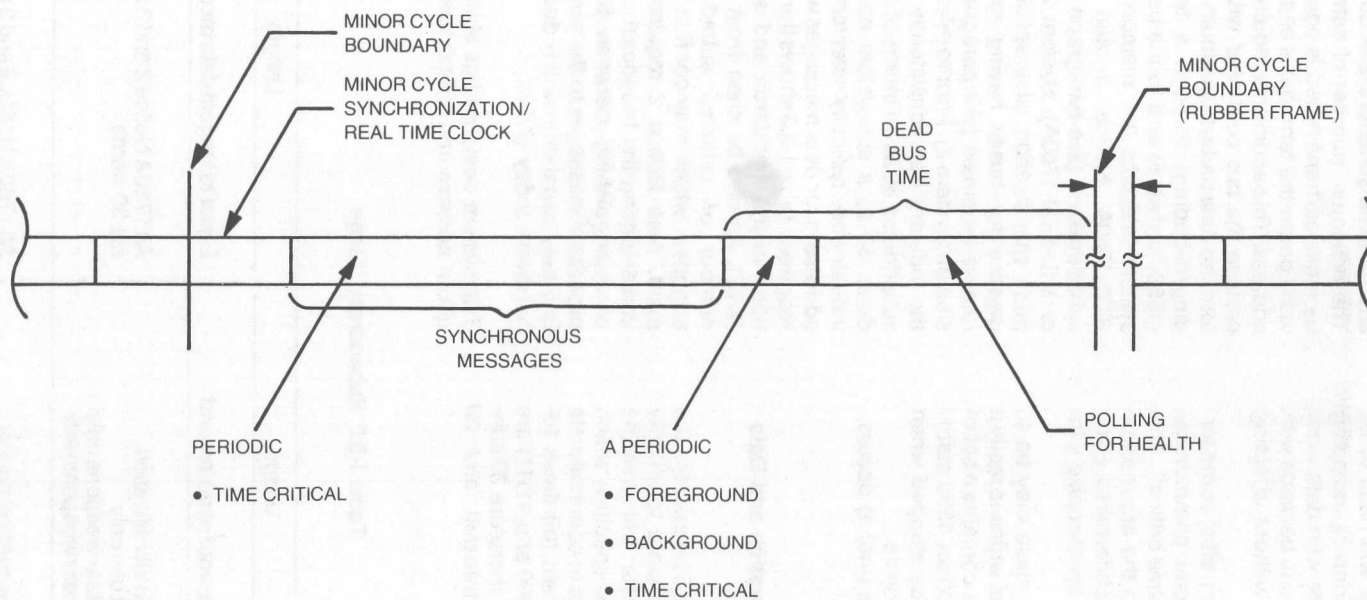


Figure I-3.12 Message Transmission During a Minor Cycle



terminal to switch its subaddress mapping number to an aperiodic (interrupt upon message arrival) table. If this occurs, the terminal will need to be returned to its periodic subaddress mapping number with another synchronize with data word mode code. Notice that changes can be made with subaddress mapping numbers without affecting the minor cycle number.

g) at the completion of periodic traffic, some terminals may be involved in aperiodic communications (foreground, background, time critical). This is accomplished by switching to the appropriate subaddress mapping table for each terminal. Each process may require use of the synchronize with data word mode code.

h) the final activity in a given cycle may be to switch to a set of communications which is really a background message list. This list contains a set of messages which request and collect 1553 status and subsystem health and can be stopped when the time runs out for the minor cycle.

i) return to a) or dead bus time until a) occurs.

### 3.7 Data Control

#### 3.7.1 Subaddress Selection/Operation and Data Storage

1553B remote terminals utilizes a 5 bit address (bit times 4-8) within the command word to identify data reception requests or data transmission requests. The bus controller also specifies which message set within the terminal is to communicate based on the 5 bit subaddress field (bit times 10-14). Two subaddress codes (00000 and 11111) are used to designate a mode code, therefore 30 subaddresses are available (30 transmit and 30 receive) for data use.

**1553B does not assign any subaddresses. However, Notice 2 says "a data wrap-around receive and transmit subaddress of 30 (11110) is desired."**

The maximum number of data words required to be received/transmitted is equal to the maximum word count the terminal is capable of for any subaddress. This additional requirement was added to provide the bus controller with a method of performing data pattern continuity (Manchester encoding/decoding) through a terminal's front end (1553 hardware) and to the beginning of the subsystem interface (i.e. memory buffer). Also MIL-STD-1760A Notice 2 and Notice 3 define subaddresses (see paragraph 7.2 for a discussion of MIL-STD-1760A). System 2, the nuclear weapons specification, also specifies certain subaddresses for buses having nuclear weapons as remote terminals (see paragraph 7.3 for a discussion on System 2). Prior to release of these notices, the industry had consistently been using receive subaddress 30 as an interrupt and transmit subaddress 30 as a subsystem health message. Also industry has typically selected lower number subaddresses for data messages when only a few were required. Table I-3.3 shows the subaddresses identified in the standards and specifications today (7/87). As can be seen from this list, a growing number of selected subaddresses are being assigned, which may conflict with existing equipment. Also Notice 2 requires remote terminals implementing the broadcast option to be capable of distinguishing between broadcast and non-broadcast messages to the same subaddress. This is a new capability which does not exist in most hardware today (7/87).

The system designer has always been concerned about address and subaddress assignments. The

Table I-3.3 Subaddress Usage

Standard/Specification	Usage	Length
1. 1553B Notice 2 SA 30 R/T	Data word wrap-around	Equal to longest data message of subsystem.
2. 1760A Notice 2 SA 1 T SA 8 R/T SA 19 R/T SA 27 R/T	Store identification Test use only Nuclear weapons only Nuclear weapons only	All 1760A Notice 2 and 3 messages are 30 words.
3. 1760A Notice 3 SA 11 R/T SA 14 R/T	Store control/monitor Store mass data transfers	All 1760A Notice 2 and 3 messages are 30 words.



proper use and selection of subaddressing can save considerable embedded protocol in data messages. Often mass transfers of data (greater than one 32 word message) occurs in 1553 systems. With proper use of subaddresses and memory mapping, multiple 32 word messages can be mapped into a contiguous memory area. This can be accomplished by assigning N (usually 16 or less) sequential subaddresses and then transmitting from or receiving these subaddresses and mapping to a contiguous block of memory. With the normal features of 1553B, an error can be detected and messages retired. Also this method does not require any particular order to the string of messages. In contrast, using an embedded protocol in 1553B data messages would require adherence to message order, sequence, and extensive error monitoring and correcting, which is not required with a set of sequential subaddresses. Another area where proper subaddress selection is necessary is for messages that require the terminal to interrupt and begin working on the data immediately upon arrival. These are usually aperiodic messages which require immediate attention by the subsystem. To meet this demand, one or more subaddress may be dedicated to interrupt on reception or transmission.

A third category of messages are safety related. These might include flight safety or weapon safety (conventional or nuclear). In these cases, subaddresses are spaced digitally (i.e. maximum hamming distance) to prevent single or multiple subaddress bit encoding/decoding errors from causing the received data from arriving at an incorrect internal memory location or a transmitted message coming from an incorrect memory area. Each of these three categories of message along with the needs of complex subsystems has increased the pressure on finding sufficient subaddresses when only 30 transmit and 30 receive are available. Early in the 1553 development process this problem became apparent, when two computers communicating with each other via the 1553 data bus, exceeded 30 data messages. Therefore, the need for expanded subaddressing was realized. The basic idea has been used for many years. Previous designs have employed the first data word as a flag or control word to provide a new subaddress for the remaining data words. This obviously carries and overhead of word count reduction. However, in recent years a more generic usage of these techniques has developed, which allows application to any remote terminal needing more subaddresses. This method is discussed next.

### 3.7.1.1 Extended Subaddressing

The ability to request a remote terminal to remap its 30 subaddresses as a function of time, minor frame processing, or message type (periodic, aperiodic, background, time critical) has been accomplished by tying message mapping and synchronization together in the system. To synchronize a 1553B system two mode codes are available: synchronize with data word (mode code 17-10001) and synchronize without data word (mode code 1-00001). Synchronize with data word is used to allow the system designer to identify which minor cycle or frame the remote terminal is to enter. Most systems operate with less than 100 frames per major cycle (time required for all periodic traffic to be transmitted once).

The data word in the synchronize with data word mode code allows the controller to switch subaddress mapping tables at anytime. The combining of synchronize and message mapping is shown in figure I-3.13, where the data word field is subdivided into a minor cycle number and an independent subaddress mapping field. This allows the mapping and minor cycle change to occur together or separately. If the subaddress field has one or more additional bits, the higher binary numbers (numbers greater than the number of minor cycles) can be used for aperiodic message mapping (foreground and time critical), background message mapping (multiple messages which do not complete within a minor frame), and

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	CYCLE NUMBER						1	SUBADR MAP NUMBER						

BIT	DESCRIPTION
0	Time info bit—if bit = 1, then bits 1–15 should be decoded as clock value
1	Minor cycle change bit—if bit = 1, set new minor cycle to value contained in bits 2–7
2–7	Minor cycle number
8	Subaddress change bit—if bit = 1, set new subaddress map to value contained in bits 9–15
9–15	Subaddress mapping number

Figure I-3.13 Synchronize Data Word  
Format Example

large data transfer maps. Included in the large data transfer maps can even be program downloads.

### 3.7.2 Data Buffering and Validity

Message validity requirements within 1553B necessitate the buffering of the entire receive message until validity of the last data word can be determined. The matter is further complicated by the desire to ensure that transmitted data from a remote terminal is from the same sample set. Mechanizations which have been implemented to meet these needs include: first-in/first-out (FIFO) buffers contained within the Bus Interface Units (BIU) circuitry and standard memory devices which employ a buffer switching scheme. The use of the first concept, a FIFO memory, is fairly straight forward. However, to ensure data continuity, a direct memory access (DMA) cycle long enough to read or write the total word count of the message is required. In today's processor systems, this timing constraint poses no problems. For the reception of data, the 1553 protocol control logic must be capable of clearing the FIFO (resetting the pointers to the starting address) in the event of an invalid message condition.

The second scheme, which is more commonly employed, allows the BIU to DMA directly into a memory buffer, usually on a word by word basis. A minimum of two buffers is established for each receive and transmit subaddress, each buffer being 32 words long (see figure I-3.14). The starting location of the buffers, a tag word for each buffer (see paragraph 5.1.4), and a series of control flags is usually contained in the Buffer Descriptor Block (figure I-3.15). These flags specify which buffer is to be used by the BIU circuitry and which is used by the host processor. In its simplest case, when the flag is set to the receive state, the BIU writes its data into one buffer as each word is received, while the host processor reads data from another buffer. When a complete message has been received, validated, and the final word stored, the BIU circuitry toggles the flag so that the buffers are now swapped. Obviously, if an error occurred within the message, the BIU would not toggle the flag. **For receive messages, the BIU controls the setting and changing of the buffer flag.** For transmit messages, when the flag is set for transmit, the BIU reads from one buffer while the host updates the data in another buffer. When completed with its update, the host will toggle the flag. **For transmit messages, the host updating the data controls, the setting and changing of the buffer flag.**

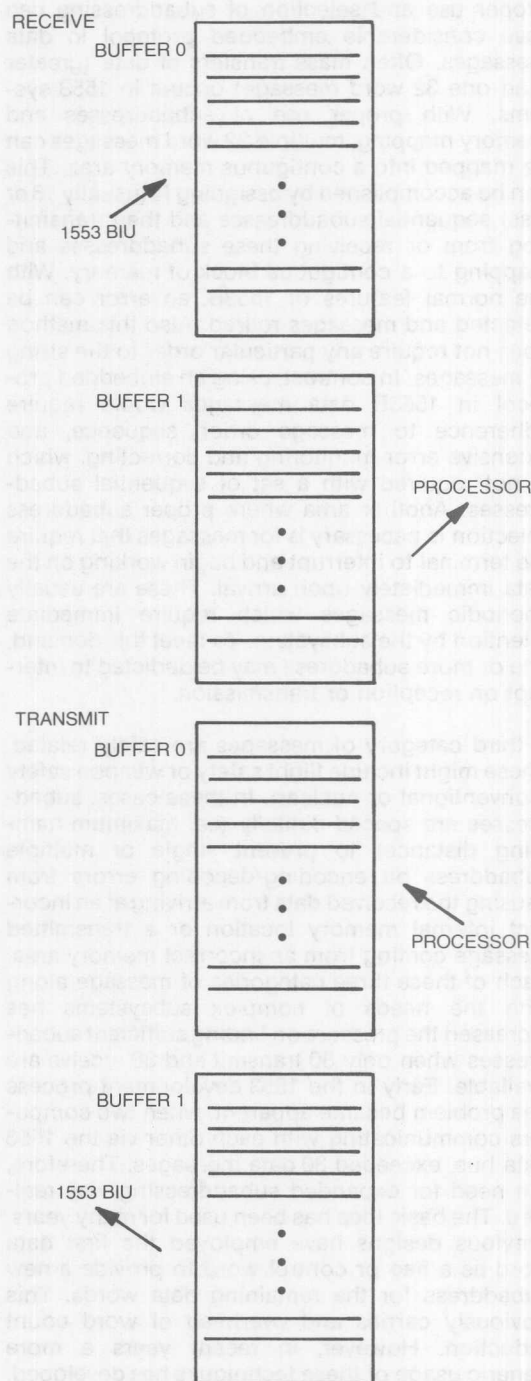


Figure I-3.14 Double Buffering Mechanization

Now there are obvious conditions during which switching of the flag (and hence buffers) is not a good idea. For receive data, with the BIU in control, this might occur after reception of a message, but NOT while the host is reading data from the opposite buffer, hence causing a mixture of old and new data. For transmit data, the host does not want to switch the buffers while the BIU is reading data from the other buffer. Therefore, some sort of handshaking between the host and the BIU is required.

However, before getting into the handshake protocol, there is a much more basic question regarding the transfer of data which needs to be addressed. Does the terminal want to always receive the NEWEST DATA available (e.g. in the case of flight control parameters), OR is it more important to receive ALL DATA in sequence (e.g. the case of data base transfers or program loads). In the case where newest data is required, the buffers are continuously swapped for each new message (assuming no errors). But in the case of wanting to receive all data, when both buffers are full (e.g. 2 messages received) AND the host has not read the contents of the first buffer, a problem exists because the next message would overwrite the first buffers contents, hence losing the data.

There are two simple solutions to the second case: first the use of more than two buffers; and second, the implementation of the busy bit in the status word. The first solution is simple, requiring only additional memory and the "housekeeping" logic to keep track of the sequence in which the buffers have been used (moving address pointers within a list). Some of the 1553 chip sets available support this approach. The second solution requires only additional logic within the BIU circuitry. The handshaking between the BIU, host, and busy bit is detailed as follows:

A BIU status flag is used to determine the status of the BIU with respect to the data buffer it is using. Similarly, a host status flag is used to determine the status of the host with respect to the data buffer it is using.

When newest data is desired, if the BIU and host status flags are cleared (inactive state), then the BIU/host is currently not using the buffer, while if these flags are set to the active state, the BIU/host is accessing the buffer. Note that these flags indicate the status regardless of whether the buffer is a transmit or receive data buffer.

Buffer swapping (the changing of the buffer flag) is performed as follows: Initially the BIU and host status flags are cleared (inactive state) and no valid data is contained in either buffer. For transmit messages, the host shall control the buffer swapping. To fill the current (selected) buffer, the host first sets its status flag to the active state, indicating its buffer is busy. When the host has completed updating the data, it changes its status back to the inactive state. When this occurs, the host looks at the BIU status flag and toggles the buffer flag if the BIU's status flag indicates it is inactive (not using its buffer). If the BIU's flag indicated it was accessing its buffer, then the host must wait until the BIU is finished prior to toggling the buffer flag. It is important to note here that Notice 2 requires that all data being transmitted on the bus must be valid. Therefore in the initialization process, the BIU must either be kept "off-line" until the host has updated one of its buffers and toggled the buffer flag, or the BIU must respond with the busy bit set in the status word until the host has updated one of the buffers.

For receive buffers, the BIU is in control of the buffer swapping. To fill the current buffer, the BIU first sets its status flag to the active state to indicate the buffer is busy (done at validation of the command word from the bus). When the BIU finishes writing data, it changes its status back to the inactive state. When this occurs, the BIU will look at the host status flag and toggle the buffer flag as soon as the hosts status indicates it is inactive. If an error occurred, the buffers are not swapped, and the erroneous data is overwritten by the next message to that subaddress.

When the collection of all data is desired, a BIU and host status bit cleared (set to inactive state) would indicate that the BIU/host has accessed and is finished with the buffer, while a status bit set to an active state would indicate that access to the buffer is currently in process or not yet started.

Swapping of the buffers and setting of the busy bit is performed as follows: For transmit data, the BIU and host status flags are initialized to indicate inactivity and activity respectively. This is done so that the BIU knows that there is erroneous data in its current transmit buffer. Here again, Notice 2 would require that the BIU respond with the busy bit set in the status word or be kept "off-line" until the host updates the first buffer. When the BIU or host is done accessing (updating) its buffer, it sets its status flag to the inactive state and checks the other flag. If the other flag is also inactive, then the

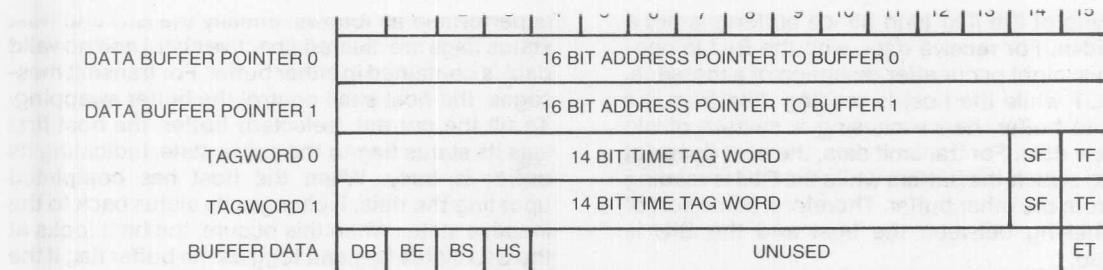


Figure I-3.15 Data Descriptor Block Format

data has not as yet been transferred out onto the bus by the BIU and the host must store the new data in the other buffer or somewhere else. For receive buffers, the BIU and host status flags are initialized to indicate activity and inactivity respectively. This is done so that the host knows there is erroneous data in its buffer. When a message comes in and the BIU has completed accessing its buffer, it shall set its status flag to indicate inactivity and checks the hosts status flag. If it is also inactive, the BIU shall toggle the buffer flags (swap data buffers) and set both the BIU and host status flags to the active state. BUT if the BIU's status flag is inactive and the host's status flag is active (both buffers full), and a new command is received over the bus, then the BIU shall respond with the busy bit set in the status word and not store the data. If an error is detected in a message, the buffers are not swapped and the BIU's and the host's status flags are not changed.

Due to the diversity of terminal designs, and the levels and complexity of memory buffering techniques, the design and implementation of the BIU/DMA/host interfacing logic is left to the subsystem designer and is usually not considered as part of the BIU protocol logic.

### 3.7.3 Block Transfers

Block transfers, moving of large amounts of data via the 1553B data bus, are common with today's data bus architectures. These transfers are used to exchange data bases between processor (e.g. primary and backup controllers), update navigational systems (e.g. GPS almanac data, digital map data bases, etc.), and perform operational program downloads.

One of the principal concerns in executing a block transfer is the handling of communications errors.

This has to be accomplished such that there are not redundant or missed messages in memory. Auto retry capabilities are usually implemented in the execution of these transfers. Subsequently, when an auto retry occurs because of an invalid message, the designer must implement the control protocol such that the retired messages will not appear twice in memory with one being invalid and the other valid.

Various schemes have been employed to accomplish these bulk transfers. Commonly used methodologies are: time spaced messages to a single subaddress; multiple messages with subaddresses; and the use of expanded subaddresses (see paragraph 3.7.1). The designer must make trade-offs between the amount of memory available, levels of buffering desired or possible, and the amount of subaddressing available for use to insure that the bulk transfers succeed in moving the proper amounts of data, in the correct sequence, with no errors.

### 3.7.4 Data Protection

Additional protection of the data, other than the message and protocol checks contained with the 1553 standard, can be accomplished. Since data words on the bus are no different than the data contents of a 16 bit computer (with the exception of being transferred serially, and containing a sync and parity field), the traditional methods of computer data protection can be applied. These include checksums and cycle redundancy checks (CRC). Each have their advantages and have been successfully used in 1553 applications. The major disadvantage is that since their purpose is to protect data being "communicated", they need to be included with the data (meaning the codes must be sent with each block of data versus a separate



any given message.

During early applications of the standard, some terminals did not protect against the mixing of old and new data within a message. While checksums and CRC codes were capable of detecting this type of error, their overhead was considered too great to be used in all messages. Therefore an effective, low overhead solution was developed - the validity bit. A validity bit (single bit) was assigned to each data word. Implementations varied as to the inclusion of this bit into each word (often the MSB) or placing all bits in the last two words of the message. The placing of the bit within the word reduced bus loading and allowed a single word read by the applications software, but it reduced the resolution of the signal it was attempting to protect. When set, the bit indicated that the associated data was good. When multiple words were involved, the processor updating the data would set the bits to the same pattern (0 or 1), alternating patterns at each update. Hence it was possible to distinguish data not of the same sample set. Today, most terminal designs, by the method of double or multi-level buffering, assure all data transferred is of the same sample set.

For data that must have extended protection, multi-bit detection and correction, a hamming code protection scheme is recommended. Section 80 (formerly Chapter 11) of MIL-HDBK-1553 Multiplex Applications Handbook provides an error protection word based upon a BCH (31, 16, 3) code which will provide error correction up to 3 bits. The overhead is great. For each protected word, an additional word is required, but if this level of protection is required — use it.

### 3.8 Data Bus Loading Analysis

Most newcomers to MIL-STD-1553B are concerned with bus loading. The serial bus standard is like many others; it works fine until you try to overload it. On the positive side of efficiency, the protocol established by the standard is a very efficient protocol and provides extensive data transfer capability.

Analysis of bus loading is a relatively simple matter requiring only a hand-held calculator, some data about the system, and some basic system decisions concerning use of the standard. There have been several computer programs developed to calculate bus loading. These programs are generally used on very large and extensive systems with

and its complexity than to calculate bus loading or build message sequencing. The basic data necessary for a simplified calculation of average bus loading is:

- (1) Message/type
- (2) Words/message
- (3) Overhead associated with each message type
- (4) Overhead associated with mode codes
- (5) Intermessage gap
- (6) Average response time
- (7) Overhead associated with non-stationary master bus controller passing

The overhead constants to consider (in microseconds) are:

- |  |                       |
|--|-----------------------|
| (1) Command word                                 | 20                    |
| (2) Status word                                  | 20                    |
| (3) Response time                                | 2-10 (average 8)      |
| (4) Intermessage gap                             | 2-100<br>(average 50) |
| (5) Mode codes without data words                | 20                    |
| (6) Mode codes with data words                   | 40                    |
| (7) Data words                                   | 20                    |
| (8) Non-stationary master bus controller passing | (48 minimum)          |

When calculating average bus loading each message type has a value where "N" is the number of words in the message.

- (1) Bus controller to remote terminal and remote terminal to bus controller  
 $20N + 68 = \text{Value for BC-RT}$
- (2) Remote terminal to remote terminal  
 $20N + 116 = \text{Value for RT-RT}$
- (3) Bus controller to remote terminals (broadcast)  
 $20N + 40 = \text{Value for BC-RT (broadcast)}$
- (4) Remote terminal to remote terminals (broadcast).  
 $20N + 88 = \text{Value for RT-RT (broadcast)}$
- (5) Mode code without data word  
 $68 = \text{Value for MC without data word}$
- (6) Mode code with data word  
 $88 = \text{Value for MC with data word}$
- (7) Mode code without data word (broadcast)  
 $40 = \text{Value for MC without data word (broadcast)}$
- (8) Mode code with data word (broadcast)  
 $60 = \text{Value for MC with data word (broadcast)}$

Therefore, the average bus loading is the sum of the message type values divided by 1,000,000 (maximum no. of bits/sec) times 100%. A system should not exceed 40% bus loading at initial design and 60% at fielding, in order to provide time for error recovery/automatic retry and to allow growth during the system's life.

### 3.9 Interface Control Documents

Section 80 of MIL-HDBK-1553 Multiplex Applications Handbook (formerly Chapter 11) provides the guidelines for the development of data words and message structure formats needed in the generation of Interface Control Documents (ICDs) for data bus compatible equipment. In addition, it provides suggestions for ICD format presentations and recommended coding techniques for various data words. Both the Navy and Army have developed data bases for terminals and systems which are available. Systems and terminal designers are encouraged to adapt these guidelines and formats in the generation of their own documentation and to make use of the data bases where possible.

In as much as Section 80 has been successfully adapted by much of industry for standardization of message and data word formats, it has some shortcomings in identifying all the required data needed by the systems level designer. Some of this data is available at the initial design while other parts may not be available until verification or final buy-off tests of the terminal has been performed. The purpose of this section is solely to identify the types to terminal data which the systems level and bus control software engineers need.

- a) Condition which sets the optional status word bits (busy, service request, subsystem flag, terminal flag) and any required responses by the bus controller
- b) Specific conditions for generation of mode codes and required responses to these
- c) Timing limits associated the mode codes (i.e. how long to reset or perform self test)
- d) Discretes to be monitored and a detailed operation of each (e.g. 'on-line', BC/BBC, etc.)
- e) Modes of operation and specific procedures associated with each (e.g. built-in-test, initialization, normal operation, maintenance, priority operation, etc.)
- f) Specific power up initialization sequence including required messages or programming (e.g. data loads, parameter initialization, operational controls, etc.)
- g) Maximum power up time till 'on-line' including

sequence (e.g. no response, followed by busy, followed by normal)

- h) Message timing constraints and interaction (if any) with the busy bit
- i) Self test procedures (internal, data wrap-around, etc.)
- j) Data coherence and sample consistency procedures
- k) Service request procedures (command sequence or vector word definitions)
- l) Bus electrical characteristics (output voltage, impedance, etc.)
- m) Electrical interface requirements (connector type, pin assignments, voltages, currents, etc.)
- n) Programmable terminal parameters (terminal address, operational modes such as monitor or backup controller)
- o) Specific hardware self test procedures, BIT word definitions, maintenance code definitions
- p) Specific polling procedures for monitoring bus and terminal health
- q) All subaddress and mode code message and data word formats in accordance with Section 8-0 of MIL-HDBK-1553
- r) First minor frame present and offset in each future periodic communications frame
- s) Unique shutdown requirements
- t) If message requires interrupt upon reception or transmission
- u) Unique or subsystem specific message strings (loading, mass transfer, sequence of messages, etc.)
- v) Mode switching constraints
- w) Validity bits (usage, rules for setting, interaction with data)
- x) Operational characteristics during "shutdown" transmitter mode code (i.e. is the terminal still capable of receiving and processing data from the bus)

## 4.0 Hardware

### 4.1 Types of Terminals

1553B defines a terminal as "the electronic module necessary to interface the data bus with the subsystem and the subsystem with the data bus. Terminals may exist as separate line replaceable units (LRUs) or be contained within the elements of the subsystem." **A terminal is further categorized by 1553B as either a bus controller, bus monitor, or remote terminal.**

### (1) Bus Controller

**MIL-STD-1553B defines a bus controller as "the terminal assigned the task of initiating information transfers on the data bus."** Notice that the definition does not necessarily depend on the physical design of the terminal but is determined by the assigned task of bus control. This implies that a terminal may have the capability of performing other functions, but during the time when it is assigned the task of bus control it is by definition a bus controller. Figure I-4.1 shows the generalized terminal functional elements that apply to a bus controller.

### (2) Bus Monitor

**A bus monitor is defined as "the terminal assigned the task of receiving bus traffic and extracting selected information to be used at a later time."** A bus monitor, therefore, is unique in that it performs no transactions on the bus (see figure I-4.2). It not only does not initiate information transfers as a bus controller, it is incapable of any response on the bus, including status response in the monitor mode. In fact, the bus monitor does not require a transmitter so it may be a "receive-only" terminal if it never performs another function (bus controller or remote terminal). However, **monitors usually have remote terminal capability to allow the bus controller to check their status health and com-**

**mand new operational modes.** Primary applications include collection of data for analysis and back-up bus controller monitoring of system status. The bus monitor, for instrumentation applications, listens to all messages or a subset of messages and stores the data internally or formats and outputs the data to a mass storage device or telemetry equipment. Many monitors are configuration programmable as to their function of message monitoring capability via 1553 messages. In association with a back-up bus controller (whether the back-up controller is either a monitor or a remote terminal), the monitor observes the bus transmissions and collects data, often performing the same operations as the bus controller with the exception of issuing commands on the bus. By operating as a monitor, the back-up controller is continuously aware of the state and operational mode of the system and subsystems. Therefore in the necessity of assuming control of the bus, the back-up controller can reduce its start-up time. This type of operation is often referred to as a "hot back-up".

### (3) Remote Terminal

**A remote terminal is defined as "all terminals not operating as the bus controller or a bus monitor."** This means that an RT cannot initiate information transfers on the bus as a bus controller and cannot

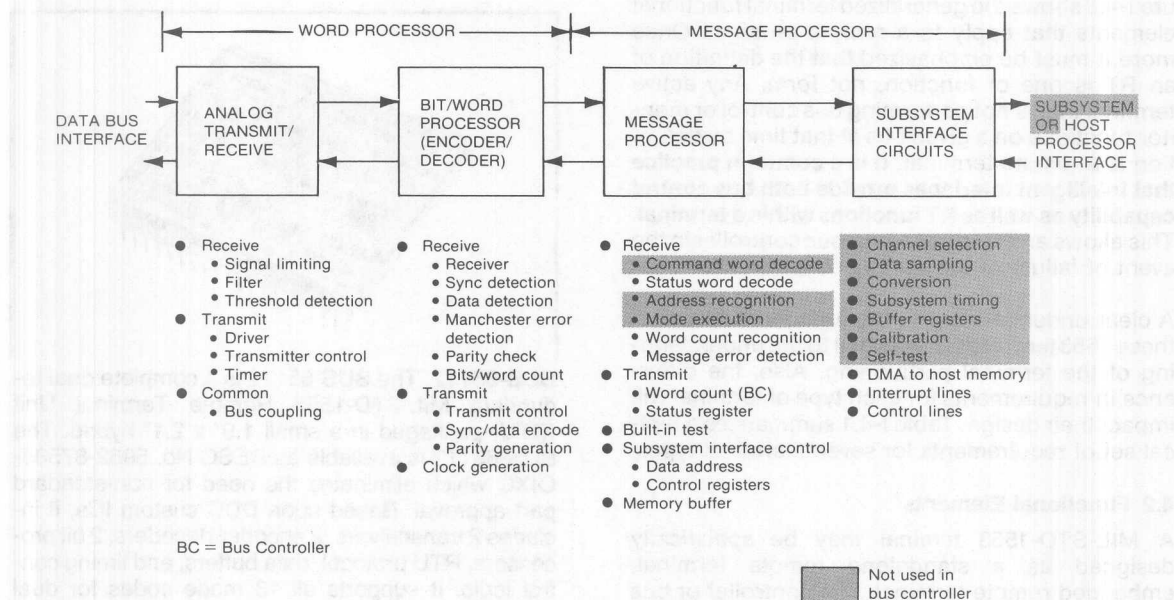


Figure I-4.1 Bus Controller Functional Elements

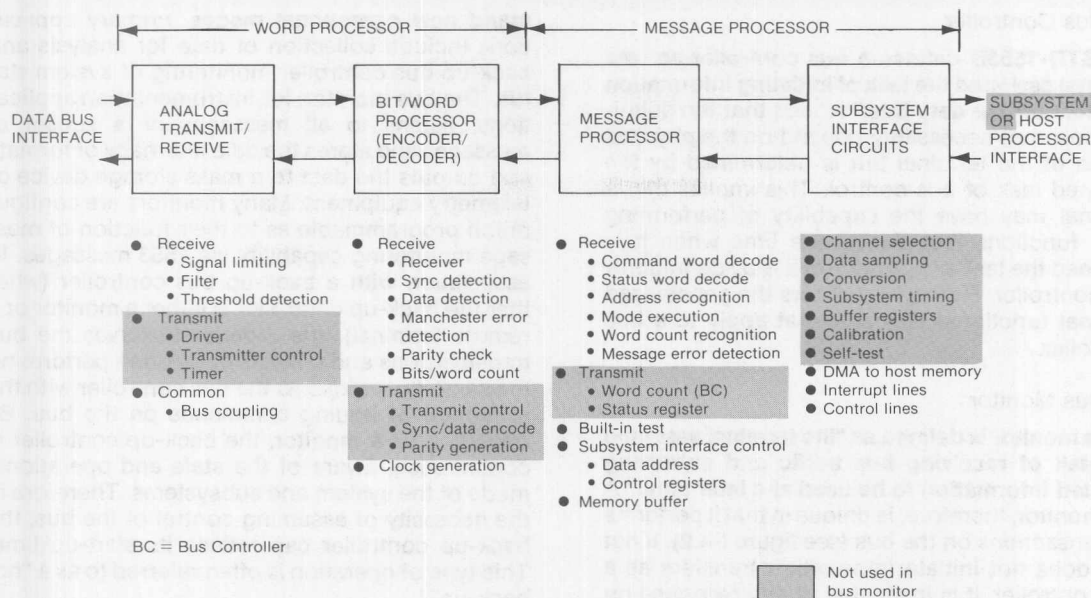


Figure I-4.2 Bus Monitor Functional Elements

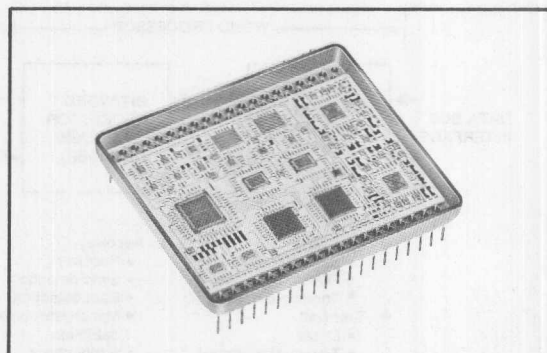
perform the monitor function. It must respond to commands issued by the bus controller in a normal command/response manner. **An RT is identified by a unique address that allows the bus controller to direct specific information to it.** Figure I-4.3 shows the generalized terminal functional elements that apply to a remote terminal. Once more it must be emphasized that the definition of an RT is one of function, not form. Any active terminal that is not performing bus control or monitor functions on a given bus at that time by definition is a remote terminal. **It is a common practice that intelligent interfaces provide both bus control capability as well as RT functions within a terminal.** This allows an RT to become a bus controller in the event of failure of the active bus controller.

A clear understanding of the functional nature of these 1553 terminals is essential to the understanding of the terminal partitioning. Also, the difference in requirements for each type of terminal will impact their design. Table I-4.1 summarizes a typical set of requirements for several terminal types.

## 4.2 Functional Elements

A MIL-STD-1553 terminal may be specifically designed as a standalone remote terminal, embedded remote terminal, bus controller or bus monitor. **Flexible terminal designs often perform both bus controller and remote terminal functions.**

This is achievable because of their intelligence (processing power) and a common front end design compatible with both remote terminal and bus controller functions. This section will describe



**BUS-65112.** The BUS-65112 is a complete dual redundant MIL-STD-1553 Remote Terminal Unit (RTU) packaged in a small 1.9" x 2.1" hybrid. The BUS-65112 is available as DESC No. 5962-87535-OIXC which eliminates the need for non-standard part approval. Based upon DDC custom ICs, it includes 2 transceivers, 2 encoder/decoders, 2 bit processors, RTU protocol, data buffers, and timing control logic. It supports all 13 mode codes for dual redundant operation, any combination of which can be illegalized.



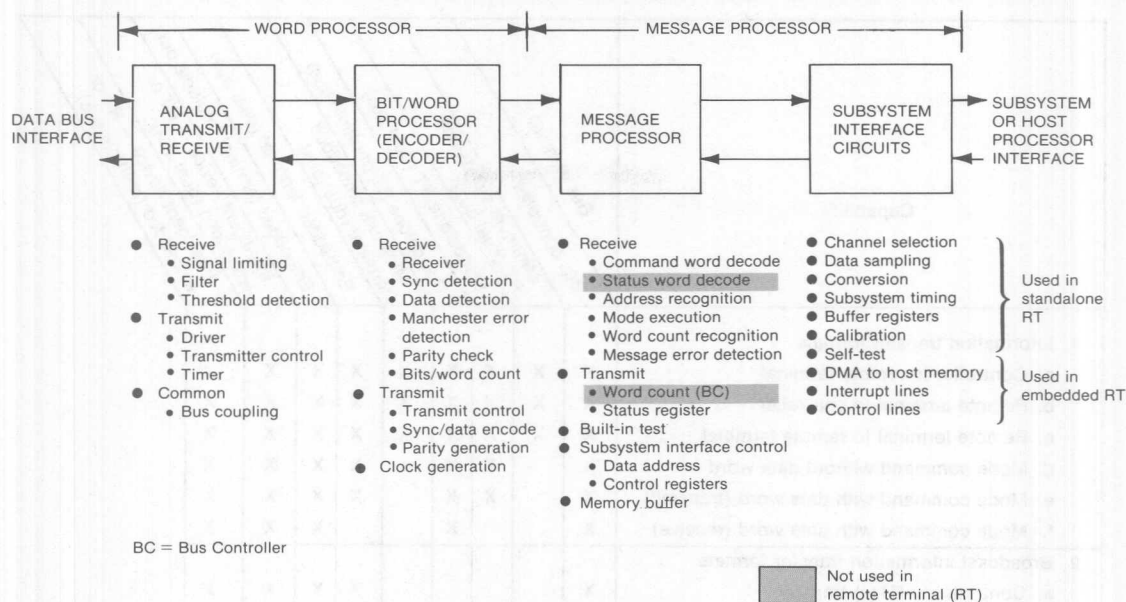


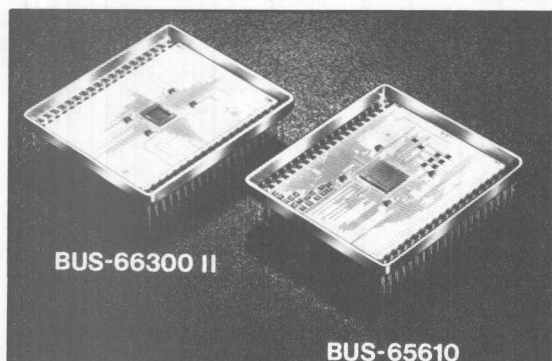
Figure I-4.3 Remote Terminal Functional Elements

the functional elements of a generalized terminal design. Figure I-4.4 identifies the major functions incorporated into a generalized terminal design. The four major functional elements are; (1) the analog receiver/transmitter, (2) the digital bit and word processor, (3) the digital message processor, and (4) the subsystem interface. Transfers of data in and out of each of these sections may be either serial or parallel or combinations of both depend-

ing on the design and the circuit implementation. As stated earlier, a 1553 terminal can be designed to perform both the bus controller and remote terminal functions. However, only terminals with a bus controller requirement should be designed to meet the more complex bus control functions. This section will discuss the common functions associated with all terminals and the unique functions associated with remote terminals and bus controllers. Two types of remote terminals will be discussed; a standalone remote terminal which interfaces non-1553 subsystems to the data bus and an embedded 1553 interface in a subsystem. The unique features of terminals performing as bus controllers will also be discussed.

#### 4.2.1 Analog Transmitter/Receiver

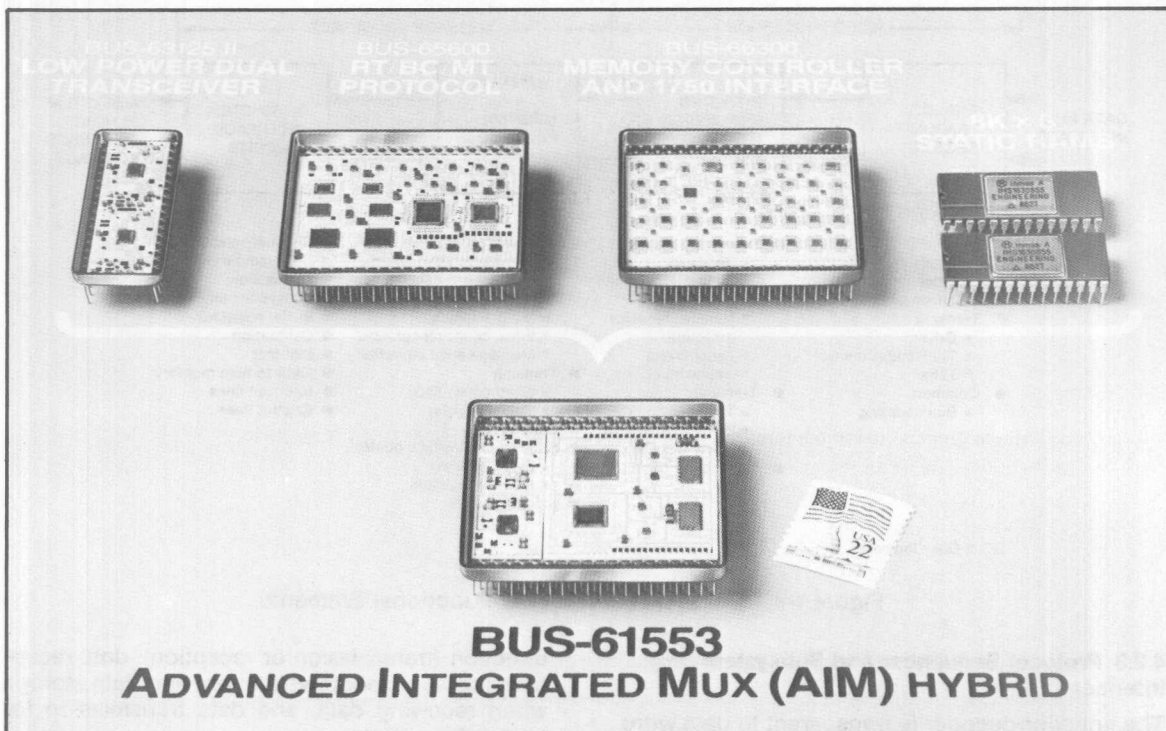
The analog transmitter/receiver functional element is primarily the analog front end required to interface the terminal's digital logic with the data bus. This section contains the coupling transformer and fault isolation resistors required for connection to the data bus. The 1553 receiver provides low level noise rejection and a digital output compatible with the digital logic that follows in the bit and word processor. The transmitter drives the bi-phase modulated signal to form data word formats defined in MIL-STD-1553B. A timer (analog or digital) is provided to cease transmission after a



**YOU CAN INTERFACE YOUR HOST CPU TO THE 1553 BUS** by using a BUS-66300 II interface module, a BUS-65610 BC/RTU/MT module, and a transceiver. The 1553 standard allows you to couple the transceiver directly to the 1553 bus, or couple it to the bus by means of a transformer.

Table I-4.1 Bus Element Capabilities

Capability	Bus element	Bus controller	Minimum standalone RT (dual bus)	Standalone RT	Standalone RT (dual bus)	Minimum embedded terminal (dual bus)	Embedded terminal (dual bus)	Embedded terminal (dual bus)	Intelligent terminal (multiple bus) embedded (dual bus) — RT or embedded (multiple bus)	Intelligent device — RT or embedded (multiple bus)
1. Information transfer formats										
a. Controller to remote terminal	X	X	X	X	X	X	X	X	X	X
b. Remote terminal to controller	X	X	X	X	X	X	X	X	X	X
c. Remote terminal to remote terminal	X	X	X	X	X	X	X	X	X	X
d. Mode command without data word	X		X	X		X	X	X	X	X
e. Mode command with data word (transmit)	X		X	X		X	X	X	X	X
f. Mode command with data word (receive)	X			X		X	X	X	X	X
2. Broadcast information transfer formats										
a. Controller to RT(s) transfer	X					X	X	X	X	X
b. RT to RT(s) transfer	X					X	X	X	X	X
c. Mode command without data word	X		X	X		X	X	X	X	X
d. Mode command with data word	X		X	X			X	X	X	X
3. Mode codes										
a. Dynamic bus control	X									
b. Synchronize	X		X	X						
c. Transmit status word	X	X	X	X	X	X	X	X	X	X
d. Initiate self-test	X		X	X						
e. Transmitter shutdown	X		X			X		X		
f. Override transmitter shutdown	X		X			X		X		
g. Inhibit terminal flag bit	X		X	X				X	X	X
h. Override inhibit terminal flag bit	X		X	X				X	X	X
i. Reset remote terminal	X		X	X		X	X		X	X
j. Transmit vector word	X		X	X			X	X	X	X
k. Synchronize	X							X	X	X
l. Transmit last command	X		X	X		X	X	X	X	X
m. Transmit bit word	X		X	X			X		X	X
n. Selected transmitter shutdown	X			X					X	X
o. Override selected transmitter shutdown	X			X					X	X
4. Status bit field										
a. Message error		X	X	X	X	X	X	X	X	X
b. Instrumentation (set to zero)										
c. Service Request			X	X			X	X	X	X
d. Broadcast received command			X	X	X	X	X	X	X	X
e. Busy			X	X		X	X	X	X	X
f. Subsystem flag						X	X			
g. Dynamic bus control acceptance								X	X	X
h. Terminal flag			X	X				X	X	X



**THE BUS-61553 ADVANCED INTEGRATED MUX (AIM) HYBRID** is a complete, stand-alone dual redundant MIL-STD-1553 interface. The BUS-61553 contains a low power dual transceiver, complete Bus Controller (BC), Remote Terminal (RTU), and Bus Monitor (MT) protocol, along with a powerful memory management host interface IC and a full 8K x 16 bits of static RAM. It is only 2.1" x 1.9" — the smallest, most integrated 1553 device available.

predetermined time (maximum 800 microseconds). This prevents uncontrolled activity on the data bus. The transmitter/receiver portion can be implemented using a combination of discrete circuits, hybrids, or monolithic chips. **Today these circuits are widely available in small low cost packages, thus eliminating the need to design your own device.**

#### 4.2.2 Encoder/Decoder

The encoder/decoder (see figure I-4.4) is used to analyze the data bits and words required for data transfer on the receiver side of the terminal. The squared up signal from the receiver is inputted to the decoder, which senses bit timing to decode the sync pattern, data bits, and parity to identify command/status or data words. Bit patterns other than the sync pattern are checked to verify proper Manchester coding. The number of bits per word and parity are verified to complete the bit and word

analysis. Error conditions are flagged if any portion of a bit or word is unsatisfactory. The encoder or data transmitter section contains the digital logic to establish both command, status, and data words for formatting; including sync, data, and parity generation. Control signals are provided to the analog transmitter/receiver section to indicate appropriate actions. **The encoder/decoder has been implemented in single LSI and Hybrid devices and are commercially available.** Usually these chips offer the best way to meet this design function.

Combinations of available analog transceivers and bit/word processors provide the basic bus interface function. This function is adequate for incorporation into the front end of computers performing as bus controllers, the front end of standalone remote terminals, and the front end of remote terminals embedded in a subsystem.

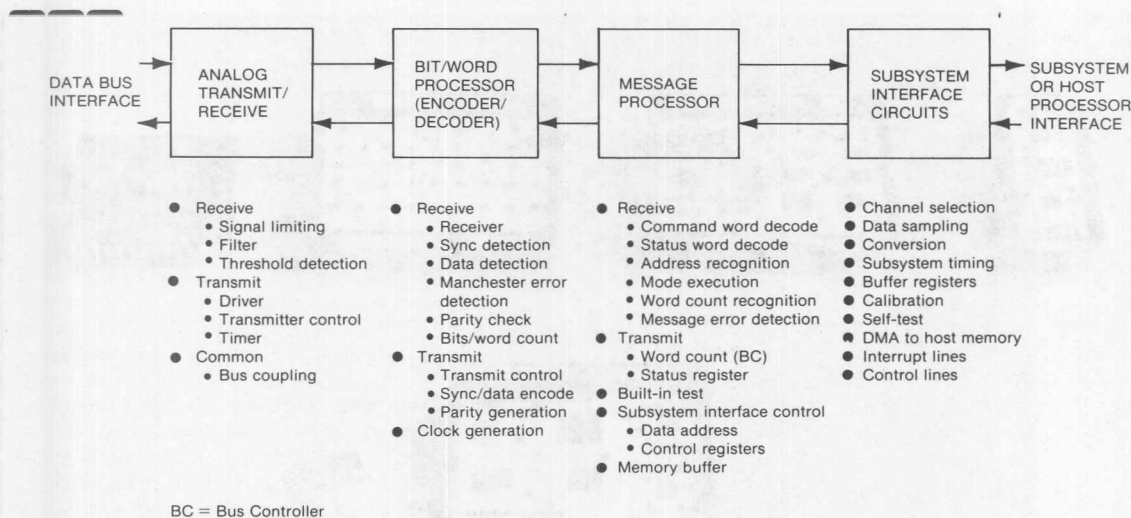


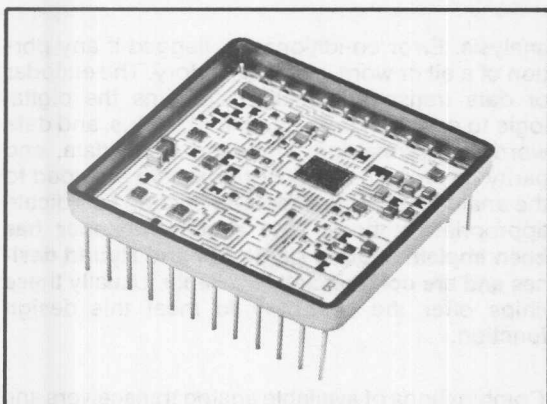
Figure I-4.4 Generalized Terminal Functional Elements

#### 4.2.3 Protocol Sequencer and Subsystem Interface

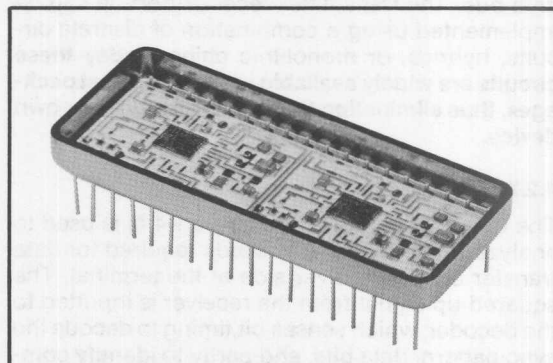
The encoder/decoder is transparent to data word type and contents. Therefore, it passes the words with the error indications to the message processor for further analysis. The message processor continues the analysis by performing command word decoding, address validation, data flow

direction (transmission or reception), data reception, message length validation, and data storage when receiving data, and data transmission for transmitting data.

A major task of the protocol sequencer is the subsystem interface control. The subsystem interface complexity may vary from a single parallel or serial handshake for communication to a DMA capability that provides an interface to main memory. Also, for standalone remote terminals, which must interface to multiple subsystems, the subsystem



**BUS-63102 II.** For systems that must interface with both MIL-STD-1553 and the McDonnell Douglas equivalent (F-18, AV-8B, etc.) a universal transceiver is available in DDC's BUS-63102 II. The pin out configuration is compatible with the earlier first generation transceivers measuring 1.25 x 1.25 in.



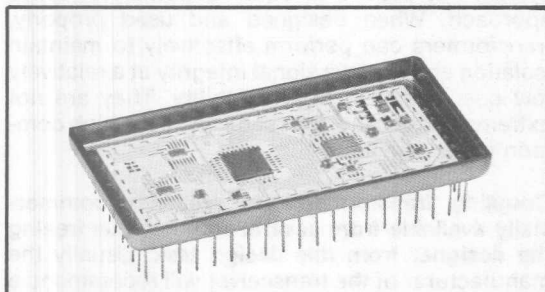
**BUS-63125 II.** This industry standard dual transceiver is now lower power and available as DESC No. 5962-87579-01XX, which eliminates the need for non-standard part approval.



interface may control and interface with a wide variety of signal conditioners (A/D converter, D/A converters, input and output discretes, serial and parallel channels) either directly or through a controller. It is because of this wide range of requirements and complexities (remote terminals versus bus controller) that system interfaces are usually designed for the specific application. The only exception to this is the circuitry that is being developed today to interface to microprocessors. Therefore, this is the area that most 1553 designers will be using their design talents in, since the analog transmitters and receivers, the encoders/decoders and protocol sequencers are available today in hybrid and LSI designs. Some manufacturers have even included the analog transceivers, further reducing the amount of circuit real estate required for the bus interface function.

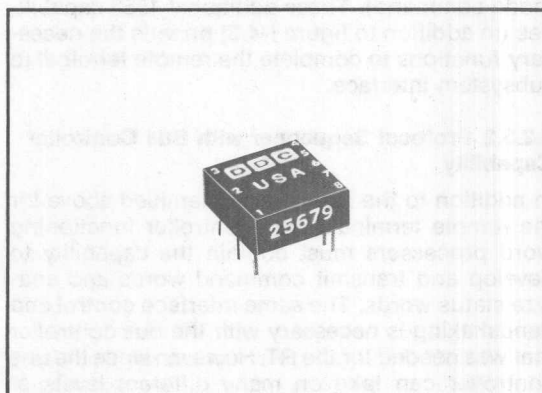
#### 4.2.3.1 Protocol Sequencer with Remote Terminal Capability

To initialize a remote terminal requires a mechanism for establishing its unique address. Two ways are available; establishing the address using an external strapping of pins to "open circuits" or "ground circuits" to establish a five bit address or host (subsystem or processor) software loaded. Each method has its place. For intelligent subsystems with a capability to change the software and for processors with software loads, software initialization of the terminal address is the most appropriate. **External pin addressing in software systems is required to identify acceptable software load and the remote terminal address used for loading the device if the load is supplied via the 1553 bus. For sensors or subsystems with fixed (unchanging) programs and for standalone RTs the aircraft wiring can supply the terminal's unique address.**



**BUS-64100.** This hybrid encoder/decoder, DDC's BUS-64100, contains the Harris 15530 Manchester II encoder/decoder plus additional IC's to offer address recognition, wrap-around self-test, parallel-to-serial and serial-to-parallel conversion.

Notice 2 requires that remote terminals must be capable of being assigned a unique address (address 11111 is still reserved for broadcast for those systems implementing this function) and that all addresses be established via an external connector to the remote terminal. The notice also specifies that changing the address must not require a physical modification or manipulation of any part of the remote terminal (i.e. changing of a memory device containing the terminal's address). No single point failure in the address strapping should cause a terminal to validate a false address. This means that, as a minimum, the remote terminal should include a parity bit along with the five address lines and should perform a parity check on the programmed address. As a minimum, that address should be validated during power-on initialization. In addition to the unique address, a terminal interfacing to a sensor, subsystem, processor or multiple subsystems/sensors requires a map or instructions indicating the destination of received messages based on their subaddress and the source or location of the data for each active transmitted subaddress. This can be hardwired in a standalone RT (subaddress to I/O port) or can be mapped using a "lookup type of table" or the mapping can be accomplished using a pointer technique often referred to as "Data Pointer Table" (see figure I-4.5). This allows a specific transmitter subaddress to be associated with a host supplied field to point to a location in main memory which is either the start of the data buffer or is the location of a word which contains the starting address of the data buffer. As you can tell, **several levels of indirection are possible using data pointers.** Therefore, the host can modify these pointers thus causing the terminal to acquire or deposit data



**BUS-25679.** DDC's BUS-25679 is typical of the many standard transformers available to couple the transceiver to the bus.

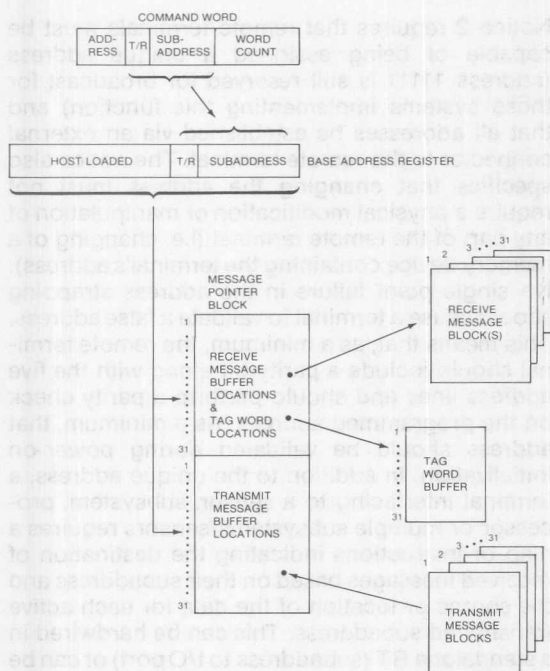


Figure I-4.5 Lookup Table Message Map

anywhere in memory. If this method is used the appropriate handshaking between the host and the message processor must be supported by the design. Additional host to remote terminal interfaces exist, which includes the ability to load the host's portion of the status word bits (service request, busy, subsystem flag, and dynamic bus control acceptance) and the mode code words that are host oriented (e.g., transmit vector word mode command). These additional 1553 capabilities (in addition to figure I-4.3) provide the necessary functions to complete the remote terminal to subsystem interface.

#### 4.2.3.2 Protocol Sequencer with Bus Controller Capability

In addition to the capabilities identified above for the remote terminals, bus controller functioning word processors must contain the capability to develop and transmit command words and analyze status words. The same interface control and handshaking is necessary with the bus controller that was needed for the RT. However, since the bus controller can take on many different levels of complexity and the partitioning between hardware and software is not as clear, a general discussion is provided in section 5 on this subject.

#### 4.2.4 Bus Coupler Design

Bus coupler networks, separate from the terminals, are required by 1553B when connected to the data bus via "long stubs". A long stub is defined to be greater than 1 ft. Direct coupling, which can be implemented without a separate coupler box, is defined for short-stub connections of 1 ft or less (Note: Notice 2 requires that for Navy applications, terminals must have both transformer and direct coupled stub connections externally available, such that either may be used; and that for Air Force and Army applications, ONLY transformer coupled stub connections will be used.) The long-stub coupler network incorporates isolation resistors and a coupling transformer. The isolation resistors are located in the terminal for the direct-coupled case, thus eliminating the need for a separate coupler box if a reliable shielded splice can be made. In most cases, the bus connections can be spliced in the terminal connector.

The coupler-transformer characteristics are very important to the signal integrity and noise performance of the data bus system. **The purposes of the coupler are to; (1) provide isolation of the main bus for fault conditions on the stub or in the terminal, (2) provide reduced bus signal distortion effect by increasing effective stub impedance, and (3) provide termination of the stub when transmitting from the terminal.** The isolation resistors and the transformer turns ratio provide the benefits listed above. The terminal input and output specifications for the transformer-coupled and direct-coupled connections are separated in 1553B, because of the effects on signal levels and impedance caused by the transformer turns/ratio.

The use of transformers as a means of coupling baseband signals in a balanced transmission line system has proved to be an extremely effective approach. When designed and used properly, transformers can perform effectively to maintain isolation and achieve signal integrity at a relatively low cost and with high reliability. They are not extremely lossy and can readily achieve high common mode rejection.

**Coupling transformers are presently commercially available from several sources thus freeing the designer from this design task.** Usually the manufacturer of the transceiver will recommend a transformer for use with the device. One point not to be overlooked is temperature rating. Most transformers have a lower maximum operating temperature than the other associated circuit components.

A review of Transformer design considerations is given in Chapter 4 of the "MIL-HDBK-1553 Multiplex Applications Handbook".

## 5.0 Bus Controller Software

At the lowest level, the function of a bus controller is to cause data to be transmitted over the 1553 bus. For the purposes of this discussion, the collection of hardware and/or software that implements the transfer of information over the 1553 bus will be referred to as the Bus Interface Unit (BIU). The bus interface may be implemented via several devices or by one of the sophisticated 1553 control units currently available on the market. These devices automatically wait a specified time (typically 14 microseconds) for a response from a Remote Terminal, know not to expect a status word after a broadcast command, etc. A dedicated processor or state machine may be utilized to offload the host CPU. The host CPU has the responsibility of downloading 1553 messages to the BIU and transferring data between the BIU and other system elements.

As a result, today's designers have a choice of 2 basic types of 1553 Bus Controller Units:

(1) Single Message Processors - this type of 1553 interface outputs individual messages without requiring overhead from the host CPU. The Bus Interface Unit determines the validity of the individual message and/or looks for anomalies in the status word. The host CPU is responsible for determining the next message to be transmitted, or the error recovery scheme to be implemented.

(2) Multiple Message Processors - this type of 1553 interface outputs a series of messages over the 1553 bus without host CPU intervention. Each message is validated by the Bus Interface Unit. If no errors were detected, the Bus Interface Unit will automatically issue the next message in the frame. If an error condition is detected, the Bus Interface Unit may halt 1553 transmissions or may continue normal operation until the end of the frame. Various error handling techniques may be initiated by the hardware, or may be left to the subsystem to resolve.

### 5.1 Single Message BIUs

Single Message BIUs essentially require that the subsystem initiate and evaluate each message that is transferred across the 1553 bus. These devices are usually less expensive than the more sophisticated Multiple Message BIUs. However, they require more host CPU overhead. With the low duty cycles typically encountered in 1553, it may seem that the CPU can easily handle both the 1553 activ-

ity in addition to other applications. The problem is that application software and bus traffic frequently grow in proportion with each other. The growth in bus traffic decreases the subsystem's processing capacity at the same time that more applications software is required to process the new data. This "double growth requirement" must be considered when performing the sizing and timing analysis of a Single Message type of BIU.

### 5.2 Multiple Message BIUs

In a Multiple Message BIU, once a START command is issued to the BIU, the subsystem is free to handle other activities. It does not need to be involved in the transfer of each individual message over the 1553 bus.

To accomplish this, the subsystem typically stores the 1553 messages in some portion of RAM that is also accessible to the BIU. The subsystem indicates which messages are to be transmitted by loading a stack with the addresses of the data blocks containing the messages, in the order in which they are to be transmitted. Alternately, the subsystem may chain the messages together, so that each message points to the next message to be transmitted. See Figures I-5.1 and I-5.2.

In either case, the subsystem must indicate how many messages are to be transmitted. This may be accomplished by loading a reserved word of the RAM with a message count, or by loading an "end of list marker" in the last message's forward pointer.

### 5.3 Message Headers

Regardless of the type of chaining architecture implemented, the BIU requires some "overhead information" for each message being processed. Typically, this consists of a control word indicating the type of 1553 message (Broadcast, Mode Code or RT to RT), a location to be used for storing the message's Time Tag, the channel on which the message is to be transmitted, the area of RAM to be used for storing or retrieving the associate data and command words, and the address of the next message. Additional information regarding error recovery options or interrupt control may also be included. (Error recovery techniques will be discussed in more detail in section 5.6).

In Multiple Message BIUs, the format of this header information is specified by the vendor. In Single Message BIUs, this header structure is defined by the user, and is implemented in software via the host processor.

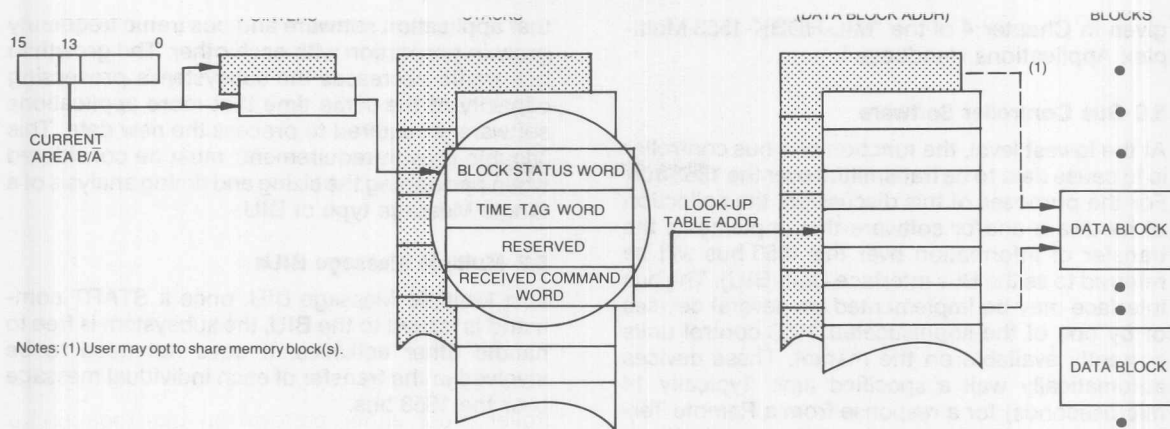


Figure I-5.1 Stack Oriented Architecture

The actual 1553 command words may be stored with the overhead information, or it may be stored with the data words associated with the message, depending on the architecture of the particular system. One or two words may be reserved for the command word(s) depending on the type of message (RT to RT for instance).

Most 1553 messages are time tagged. This value may be the actual contents of the system clock at the time the message transaction began or completed, or it may be a system defined 16bit number. In any event, it is linked to the particular message either by a pointer or by storing the actual Time Tag with the rest of the message's overhead information.

#### 5.4 Stacks vs Linked Lists

As previously mentioned, the address of the message(s) may be stored in either a stack configuration or in a linked list. Each has its advantages and disadvantages. A stack is simple to implement, and facilitates the implementation of minor frames. Separate stacks can be used for each minor frame. The host simply initializes the stack pointer to the appropriate stack each time the particular minor frame is to begin. See Figure I-5.3. Alternatively, the user can imbed the minor frames in the contents of the stack itself (see Figure I-5.4). For instance, assume that the frame consists of Messages 1, 2, 1, 3, 1, 4, 1, 4 and then the sequence repeats. The host can simply load the messages into the stack in that order, and issue a START command at the begin-

ning of each major cycle. A disadvantage of a stack architecture is that it is not easy to insert messages into the middle of an existing stack. A typical application would be to insert an error recovery procedure into the message stream upon detection of a no response or other error condition. The host would have to physically change the value of the stack pointer to point to the new message stack. When the error recovery messages completed, the host would have to reinitialize the stack pointer to point to the next message in the original stack.

In a linked list architecture, each message points to the next message to be transmitted. This makes it very easy to insert messages into the middle of the message stream. The bus controllers software simply replaces the forward pointer of the particular message with the address of the message to be inserted. The last message to be inserted would then simply point to the next message in the original list. See Figure I-5.5.

However, it is not as easy to implement the repetitive minor frames with a linked list architecture. For instance, let's assume that the frame consists of Messages 1, 2, 1, 3, 1, 4, 1, 4 and then the sequence repeats. The host can set the forward pointer of message number 1 to points to message number 2. The problem arises with the forward pointer for message number 2. If it points back to message number 1, the host will have set up an infinite loop since message number 1 point back to message number 2. One solution is to make another copy of message number 1 and store it in a different portion



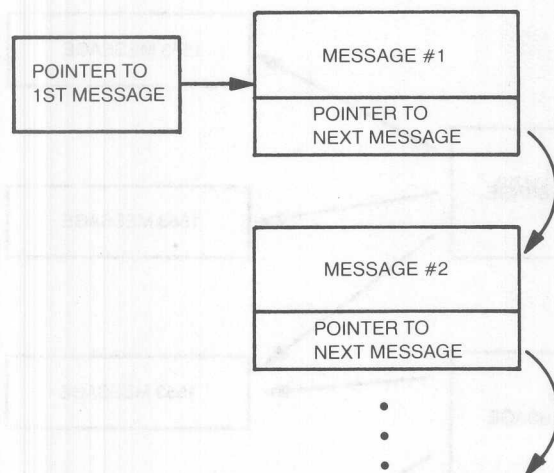


Figure I-5.2 Linked List Architecture

of RAM. Message 2 can then point to this copy of message number 1. See Figure I-5.6. That copy would then point to message number 3. The problem arises again with the decision of what to do with the forward pointer for message number 3. Additional copies can, of course, be made. However, this architecture requires much more memory than does the stack approach, as well as requiring much more system overhead to maintain the individual messages.

A linked list approach is somewhat more complex to set up. The bus controller software must embed the addresses of the next message in the body of each individual message block. As these messages may be scattered throughout memory, the possibility for error is somewhat greater than it is in the case of a stack, where the host simply loads a fixed portion of RAM with the starting addresses of the individual messages. With a stack it is also possible to see at a glance what messages will be transmitted, and in what order. A linked list typically requires a user to perform a memory dump of a much larger area of memory to trace the 1553 setup.

### 5.5 Status Word Analysis

The primitive bus controller must analyze each bit in the status word to determine if any extraordinary action must be taken. If several different 1553 protocols are used, the controller must differentiate the significance of the bits and act appropriately.

Because 1553A (F-16) allowed the message error bit to set when the status word was returned following message transmissions, that bit must be checked for each 1553A type transmission. The type of protocol (1553A, 1553B, F-16, etc.) will be indicated by either a field in the message header control word if each message can be a different protocol or by a control field accessible to the bus control software for block changes. **Because of the large inventory of 1553A equipment, the mixed mode of operation will exist for many years.** If a message error is indicated or if the status word is withheld the message is to be retried according to the established procedures.

If the service request bit is set, then the bus controller must either perform an interrogation to determine the specific service desired (transmit vector word mode code) and present the data to the main bus controller for a decision, or act upon the request based upon a table of actions known to the bus controller. See paragraph 3.6 for a detailed discussion of the protocol. The terminal flag and subsystem flag indicate faulty equipment. These problems are referred onto the main bus control program, unless an option exists to mask the problem (using an interrupt or to provide a branch to a set of instructions which collects data or resolves the problem). It may also be a requirement to pass these two flags onto applications software such as a fault detection, maintenance, or caution/warning, or other general applications programs. In addition to these two flags, the terminal address might also be required so as to be able to identify the faulty terminal. Since the data was received with no errors (for the fact a status word was received), the applications software may use the subsystem flag as one of its validity checks in determining whether or not to use the data. For these reasons, some applications store the status word along with the data words in the memory buffer. In other applications, if the status word and/or tag words are stored, they should be separated from the data in order to allow contiguous data blocks of more than 32 words. The designer should analyze the systems requirements and determine the method of storage to meet his own requirements.

The remainder of the flags (dynamic bus control acceptance or broadcast command received) are normally passed to the main bus control software as a special condition, but the bus control software should be used in performing dynamic bus allocation as an operational function. The busy bit is normally handled the same as an error, since a

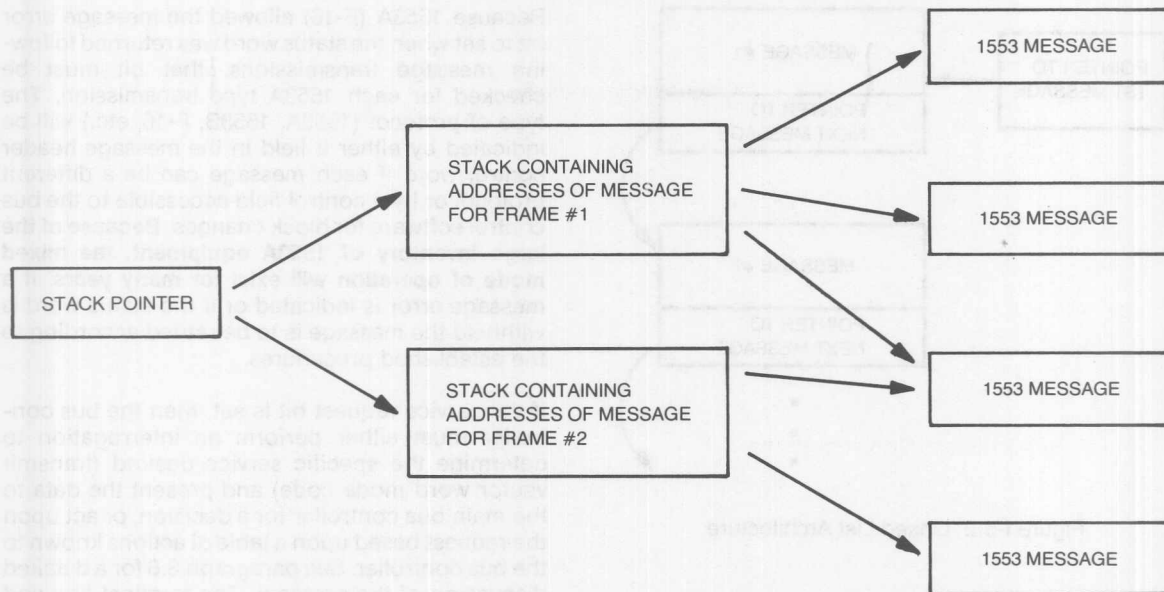


Figure I-5.3 Use of Stacks to Implement Minor Frames

retry could be quicker than the analysis to determine that the device was busy rather than an error had occurred. By the time the retry is initiated, the device should have removed the busy bit.

### 5.6 Error Handling

The extent to which specific error handling is included in the bus control software is a matter of design and the level of protocol which is embedded within the bus controller. It is difficult to embed specific error handling and recovery procedures because each application has different needs.

The bus controller is responsible for the execution of the parameters indicated in the channel control words. Certain error handling activities are implicit for these parameters. **The bus controller is responsible for detecting that a message has not been completed; either by hardware indicating a bit error, word count error, Manchester waveform error, or lack of a status word.** Then the bus controller will time out and request the status word (transmit status word mode code) or simply retry the message according to the rules given in the message header blocks. The most commonly used procedure is to retry once on opposite bus before trying next message in the list. Many variations are available once it has been determined that the

message has failed to pass the retry procedure. These issues are discussed in the next section under Error Recovery (see paragraph 5.2.5).

### 5.7 Tag Words

In time critical functions (e.g. flight controls), it is often necessary to "time tag" the data such that the applications program has an indication as to the data latency or sample period of the data it is processing. In some applications, the "tagging" of the data occurs at the source with the tag word being inserted (usually in the first data word) to the message containing the data. During bus transmissions, this would be processed as normal data and passed to the applications program for processing.

In other applications, the terminal receiving the data will time stamp the data itself, usually using its systems clock as the tag. This tag word is then stored not in the data buffer with the data, but in an accessible location to the applications program, usually the Data Descriptor Block (see Figure I-3.14). If multiple buffering schemes are implemented (see paragraph 3.7.2), then a tag word for each buffer would be required. One other tag word approach is used, where the receiving remote terminal uses the minor cycle number, message validity indication, and an active buffer indication.

These tag words are collected in a common buffer area for the applications software to examine when it begins processing of this minor frame data. In hierarchical architectures, where data must be passed between bus networks, data latencies can expect to be increased.

Terminals "tagging" the data, which are functioning as the gateway, present a problem. It may be necessary for this tag word to be appended to the data being passed through. In order to accomplish this, the tag word must now be stored with the data in the data buffer. By the terminal appending this tag word, the maximum word count of the original message is limited to 31 words.

### 5.8 General Software Considerations

Many of the functions previously discussed could be implemented as separate BIU software or BIU hardware/firmware. **Functions which almost always fall into the software domain outside of the BIU are: BIU initialization, synchronization, asynchronous message insertion, scheduling tasks waiting for bus-oriented events, and message/device error handling, recovery and reconfiguration.**

### 5.8.1 BIU Initialization

The BIU must be set up for communications and the flow of information controlled at a high level. The interface between the bus controller software and the BIU hardware/firmware is: (1) control words which direct the BIU to perform certain functions during the normal course of message transmissions and reception. This type of information is conveyed in the message header blocks; and (2) An I/O interfaces which provides the mechanism for the initialization to be performed.

The following types of data are typically communicated through this interface:

- 1) Characterization Data
  - a) Whether the BIU is to act as a bus controller or remote terminal.
  - b) Terminal number (unique MIL-STD-1553 address).
- 2) Access Data
  - a) Pointer to the next message header block that should be accessed for normal operation.

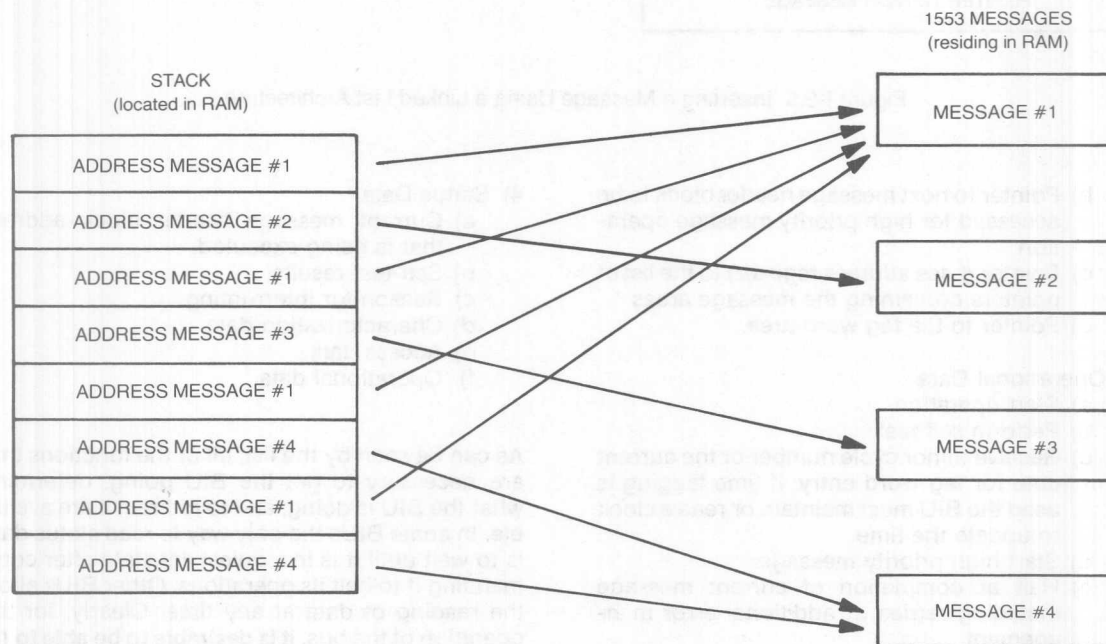


Figure I-5.4 Alternate Use of Stack to Implement Minor Frame

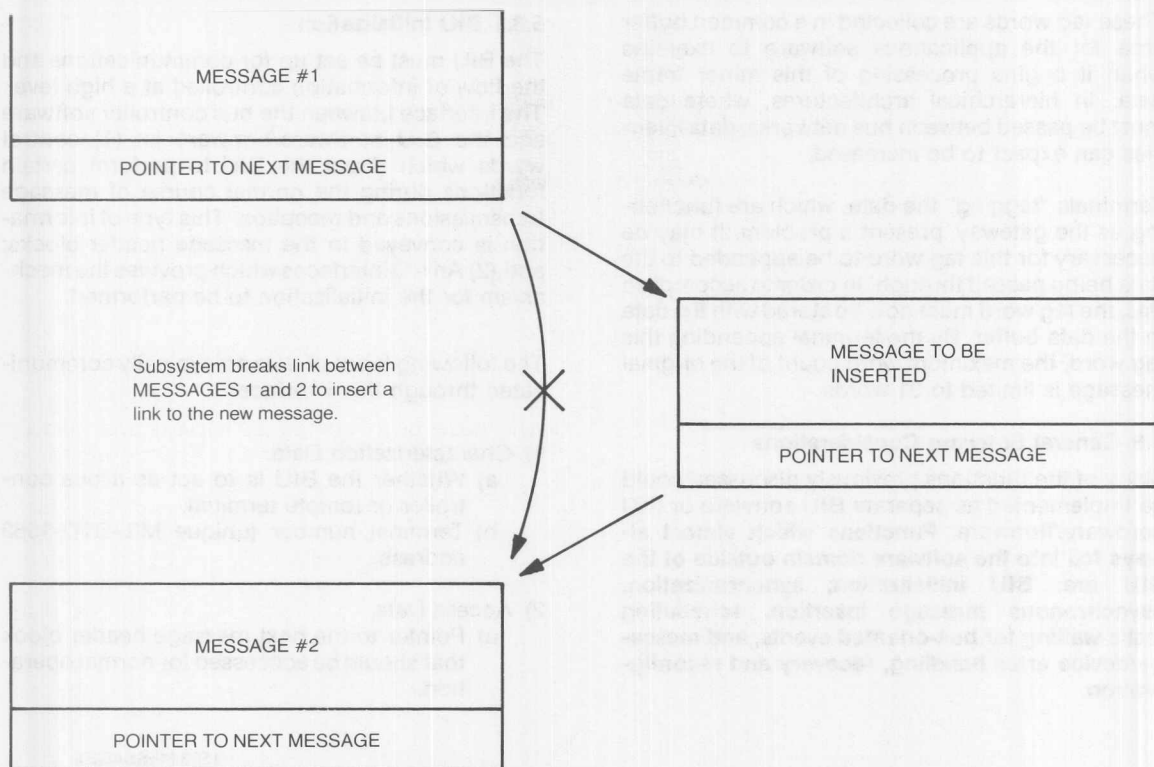


Figure I-5.5 Inserting a Message Using a Linked List Architecture

- b) Pointer to next message header block to be accessed for high priority message operation.
  - c) Pointer (base address register) to the list of pointers containing the message areas.
  - d) Pointer to the tag word area.
- 3) Operational Data
    - a) Start operation.
    - b) Perform self test.
    - c) Receive minor cycle number or the current time for tag word entry. If time tagging is used the BIU must maintain or read a clock to update the time.
    - d) Start high priority message.
    - e) Halt at completion of current message including retries or additional error management.
    - f) Halt immediately.
    - g) Resume operation from wherever the suspension occurred.
  - 4) Status Data
    - a) Current message header block address that is being executed.
    - b) Self-test results.
    - c) Reason for interrupting.
    - d) Characterization data.
    - e) Access data.
    - f) Operational data.
- As can be seen by the list, all of the functions that are necessary to get the BIU going, determine what the BIU is doing, and to redirect it are available. In some BIUs the only way to read status data is to wait until it is in a quiescent state after commanding it to halt its operations. Other BIUs allow the reading of data at any time. Clearly, for the operation of the bus, **it is desirable to be able to (at least) determine the current and next message header block addresses, so that alterations in the chain can be made for asynchronous messages.**



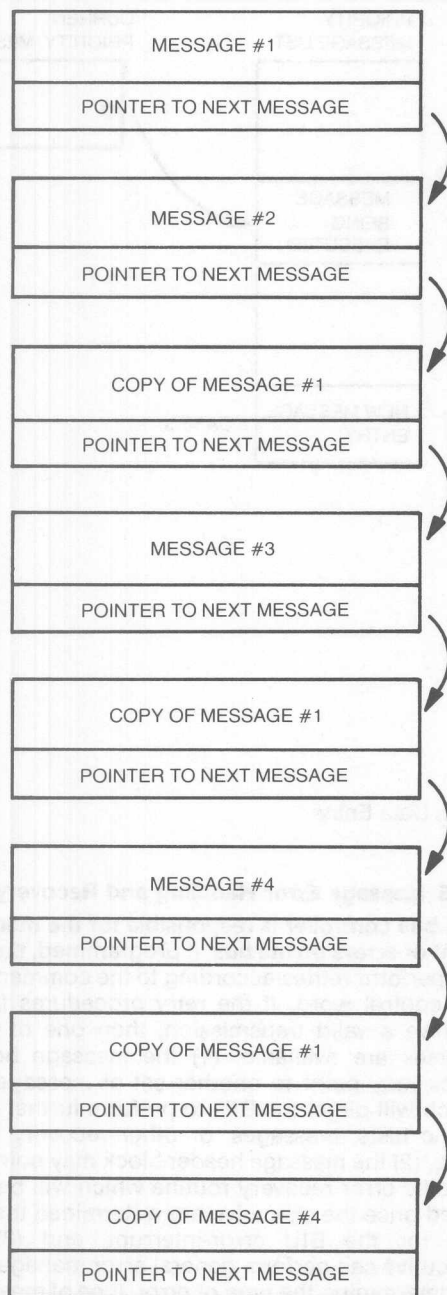


Figure I-5.6 Use of Multiple Copies of Individual Messages to Implement Major Frames

### 5.8.2 Controller Synchronization

Two or more processors (as well as the primary and back-up controller) may require knowledge as to what "address state" the others are in, as well as "what time it is." In large systems more than 30 different input messages are required to be transmitted on the same bus to the same device. This condition leads either to the addition of more buses or a change of message subaddress meaning between each minor cycle (see paragraph 3.1.1 for protocol discussion). Synchronization is a method of signaling each processor that it is time to change the message memory map to the indicated minor cycle. Minor cycle synchronization also indicates that the previous set of transmissions have been completed. This signal allows tasks waiting for completion to begin processing on the data that arrived during the last minor cycle. This type of coordination can assure that the task will operate on data that is integral and not subject to change. Consequently, all synchronous tasks can wait for the start of the next minor cycle, unless a severe timing constraint exists that requires a task to process its data immediately upon arrival. In this case an interrupt must be set up to accomplish the scheduling of the affected task.

### 5.8.3 Asynchronous Message Insertion

An aperiodic message may be requested to be sent by the applications software via an executive request. The bus controller must link the data into the appropriate message stream, usually in one of three ways: (1) by priority into the bottom or top of that priority level (Figure I-5.7 case 3), (2) as the next available message to be transmitted (Figure I-5.7 case 1 or 3) as the last message to be transmitted (Figure I-5.7 case 2). Finally, there may be a special BIU priority transmission as the next message out (Figure I-5.7 case 3). The message headers may contain the capability to unlink (go back to where it was before the priority interrupt). However, the bus controller must remove the asynchronous message from the transmission list or link into the message list chain (in the case of "transmit immediately"), since it may point into a special asynchronous area as shown in Figure I-5.7 case 3. In the third case the asynchronous transmission would be initiated immediately and the next message header block would cause a branch back to the next synchronous instruction to be transmitted. Note that these techniques require that the bus controller determine which message header the BIU is operating upon, inhibit it from accessing the next one, and link into the message list chain as shown in Figure I-5.7 case 1.

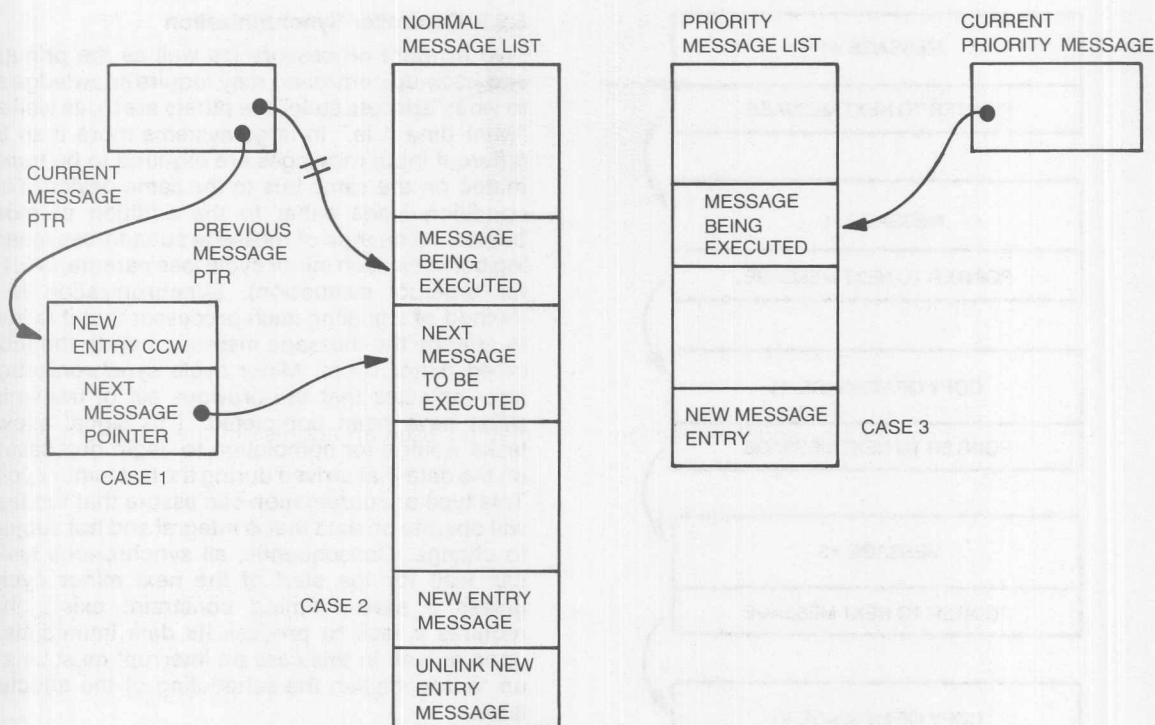


Figure I-5.7 Asynchronous Data Entry

#### 5.8.4 Scheduling Via Bus Event

A scheduler can potentially activate tasks based upon a number of events which can occur over the bus such as minor cycle synchronization, arrival of a message, and completion of a message transmission. **The most common occurring event is the minor cycle. All normal synchronous tasks can wait for this event, either in a wait queue or by having the cyclic tasks grouped together. Because this is so dominant, a special routine may speed the process.** The remaining tasks will be waiting on event queues, one per event. The message arrival/transmission event can be signaled in some BIUs by interrupting if a particular bit is set in the control word for transmission or reception on the bus controller, or as part of the message pointer in a remote terminal. The interrupt handler must determine the cause of the interrupt, then it will pass control to the bus controller to determine the reason for the interrupt. After this it will pass control to the event handler to set the event, which will schedule tasks that have been waiting for the event.

#### 5.8.5 Message Error Handling and Recovery

**The bus controller is responsible for the management of errors on the bus.** If programmed, the BIU will perform retries according to the commands in the control word. If the retry procedures fail to achieve a valid transmission, then one of three courses are available; (1) the message header block may point to another set of message lists which will direct the BIU to perform further diagnostic tests, messages, or other recovery functions, (2) the message header block may point to a specific error recovery routine which will be executed once the executive has determined the reason for the BIU error-interrupt, and (3) the executive can perform general error management by determining the type of error, type of message, source/destination, and by performing various types of diagnostic analyses according to time availability and need.

Many different error management schemes exist based upon the system requirements and individual designer's choice. Three examples are given to

show the variety which can exist for error management routines:

(1) Some error handling mechanisms simply delete communication with that remote terminal until the conclusion of the major cycle, at which point a test message (e.g. transmit status word mode code) is sent to the RT to re-establish communications. The results of the test message weighted by some recovery algorithm (e.g., 5 correct responses in a row) will allow the re-admission of communication with the RT.

(2) Ignore the failure and proceed. This moves error recovery from the channel controller to the applications software for determination that a problem exists which requires additional action. The tag word is a valuable tool in this mode, since it provides a time stamp (in terms of either minor cycle number or BIU/processor clock time of arrival). The application software must determine when the non-arrival of data becomes important and must invoke higher level application software and bus control functions to acquire alternate sources of data if such exist. The problem encountered in ignoring faults in communication are two fold: a) data is not necessarily gathered relative to the device failures and b) multiple failures can cause excessive transmission delays which can in turn cause minor cycle overruns. A variation on this is to perform error retries until a maximum number of retries have been used. At that point discontinue retries and finish the transmissions necessary for completion of the minor cycle.

(3) Respond immediately to the failure and initiate simple retry procedures based upon the channel control word parameters. The message header block may point to individual applications oriented executive software routines that involve specific error management routines embedded in the bus controller. These functions may be necessary to perform a self-test or to cause a message sequence to be retried from the beginning. This approach provides more flexibility in the management of errors than the first approach, since the first approach could be implemented in terms of the capabilities described in the second. **The bus control interface must provide utility functions that could be invoked by user-defined routines for specific message sequences.** The more pre-programmed version of this type of error management the more a common recovery procedure is established for a specific class messages (there may be two or three general classes). These procedures can invoke self-test in other RTs, decide when a

device is faulty and invoke reconfiguration functions. **Generally, the quicker the problem can be identified, the guilty established and recorded for later analysis (off-line) and the recovery performed, the simpler the system design will be.** The availability of redundancy (similar or dissimilar) plays an important role in arriving at a quick solution. Remember, while the system is resolving the problem, it is not doing its primary job.

### 5.9 Message Reception and Use

When a bus controller commands a message to be transmitted to itself, the memory address into which the message is to be sent is computed in two ways; directly and indirectly. The direct address method uses an address in the channel control word to explicitly state the destination address. The advantage of this method is that it is very efficient for the bus controller and retains very explicit control at all times as to where the message will go. The indirect method makes use of a message subaddress and a base register. **The subaddress and T/R bit of the 1553 command word is added onto the base address to determine the address of the memory location containing the destination address of the message** as shown in Figure I-5.8. This extra level of indirection is used to make it very easy to change the location to which a message will go by simply changing the base register to point to another block of message addresses. The advantage of this method is that it is very easy to double buffer (or multi-level buffer) messages coming into a device at the highest update rate. Note that all message addresses can be changed when changing the base address register. Even if none are to change the base address concept could be employed. Each method requires that the number of words in the message be contained within the message header block. The disadvantage is for each message access, a separate memory fetch is required to determine the actual message location. A combination of the two methods results in a base address pointing to the beginning of multiple fixed 32-word message blocks. This method was used on some of the simpler bus controllers. The cost of simplicity is the 32-word message buffer regardless of message length.

If a bus controller must also act as a remote terminal, the message reception mechanism must be different from a direct address scheme. **The subaddress and pointer mechanism is the normal method for the reception and transmission of messages.** In the most general case, each message

message has either arrived or been transmitted.

An example of such a descriptor format is shown in Figure I-3.14. This method allows double buffering which the remote terminal BIU must perform by exchanging the two pointer variables. Additional actions which may occur are setting an event flag or causing an interrupt on either the arrival or the departure of a message. These constructs allow two messages to come to the same subaddress without immediate software processing of the message. Such constructs also allow a "loose" coupling between the timing of the message arrival and the processing of the message. If only a single buffer were used the first message must either be processed or it would be written over with the arrival of the next message to the same subaddress. The interrupt, on the other hand, allows immediate attention upon arrival of a particular message (e.g., deliver the weapon).

**In conjunction with the arrival of each message can be a tag word identifying some characteristics of the transmission.** For example the validity of the message and time of arrival are two transmission parameters of use to applications software. The 1553B standard states that invalid messages are not to be used. In reality most designs require a message to be deposited word by word as they arrive. If a word in the middle of the transmission is in error, the remainder of the message may not be deposited. This situation would result in part of the new message and part of the old message being consolidated together. At best the data would be independent and not matter or at worst the data might be word-coupled (e.g., two words in a floating point number) and changing one part and not the other would completely change the meaning of each. A tag word allows the application software to determine validity and decide whether to use the old data, the new data, (valid to the point of error discovery) or neither in its computation. The tag word could also be the key into the error management/reconfiguration routines as discussed in paragraph 5.2.

Once the data has been received, the final step is to make the data available to the application software. In most 1553 systems, the data is available at all times to the applications software, and it is incumbent upon the applications to determine the validity of the data (e.g. was the subsystem flag bit set or is a validity bit associated with the data words) and which of multiple buffers to use. In

with an input are completed before commencing processing or by using buffers which have been filled and isolated by the 1553 BIU. If the system is very concerned about data integrity then completed buffers can be moved to the applications software for use. Then when complete they can be output from the applications software to the 1553 transmission buffers. However, the rather high penalty of copying each message discourages most users from applying this technique.

## 6.0 Testing, Integration, and Instrumentation

### 6.1 Testing

The purpose of any form of testing is to determine the quality or functional capability of an item. In the testing of 1553 devices, the purpose of the test procedure is to verify that the design does meet the 1553 specifications and that the options implemented have been done so correctly.

In the early days of 1553 implementation, there were few, if any, standard components (e.g. transceivers, encoders/decoders, protocol sequencers, etc.) available for the designers to use. Therefore, designers were developing their own based upon their interpretation of the standard. In addition, there was no standard "off-the-shelf" 1553 test equipment available to test the design, so the designers had to develop limited capability testers themselves to prove that their own designs worked and to provide their production facilities with a method of testing. As time and the popularity of the standard progressed, standardized components (sometimes available from multiple sources) started to become available. More important though, the experience in testing and integrating 1553 systems has led to the generation of a series of standardized test plans to support these requirements.

#### 6.1.1 Levels of Testing

The levels of testing can be identified as follows: developmental, design verification, production, systems integration, and field/operational testing. These levels may be applied to the remote terminal, bus controller, monitor, or actual bus system (cable, couplers, stubs, etc.). These levels are discussed as follows:

(1) Developmental Testing. Developmental testing begins with the breadboard of the design. It is used to determine the circuits operation and to eliminate any design flaws. This level of testing



also includes the testing of the circuits operating margins and tolerance limits usually over the required operational requirements (e.g. temperature range, etc.).

(2) Design Verification. For design verification, usually a preproduction unit is subjected to a series of tests designed to verify that the unit satisfies the requirements of the 1553 standard and the options specified in the system specification. This level is generally the most extensive phase of testing.

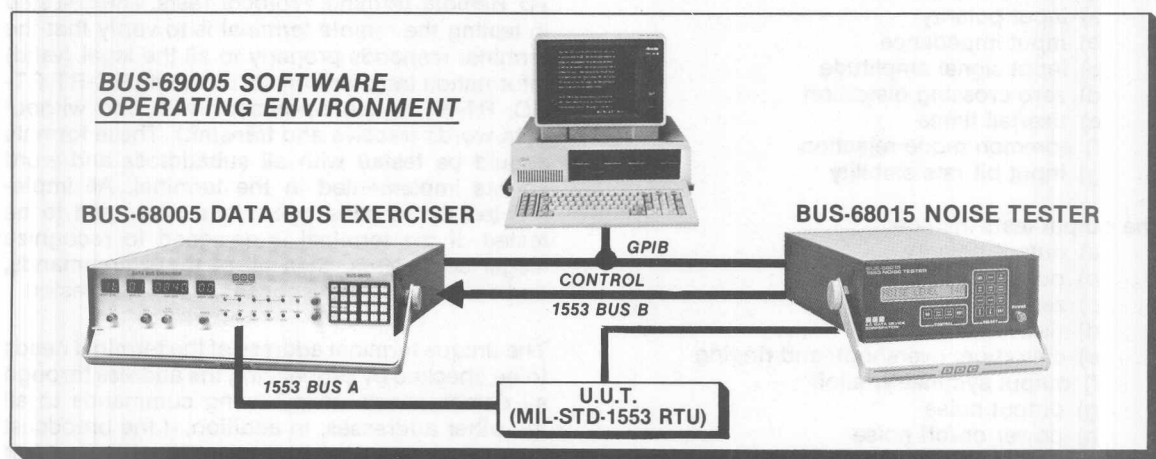
(3) Production Testing. Production testing is generally referred to as "end item" or "acceptance" testing, but can also be applied to in-progress or subassembly items. It is assumed that the design has been previously verified and that this level of testing is performed to verify that all of the circuitry is functioning properly including mode code operation, error message validation, and any other special sequences that can normally be performed. Production testing procedures usually consist of a subset of the design verification tests.

(4) Systems Integration Testing. The purpose of systems level testing is to insure that all elements of the bus network "play" together. This level of

testing is usually centered around the operation of the bus controller's software and its ability to manage the data flow on the bus. This level of testing is generally performed in a Systems Integration Laboratory (see paragraph 6.2 on integration).

(5) Field/Operational Testing. Regardless of the amount of integration testing performed, the final design verification is the actual field/operational testing of the system. Often this is the first time the actual subsystems (as opposed to simulated systems) are interfaced to the bus network. For military applications this level of testing is usually referred to as Development Test/Operational Test (DT/OT). This level of testing is systems oriented and encompasses a total examination of all systems functions from the man/machine interface to the accuracy to the systems performance.

Paragraph 1.6.8 describes the efforts of the Air Force testing program and the development of a series of test plans to cover both the remote terminal and bus controller for validation and production testing. These test plans have been jointly developed by industry and government 1553 experts and should be used as a source of guidance in the areas of circuit design, specification interpretations, and testing procedures.



**1553 SOFTWARE PUTS TEST PLAN UNDER IBM PC® CONTROL.** The BUS-69005 software package provides IBM PC-based ATE control for FULL SAE-AE9 RTU PRODUCTION TEST PLAN, protocol testing with potentially "zero" development time. Utilizing the BUS-68005 MIL-STD-1553 Data Bus Exerciser, BUS-68015 Noise Tester, a GPIB card and a standard IBM PC or compatible, the BUS-69005 delivers comprehensive Production Test Plan customization capability for most RTU configurations within a truly user-friendly, menu-driven operating environment.

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## 6.1.2 Test Requirements

Test requirements for terminals can be divided into two main topics: electrical interface tests (including noise tests), and protocol tests. The electrical interface tests apply to all terminal types (remote terminals, bus controllers, and monitors), whereas the protocol tests are a function of the type of terminal being tested. All tests should be applied to each of the buses when the terminal contains redundant buses. Some of the tests are used to "characterize" the terminal rather than to verify compliance to the standard and the results should be included in the Interface Control Document (see paragraph 3.9). Each of the tests are summarized as follows:

### 6.1.2.1 Electrical Interface Tests

The specifications called out in the standard define the requirements at the connector pins of the terminal. These points are defined by point A in figures 9 and 10 of MIL-STD-1553B. It is important to note that all of the specified requirements are for the terminal itself and are not to be measured with the terminal connected to a system where they would be dependent on other system elements. The electrical interface tests can be subdivided into four parts: input, output, isolation, and noise tests.

The input tests include:

- a) input polarity
- b) input impedance
- c) input signal amplitude
- d) zero crossing distortion
- e) rise/fall times
- f) common mode rejection
- g) input bit rate stability

The output tests include:

- a) output polarity
- b) output amplitude
- c) zero crossing stability
- d) rise/fall times
- e) distortion, overshoot, and ringing
- f) output symmetry/tailoff
- g) output noise
- h) power on/off noise
- i) output bit rate stability

Since terminals functioning as monitors need not be designed with a transmitter, the output tests do not always apply.

The isolation tests are used to verify the input and output isolation between buses in a redundant bus

design. The requirement is given as the ratio in dB between the voltage on the active bus and the voltage on the inactive bus.

The noise rejection tests are required to verify that the terminal exhibits a maximum word error rate of one part in  $10^7$  when operating in the presence of additive white Gaussian noise. The noise test is run continuously until the number of words received by the terminal exceeds the required number for acceptance or is less than the required number for rejection for a particular number of errors. The acceptance/rejection criteria is specified in Table II in the standard. In this test, it is the common practice to gate the noise source off while the terminal responds to the bus tester. This reduces the probability of the status word being "garbled". A typical set up for the noise rejection test is shown in figure 6.1.

### 6.1.2.2 Protocol Tests

The protocol tests are performed as a function of the terminal type. Bus controllers which are also capable of performing as a remote terminal (e.g. while acting as the backup bus controller) need to be tested for both functions. The protocol tests for the remote terminal and bus controller are summarized as follows:

(1) Remote Terminal Protocol Tests. The first step in testing the remote terminal is to verify that the terminal responds properly to all the legal (valid) information transfer formats including BC-RT, RT-BC, RT-RT, mode commands with and without data words (receive and transmit). These formats should be tested with all subaddress and word counts implemented in the terminal. All implemented mode code operations also need to be tested. If the terminal is designed to recognize illegal commands, then all of these commands, and their specified response, need to be tested.

The unique terminal address of the terminal needs to be checked by sequencing the address through all combinations while issuing commands to all the other addresses. In addition, if the broadcast option has been implemented, all of these tests need to be repeated for the broadcast address.

The terminals timing characteristics need to be verified and characterized. This includes the measurement of the status word response time. The terminal should also be tested for its ability to respond to superseding commands.

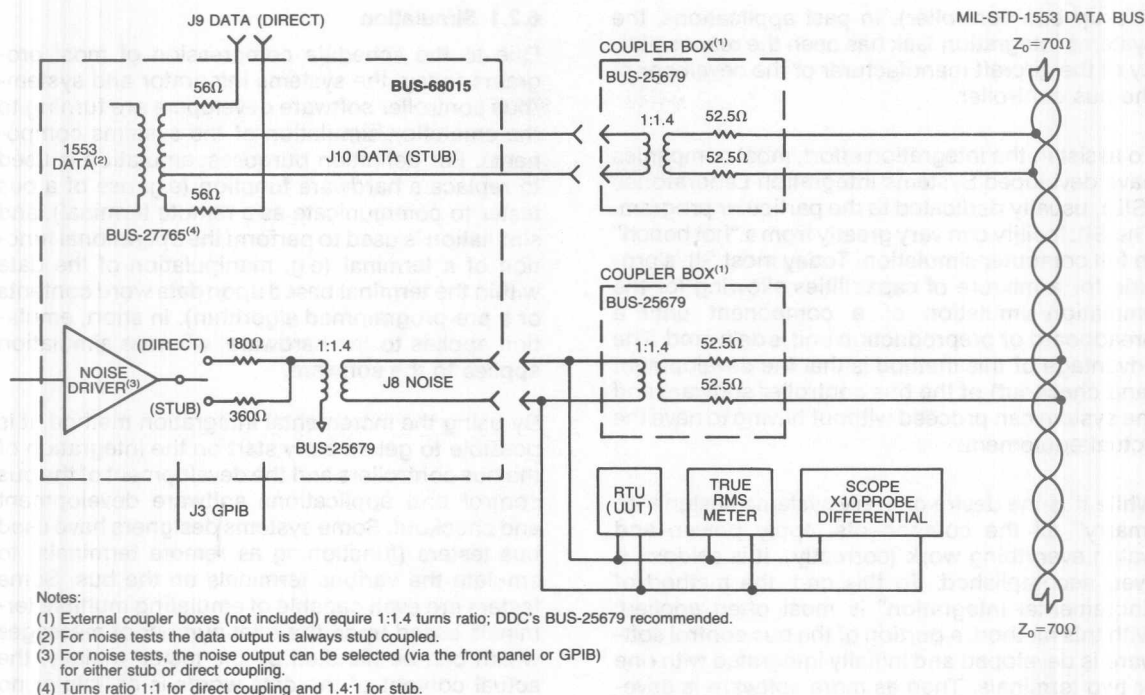


Figure I-6.1 Typical BUS-68015 Based Noise Test

The message validation of the terminal needs to be examined by injecting messages with various error conditions. The validation criteria which needs to be tested includes:

- a) sync errors
- b) encoding errors
- c) bit count errors (word length)
- d) parity errors
- e) word count errors (message length)
- f) gaps (discontinuous data)

(2) Bus Controller Protocol Tests. Testing of the bus controller function requires prior knowledge of the bus controllers software. The first step is to verify that the bus controller is capable of issuing the desired command list and data. This is often difficult to do, especially in systems where events occurring on the bus or data word patterns cause the insertion of various aperiodic messages into the command list. Also an important part of this test is to monitor that the controller never issues invalid commands (1553) OR commands prohibited by the systems specification (i.e. dynamic bus control mode codes). The bus controller must also be tested to insure that it transmits on only one bus at a time.

If possible, the proper processing of the normal valid terminal responses must be tested. The bus controller must also be tested for its processing of abnormal or invalid responses. These may include: no response; improper status bits; word errors (sync, encoding, parity, etc.); discontinuous data words; and word count errors.

The bus controllers timing characteristics also needs to be verified. This includes the minimum intermessage gap and the minimum no response time out. As can be seen, knowledge of the software operation is required in order to perform most of the bus controller protocol tests.

## 6.2 Systems Integration

Systems integration is the process where all of the components (bus controllers, remote terminals, and subsystems) are brought together and "married" into the common bus network. For multilevel or hierarchical networks, this may be first done at the lower bus level and then later combined into the total system. The process almost always includes the "marriage" of the system hardware (bus network) and software (bus controller and

development community. In past applications, the systems integration task has been the responsibility of the aircraft manufacturer or the developer of the bus controller.

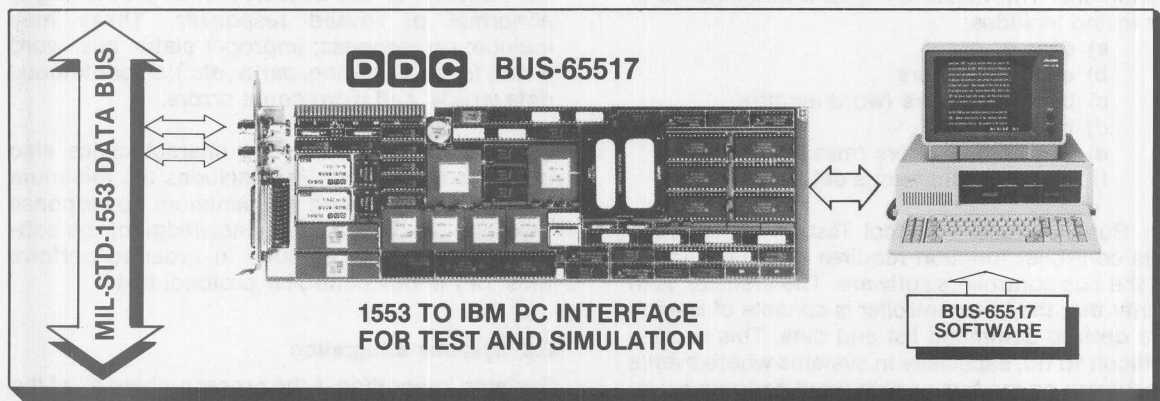
To assist in the integration effort, most companies have developed Systems Integration Laboratories (SIL), usually dedicated to the particular program. The SIL facility can vary greatly from a "hot bench" to full computer simulation. Today most SIL's provide for a mixture of capabilities allowing for the emulation/simulation of a component until a breadboard or preproduction unit is delivered. The advantage of this method is that the development (and checkout) of the bus controller software and the system can proceed without having to have the actual equipment.

While it is the desire of every systems designer to "marry" all the components, apply power, and watch everything work (correctly), it is seldom, if ever, accomplished. To this end, the method of "incremental integration" is most often applied. With this method, a portion of the bus control software is developed and initially integrated with one or two terminals. Then as more software is developed or more terminals are delivered, they are added to the system until at last the entire system has been successfully "married" together.

#### EMULATION

Due to the schedule compression of most programs today, the systems integrator and system-/bus controller software developers are turning to the emulation/simulation of the systems components. For definition purposes: emulation is used to replace a hardware function (e.g. use of a bus tester to communicate as a remote terminal); and simulation is used to perform the operational function of a terminal (e.g. manipulation of the data within the terminal based upon data word contents or a pre-programmed algorithm). In short, emulation applies to the hardware, whereas simulation applies to the software.

By using the incremental integration method, it is possible to get an early start on the integration of the bus controllers and the development of the bus control and applications software development and checkout. Some systems designers have used bus testers (functioning as remote terminals) to emulate the various terminals on the bus. Some testers are even capable of emulating multiple terminals based upon the total number of messages which can be handled by the tester. Initially, the actual content of the data words is of little or no importance and therefore they can be set to random or constant data patterns or be set to incrementally change for each message transmission.



**COMPLETE 1553 TEST AND SIMULATION UNDER IBM PC® CONTROL.** The new MIL-STD-1553 integrated card and software development package, is designated the BUS-65517. Completely contained on a single IBM PC compatible full-slot card, with companion software disk, the BUS-65517 is a versatile workstation for the Integrated Development, Emulation and Analysis (I.D.E.A.) of MIL-STD-1553 systems. The BUS-65517 simultaneously simulates a Bus Controller, 31 Remote Terminals and an active Monitor. In addition, the BUS-65517 provides comprehensive Error Injection capabilities with bit/word resolution.

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tion will allow for the injection of errors in the messages and allow for the verification of the bus controllers error handling and recovery procedures.

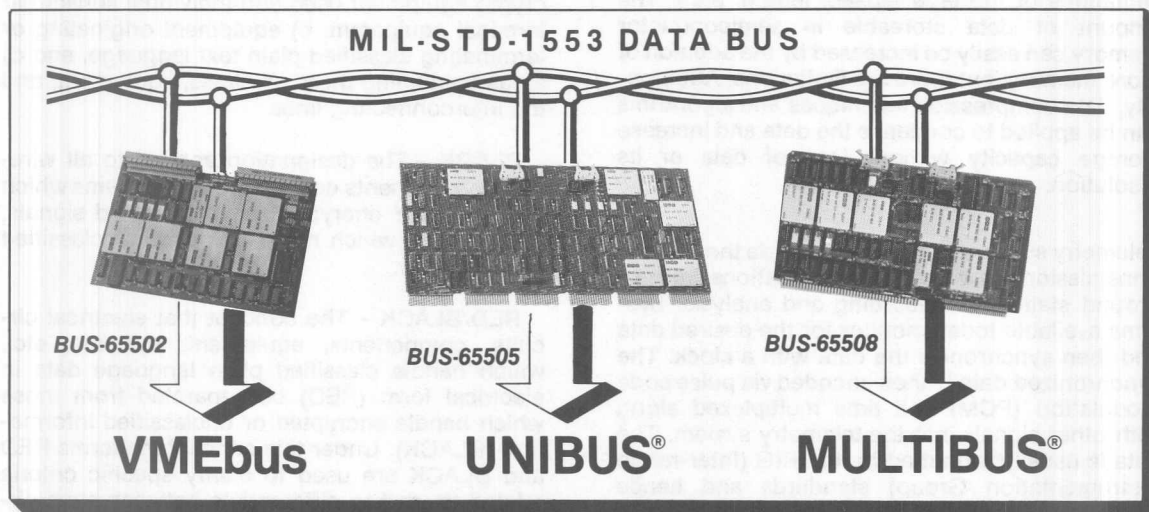
As the integration and software development progress, the content of the data words will start to become of some importance, especially to the applications programs. Some of the bus tester have limited processing capability which would allow for the movement of data between buffers or simple operations upon the data. For some terminals, this level of simulation may be sufficient. However, for the more complex subsystems and terminals, it may be necessary to go to a bigger computer with more computational power. To this end, several manufacturers have developed 1553 cards which interface to mini/micro computer backplanes (e.g. LSI-11, PDP-11, VAX, NOVA, Eclipse, S.E.L., Multibus) and interface via DMA techniques to the computer. This allows for some large applications simulation programs (i.e. aircraft flight characteristics, navigational models, etc.) to be developed on the host computer and the

transmitted on the bus when commanded.

This simulation method can be used until actual hardware is available or until it is necessary to install the components on the aircraft or platform. Most systems integrators retain the SIL facility for use in solving system problems encountered during DT/OT and for the integration of future additions to the system.

### 6.3 Instrumentation

The ultimate systems test is DT/OT testing. Whether the application is airborne or ground based, this is often the first time some of the platform or mission equipment (e.g. engines, sensors, weapons systems, etc.) are connected to the bus network. It is also during the DT/OT phase that the customer evaluates the performance of the product. Therefore, it is necessary in the effort of continued systems integration or performance evaluation to monitor and collect data from the bus network. In addition to the testing phase, some applications continuously monitor certain bus



**INTERFACE CARDS ADD 1553 I/O TO POPULAR COMPUTERS.** DDC offers a full line of MIL-STD-1553 BC/RTU/MT cards to interface the 1553 serial MUX bus to the most popular computer buses. These cards provide software selectable BC, RTU, or MT operation; support all 1553 message formats, 12 mode codes, and have complete built-in-test capabilities. Each card includes a 4K x 16 dual port RAM to store 1553 messages and commands, thereby reducing subsystem processor overhead. All 1553 functions, including address recognition, Manchester coding validation, and mode code response, are supported transparent to the processor. Whatever your requirement, you can depend on DDC to satisfy it with an easy to use, cost effective computer interface card.

parameters as part of the vehicle/platform maintenance activity.

For validation and testing purposes, it is often necessary to collect one hundred percent of the data bus traffic. Today, bus monitors exist which are capable of extracting all data or being programmed to collect only certain messages to selective terminal addresses and subaddresses or error conditions.

Since 1553 is a one megabit asynchronous bus, the high speed (compared to other platform functions) and non-synchronous nature of the data traffic present particular problems in the acquisition and analysis of the data. There are two primary methods for acquiring and storing this data: on board bulk storage, and telemetry.

On board bulk storage is performed by means of magnetic tape or semiconductor memory. High density, multitrack tape has advantages of allowing the data bus to be recorded and synchronized to a clock. Its obvious disadvantage is the amount of data which can be acquired due to the time limitations of the tape (speed, length, etc.). The amount of data storeable in semiconductor memory can easily be increased by the addition of more memory, but there are limitations. Additionally, data compression techniques and algorithms can be applied to condense the data and increase storage capacity without loss of data or its resolution.

Telemetry systems collect and encode the data for transmission, via a radio communications link, to a ground station for recording and analysis. Systems available today monitor for the desired data and then synchronize the data with a clock. The synchronized data is then encoded via pulse code modulation (PCM) and time multiplexed along with other signals into the telemetry system. The data is usually formatted to the IRIG (Inter-range Instrumentation Group) standards and hence existing ground receiving equipment can handle the decommutation of the data.

The instrumentation of the data bus needs to be addressed as part of the overall testing and systems integration activities. The systems designer needs to analyze and identify the signals with need to be monitored such that an adequate instrumentation package can be designed.

## 7.0 Other Issues

### 7.1 Network System Security

The application of multiplex data bus networks to military aircraft has provided for a significant level of subsystems and data integration, expanding the capabilities of the avionics systems. In doing so, the "old" techniques of maintaining data security by using only discrete electronics systems and wiring is no longer possible without sacrificing many of the benefits of multiplex systems integration. Therefore, military data bus network designers must address the maintenance of data security within this integrated avionics system for both flight and ground operations.

#### 7.1.1 Definitions

In order to provide a common lexicon from which to work with, the following definitions are provided.

**RED** - A designation applied to: a) all wirelines within the terminals or data routing equipment carrying classified plain language, b) all wirelines between the unencrypted side of the on-line crypto equipment used and individual subscriber terminal equipment, c) equipment originating or terminating classified plain text language, and d) areas containing these wirelines, equipment, and the interconnecting lines.

**BLACK** - The designation applied to all wirelines, components equipment, and systems which handle ONLY encrypted or unclassified signals, and areas to which no unencrypted or classified signals occur.

**RED/BLACK** - The concept that electrical circuits, components, equipment, systems, etc., which handle classified plain language data in electrical form (RED) be separated from those which handle encrypted or unclassified information (BLACK). Under this concept the terms RED and BLACK are used to clarify specific criteria related to, and to differentiate between such circuits, components, equipment, and systems, etc., and the area in which they are contained.

**TEMPEST** - An unclassified short name referring to investigations and studies of compromising emanations. It is sometimes used synonymously for the term "compromising emanations" (e.g. TEMPEST tests, TEMPEST inspections, TEMPEST control plan).

### 7.1.2 System Security Policy

The design (system, hardware, and software) must fulfill the operational, maintenance, and logistic security policy of the aircraft, ship, or system, on which it is used. This policy is established by the government program manager in conjunction with the operational user. The details of this policy which impact system designers are provided in the program security classification guide and its references.

Some major areas capable of impacting the design are:

- a) The maximum classification of the data processed by each of the systems using the bus.
- b) The maximum classification and compartmentalization of the data transferred via the bus.
- c) The maximum authorized classification and compartment level of the systems connected to the bus.
- d) The access authorization of the various crew and maintenance personnel who will be using systems connected via the bus.

### 7.1.3 System Security Architecture

The data bus network operates as a time shared system between various processors and users of the data. If any of these subsystems process RED information, then the data bus network design must address three complementary security areas: 1) compromising emanations (i.e. TEMPEST), 2) encryption, and 3) trusted message routing and control. Each of these areas interacts with the other, and the system designer must determine the optimum combination to satisfy the security requirements.

System security architectures, each with different advantages and disadvantages, are:

- 1) All BLACK bus - No RED data or RED data processor is directly connected to the bus.
- 2) All RED bus - All systems connected to the bus are authorized access to the highest data classification and all compartments using the bus.
- 3) RED/BLACK Gateway - Separate all RED and all BLACK buses, as defined above, are used with a gateway to allow necessary data to securely pass between them.
- 4) RED/BLACK Composite - On a time-share basis, the bus processes RED and BLACK data between RED and BLACK subsystems securely.

### 7.1.4 TEMPEST Design

TEMPEST requirements must be fulfilled by the bus interface circuitry and the transmission media (bus network) for data bus systems processing RED information. The data bus network shall fulfill the TEMPEST provisions of the following documents:

- 1) NACSIM-5100 and NACSIM-5112 for U.S. Military Systems.
- 2) BID/01/202 (4) and BID/01/200 (Series) for United Kingdom Military Systems.
- 3) AMSG-719 and AMSG-720 for NATO Military Systems.
- 4) Equivalent national requirements for other national military systems.

### 7.1.5 Encryption Designs

Encryption techniques may be used by the data bus network and its associated terminals and processor to convert RED data into BLACK data and to isolate multiple classification levels and compartments of RED data. The specific encryption technique and system design must be approved by the government agency responsible for encryption certification. While a discussion of specific acceptable encryption techniques is beyond the scope of this Designer's Guide and is classified, any encryption design for military systems must include the following:

- 1) TEMPEST design to preclude compromising emanations from by passing the encryption circuitry.
- 2) Trusted design of the encryption control, input/output and data processing circuitry, and software to preclude information compromise through failure or manipulation.
- 3) Cryptographic key management, coordination, distribution, and zeroize techniques, circuitry and software.
- 4) Synchronization and timing protocols.
- 5) Encryption alarm and alarm check techniques.

### 7.1.6 Trusted Message Routing and Control Design

The data bus network design must fulfill the requirements of DoD 5200.28-STD, "Department of Defense Trusted Computer System Evaluation Criteria", or national equivalent, with less than one undetected control error per 10,000 hours of operation at the maximum bus message transfer rate. Corrective control action to maintain and restore

system trust must be incorporated for detected system security failures.

The data bus network can be designed to meet these requirements by using the following:

- 1) Low bit error rate circuitry and cabling techniques.
- 2) Parity coding of control words involved in message routing.
- 3) Bus controller monitor to detect and correct message routing errors.

Each of the System Security Architectures, as defined in the previous sections, have individual TEMPEST, encryption, isolation, and Trusted Computer System requirements for the data bus network's transmissions media, terminal and controller designs, and gateway designs. Designers are directed to their Program's Security Classification Guide, DoD 5200.28-STD, and the TEMPEST provisions in the aforementioned documents for assistance in determination of the design requirements.

## **7.2 MIL-STD-1760A Interconnect Standard for Aircraft Stores**

MIL-STD-1553B, due to its maturity and adaptability, has found itself being used, either in total or parts thereof, in other standards and specifications within various military architectures. One such adaptation has been to MIL-STD-1760A. In addition to the adoption of 1553B, new hierarchical multilevel bus network architectures are being developed and imposed with this new standard. For this reason, an overview of 1760A, and supporting specifications is presented here. Current status of the 1760A standard includes Notices 2 and 3.

### **7.2.1 Definitions**

MIL-STD-1760A defines the electrical signal characteristics, connectors, and interface software (messages) for US/NATO aircraft and stores. For definition purposes, a store is defined as any external device attached to the aircraft and is composed of devices which separate (leave the aircraft) such as a missiles and bombs, and as permanent modules such as electronics pods (e.g. ECM, LAN-TIRN, etc.) or fuel tanks. Retrofit systems employing 1760A stores include existing aircraft such as the F-5E, F-16A/B, B-52G/H, and the B-1B. 1760A stores will also be designed into the new ATA, ATF, and LHX aircraft.

The control path for these stores is a MIL-STD-1553B data bus. However, there are restrictions, selected options, and exceptions to 1553B taken within 1760A to meet the aircraft/stores interoperability that requires attention by system designers.

MIL-STD-1760A defines a Mission Stores Interface (MSI) as a single electrical receptacle external to the store structure. The aircraft connection is defined as the Aircraft Station Interface (ASI). Connection point examples are pylons, fuselage hard points, internal weapons bays, and wing tips. Umbilical cables connect the aircraft ASI to the store MSI. Figure I-7.1 illustrates a weapon attached to an ejector (suspension and release equipment) which is attached to a wing pylon. The primary 1760A signal set is available at the pylon ASI and connects to the store via the umbilical to the MSI. Each store uses selected signals from the available set as required. A carriage store is a device that attaches a Carriage Store Interface (CSI) to a single weapon station ASI and can interface with multiple mission stores.

In 1760A, no spare pins are available to aircraft or store designers. All interface pins in the connector are fully defined. Instead of unique signals over dedicated wires, data in 1553 word format is transmitted over a 1553 dual redundant standby bus network.

Mission stores contain embedded 1553 remote terminals. Per the standard, mission stores must be capable of BC-RT, RT-BC, and RT-RT message transfers. 1760A allows for both normal 1553 bus communication protocol (command/response), and broadcast message protocol. **The aircraft has the responsibility to function as the bus controller.** Due to the safety critical nature of stores, dynamic bus control is prohibited from use on a 1760A bus network.

### **7.2.2 Restrictions**

Subaddress assignments were defined in Notice 2 and 3 (see paragraph 3.7.1 on subaddressing). Defined subaddresses include: a) store identification, b) test operations, c) nuclear store operations, d) control and monitoring, and e) mass data transfer. As in 1553B both mode code indicators (00000 and 11111) are required. Mission store terminals are required to implement the transmit status word, reset remote terminal, transmitter shutdown, override transmitter shutdown, transmit vector word, synchronize with data word, and transmit last command word mode codes. If the





terminal flag bit is implemented, then the inhibit terminal flag mode code is required. In addition, if the service request bit is used, the data word associated with the transmit vector word mode code must be available when the bit is set. The setting of the subsystem flag bit is interpreted as a total loss of the store.

MIL-STD-1760A imposes a 30 word limit on both transmit and receive messages to/from a store (see paragraph 3.4 on gates). The use of checksums in the data message is optional except for: a) store identification messages, b) mission control and monitoring messages, and c) mass data transfer messages.

Store initialization sequences were defined in Notices 2 and 3. The initialization procedure imposes on the network bus controller a message timing sequence to first communication no sooner than 150 milliseconds for first status response (with potential for the busy bit to be set in the status word) and up to 500 milliseconds for response of a valid store identification message. The timing reference point is 100 milliseconds after the application of power to the store (115/120V ac and 28V dc power #1). The 30 word identification message consists of: a) a one word header with a fixed hexadecimal pattern of 0421, b) a one word country code, c) nine words of upper case ASCII representation of the store number (e.g. AGM-131), d) eighteen words of null characters, and e) one word of the checksum value for the message.

### 7.2.3 MIL-STD-1760A Signals Related to 1553B

Figure I-7.2 shows the interface signals related to the data bus system. Mux A and mux B are the 1553 transformer coupled stubs from the aircraft. The address and odd parity bits are for wiring the unique remote terminal address which is established at the ASI connector. It is permissible for stores to latch the address upon initialization rather than continuously reading it. Store implementing Notice 3 control messages (critical control 1 word 4 and critical control 2, word 6) MUST also read the terminal address and set the value in the Address Confirm field (bits 11-15) in each word of the message.

As shown in figure I-7.2, the aircraft determines the stores presence by monitoring the interlock circuitry. The store is designed to jumper the interlock signal to the interlock return signal. The circuit is broken when the store separates. The store is not permitted to use the interlock signals to determine

the aircraft's presence. The store may use the terminal address lines to determine if the aircraft is present (attached). However, since a single fault failure is possible at the address interface, **the store designer should not allow safety critical functions to occur based solely upon detection of the no aircraft.**

Enabling of release consent is used to signal to the store that safety critical messages arriving via the data bus are to be acted upon as valid consent from the aircraft (crew). Safety critical events include irreversible functions such as rocket motor ignition, suspension hook release, and deployment of chutes and fins. 1760A allows 10 milliseconds for the consent signal stabilization before the messages start arriving. The return reference for release consent is the return of dc power #2.

### 7.2.4 Data Bus Networks and Components

The network configuration depends upon the mission. The initial store load determines the number of remote terminals to be connected to the weapons network. During flight weapons are expended and removed from the bus. Since the number of remote terminals is changing, the bus loading and network reflections is also changing. Improper store separation may physically damage the umbilical. Hot rocket exhaust plume potentially could cause multiple shorts on the bus, hampering communications with the remaining stores. Since ASI and MSI connectors and umbilicals are exposed to extreme physical environments, the stubs are more likely to experience shorts than the network contained within the aircraft fuselage. Therefore, the systems designer must take special precautions when designing 1760A bus networks.

Transformer coupled stubs are required for all connections in 1760A. **To be interoperable to all stores, the aircraft coupler transformer should not be center tapped on the stub side.** In order to support multiple aircraft store stations without routing the bus, coupler boxes with five to eight transformer coupled stubs are now available. This allows the bus to remain in a more protected environment, such as inside the fuselage or wing, and branch out with stubs to a cluster of external connectors at the stations.

Transceiver output voltage for the stores is set at a minimum of 20 volts when measured at the MSI; two volts higher than the 1553B minimum. This additional requirement on transceivers is necessary since the network paths vary from aircraft to

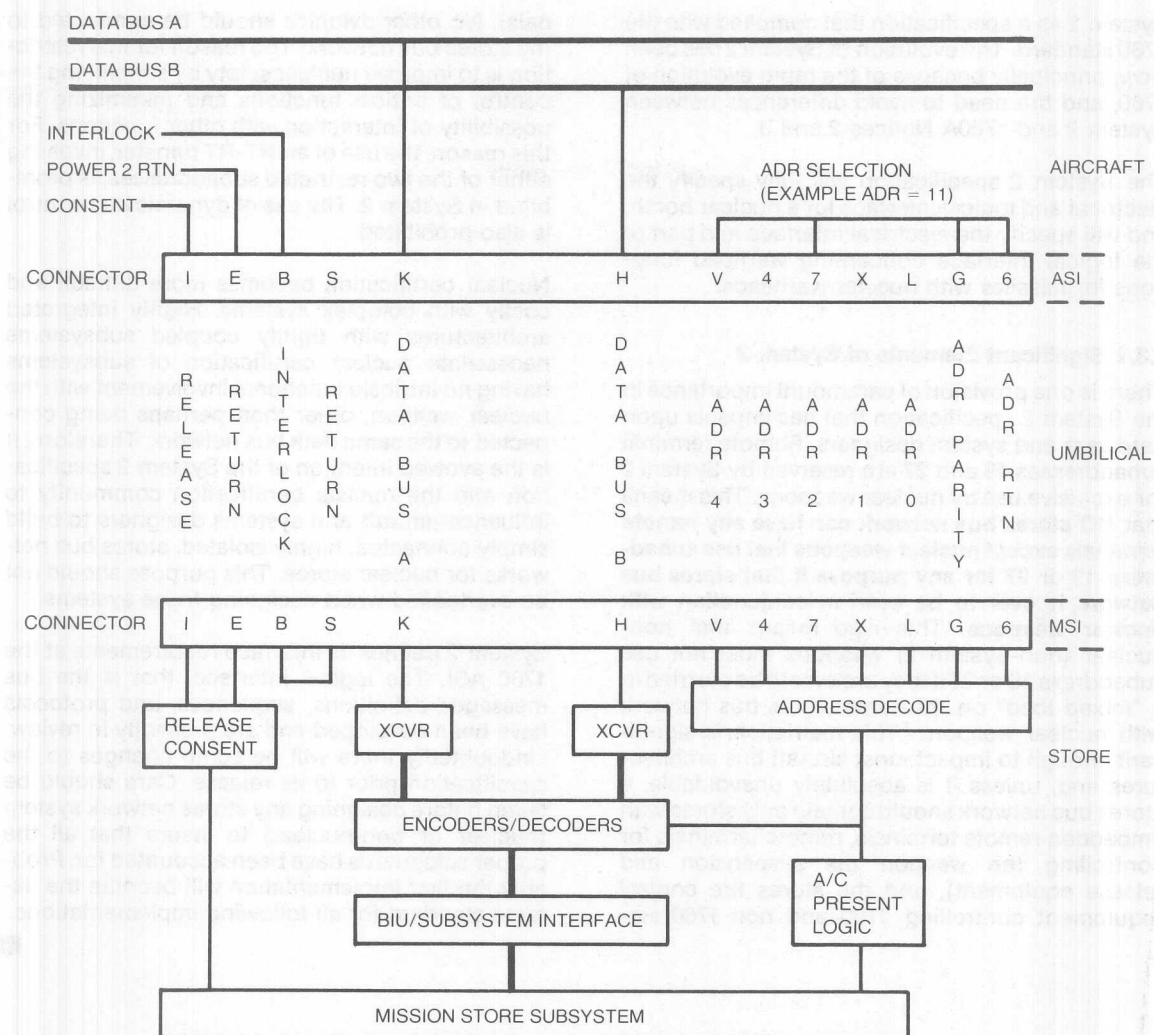


Figure I-7.2 1553B Signals in 1760A

aircraft and station to station. The ASI and MSI also cause network breakpoints that are not usually made for stubs. Constant voltage transceivers will provide a tighter control of output voltage (as opposed to constant current transceivers) as the network load changes. Current limiting of the transceiver output stage provides protection against multiple high loads on the network.

Twinax connector design is required in 1760A for both data bus signals (A and B). The coaxial data high, data low, and shield provides a protection from the electromagnetic environment (EMI, EMP, and lighting).

### 7.3 System 2

System 2 is a specification conforming to MIL-STD-1760A covering the interface between an aircraft and a nuclear weapon. Publication of the System 2 specification has not yet occurred (7/87). Therefore it is not possible to definitively present and explain its implications. But there is a need for aircraft, fire control, and weapons manufacturers and designers to understand the requirements and goals of this specification. The development of System 2 goes back as far as the development of MIL-STD-1760. Early in the development stage of both documents, the decision was made to keep

1760 standard. The evolution of System 2 has been slow, principally because of the rapid evolution of 1760, and the need to avoid differences between System 2 and 1760A Notices 2 and 3.

The System 2 specification will fully specify the electrical and logical interface for a nuclear bomb, and will specify the electrical interface and part of the logical interface concerning warhead functions for missiles with nuclear warheads.

### 7.3.1 Significant Elements of System 2

There is one provision of paramount importance in the System 2 specification that has impacts upon hardware and system designers. Remote terminal subaddresses 19 and 27 are reserved by System 2 for exclusive use by nuclear weapons. This means that **NO stores bus network can have any remote terminals except nuclear weapons that use subaddress 19 or 27 for any purpose if that stores bus network is ever to be used in conjunction with nuclear weapons.** This also means that non-nuclear (non-System 2) weapons must not use subaddress 19 or 27 if they are ever to be carried in a "mixed load" on the same stores bus network with nuclear weapons. This restriction is significant enough to impact most aircraft bus architectures and, unless it is absolutely unavoidable, a stores bus network should contain only stores with embedded remote terminals, remote terminals for controlling the weapon (its suspension and release equipment), and the stores fire control (equipment controlling 1760 and non-1760 sig-

the stores bus network. The reason for this restriction is to improve nuclear safety by simplifying the control of critical functions and minimizing the possibility of interaction with other functions. For this reason, the use of an RT-RT transfer, involving either of the two restricted subaddresses, is prohibited in System 2. The use of dynamic bus control is also prohibited.

Nuclear certification becomes more difficult and costly with complex systems. Highly integrated architectures with tightly coupled subsystems necessitate nuclear certification of subsystems having no intrinsic functional involvement with the nuclear weapon, other than perhaps being connected to the same data bus network. Therefore, it is the avowed intention of the System 2 specification and the nuclear certification community to influence aircraft and systems designers to build simply connected, highly isolated, stores bus networks for nuclear stores. This purpose should not be overlooked when designing these systems.

System 2 defines its interface requirements at the 1760 ASI. The logical interface, that is the bus messages definitions, sequences, and protocols have been developed and are presently in review. Undoubtedly there will be some changes to the specification prior to its release. Care should be taken before designing any stores network system (nuclear or non-nuclear) to insure that all the proper safeguards have been accounted for. Probably the first implementation will become the de-facto standard for all following implementations.



## 11

## II. REVIEW AND RATIONALE OF MIL-STD-1553A AND MIL-STD-1553B.

*This section is an explanation of each part of MIL-STD-1553B on a paragraph-by-paragraph basis. The descriptions include (1) rationale for the requirements specified; (2) the requirements; and (3) identification of differences between MIL-STD-1553A and MIL-STD-1553B. The 1553B part that is discussed is presented first (indented as below), followed by the rationale, explanations, and differences from 1553A.*

### 1. SCOPE

**1.1 Scope.** This standard establishes requirements for digital, command/response, time division multiplexing (Data Bus) techniques on aircraft. It encompasses the data bus line and its interface electronics illustrated on figure 1, and also defines the concept of operation and information flow on the multiplex data bus and the electrical and functional formats to be employed.

**1.2 Application.** When invoked in a specification or statement of work, these requirements shall apply to the multiplex data bus and associated equipment which is developed either alone or as a portion of an aircraft weapon system or subsystem development. The contractor is responsible for invoking all the applicable requirements of this Military Standard on any and all subcontractors he may employ.

*Additional sentences were added to 1553B to clarify designer selected options. The basic difference between 1553A and 1553B is that in 1553B the options are defined rather than being left for the user to define as required. It was found that when the standard did not define an item, there was no coordination in its use. Hardware and software had to be redesigned for each new application. Therefore, the one primary goal of 1553B was to provide flexibility without creating new hardware and software designs for each new user. This was accomplished by specifying the "use of" rather than the requirement "to use" in the functional areas and by specifying the electrical interfaces explicitly so that compatibility between designs by different manufacturers could be electrically interchangeable.*

### 2. REFERENCED DOCUMENTS

**2.1 Issue of document.** The following document, of the issue in effect on date of invitation for bid or request for proposal, forms a part of the standard to the extent specified herein.

### SPECIFICATION

#### MILITARY

**MIL-E-6051** Electromagnetic Compatibility Requirements, Systems

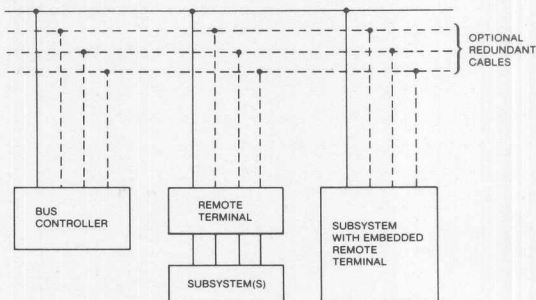


Figure 1 of 1553B. Sample Multiplex Data Bus Architecture

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

*The only difference between the two revisions was that in 1553B the references to MIL-STD-461 and MIL-STD-462 were removed (i.e., both electromagnetic interference requirements and measurement standards). MIL-E-6051 "System Electromagnetic Compatibility Requirements" is still applicable in 1553B to define the wiring and cabling provisions of the specification (see MIL-STD-1553B, paragraph 4.5.1.1.5.3).*

*The definition section of the standard has been expanded and reordered in 1553B. The purpose for the change was to address definitions in order of complexity and to describe new functions, modes, and devices. A comparison of the definition included in 1553A and 1553B is presented in table II-1.*

### 3. Definitions

**3.1 Bit.** Contraction of binary digit: may be either zero or one. In information theory a binary digit is equal to one binary decision or the designation of one or two possible values of states of anything used to store or convey information.

**3.2 Bit rate.** The number of bits transmitted per second.

**3.3 Pulse code modulation (PCM).** The form of modulation in which the modulation signal is sampled, quantized, and coded so that each element of information consists of different types or numbers of pulses and spaces.

**3.4 Time division multiplexing (TDM).** The transmission of information from several signal sources through one communication system with different signal samples staggered in time to form a composite pulse train.

**3.5 Half duplex.** Operation of a data transfer system in either direction over a single line, but not in both directions on that line simultaneously.

**3.6 Word.** In this document a word is a sequence of 16 bits plus sync and parity. There are three types of words: command, status and data.

**3.7 Message.** A single message is the transmission of a command word, status word, and data words if they are specified. For the case of a remote terminal to remote terminal (RT to RT) transmission, the message shall include the two command words, the two status words, and data words.

**3.8 Subsystem.** The device or functional unit receiving data transfer service from the data bus.

**3.9 Data bus.** Whenever a data bus or bus is referred to in this document it shall imply all the hardware including twisted shielded pair cables, isolation resistors, transformers, etc., required to provide a single data path between the bus controller and all the associated remote terminals.

**3.10 Terminal.** The electronic module necessary to interface the data bus with the subsystem and

Table II-1. Comparison of MIL-STD-1553A and MIL-STD-1553B Definitions

MIL-STD-1553A definitions (paragraph number)		MIL-STD-1553B definitions (paragraph number)	
Bit	(3.2)	Bit	(3.1)
Bit rate	(3.3)	Bit rate	(3.2)
Pulse code modulation	(3.4)	Pulse code modulation	(3.3)
Time division multiplexing	(3.5)	Time division multiplexing	(3.4)
Half duplex	(3.7)	Half duplex	(3.5)
Word	(3.10)	Word	(3.6)
Message	(3.11)	*Message	(3.7)
—		**Subsystem	(3.8)
Data bus	(3.12)	*Data bus	(3.9)
—		**Terminal	(3.10)
Bus controller	(3.13)	*Bus controller	(3.11)
—		**Bus monitor	(3.12)
Remote terminal	(3.1)	*Remote terminal	(3.13)
Asynchronous operation	(3.8)	Asynchronous operation	(3.14)
Dynamic bus allocation	(3.9)	Dynamic bus control	(3.15)
Command or response mode	(3.6)	Command or response mode	(3.16)
—		**Redundant data bus	(3.17)
—		**Broadcast	(3.18)
—		**Mode code	(3.19)

\*Definition changed significantly.

\*\*Not previously defined.

the subsystem with the data bus. Terminals may exist as separate line replaceable units (LRU's) or be contained within the elements of the subsystem.

*This definition of terminal is intentionally broad. Terminals in 1553 have common operational characteristics, as well as assigned roles in data bus operation. The three allowable roles are defined in 3.11, 3.12, and 3.13. Common operational requirements of terminals are given in 1553B, paragraph 4.4.1. Note that the definition gives designers complete freedom of functional partitioning of the operating parts of a terminal, and that there is also no restriction of physical partitioning.*

**3.11 Bus controller.** The terminal assigned the task of initiating information transfers on the data bus.

**3.12 Bus monitor.** The terminal assigned the task of receiving bus traffic and extracting selected information to be used at a later time.

**3.13 Remote terminal (RT).** All terminals not operating as the bus controller or as a bus monitor.

**3.14 Asynchronous operation.** For the purpose of this standard, asynchronous operation is the use of an independent clock source in each terminal for message transmission. Decoding is achieved in receiving terminals using clock information derived from the message.

*This definition refers to the electrical characteristic by which the timing of message bits in a word are decoded. This use of "asynchronous operation" should not be confused with an asynchronous message that may interrupt or suspend the transmission of synchronous (i.e., periodic) messages in an avionics system.*

**3.15 Dynamic bus control.** The operation of a data bus system in which designated terminals are offered control of the data bus.

**3.16 Command/Response.** Operation of a data bus system such that remote terminals receive and transmit data only when commanded to do so by the bus controller.

*In the case of the definitions for message, bus controller, remote terminal, asynchronous operation, dynamic bus control, and command/response, the change from 1553A to 1553B was developed to produce a more general definition. However, in the definition of data bus, 1553B encompasses more equipment. Instead of*

*including only the wire, the data bus couplers are also included. Two definitions were added for clarity: subsystem and terminal. The others (bus monitor, redundant data bus, broadcast, and mode codes) were added to define the additional requirements stated in 1553B. The function of a bus monitor is to monitor the data bus and record specified bus activity. The objective of defining a bus monitor function is new to 1553B. Two basic capabilities have been identified for the monitor in paragraph 4.4.4 of 1553B: (1) an offline application including a flight test recording, maintenance recording, or mission analysis, and (2) a unique data bus terminal, which provides an internal backup bus controller function, with sufficient information to take over as the active bus controller in the event of a switchover or a failure of the active bus controller. In these two roles, the bus monitor hardware may have the performance capability of a terminal (unique address) or may be attached to the data bus without the knowledge of the other bus users (including the bus controller). In this second approach, no bus communication from or to the bus monitor by the bus controller is possible. The bus monitor acts as a passive listener to the specified traffic it is assigned to record. Obviously, the performance of a bus monitor requires the monitoring of the data bus for command words, status words, and data words. From this monitoring, the specific message collection process can occur during normal and abnormal (bus error and recovery) bus traffic. To aid in accomplishing the detection of these words (command and status), the optional instrumentation bits (bit 10 in the status word) and the associated bit in the command word (bit 10) can be set to a logic 1 and a logic 0, respectively.*

**3.17 Redundant data bus.** The use of more than one data bus to provide more than one data path between the subsystem, i.e., dual redundant data bus, tri-redundant data bus, etc.

*The redundant data bus definition was added to 1553B to identify a particular approach for obtaining multiple data paths to improve message arrival probability. Paragraph 4.6 of 1553B discusses the use of a dual-redundant data bus where the operation is identified as dual standby. In this mode, only one bus is active at any given time, except when superseding commands are sent on the standby bus. Under this condition, the terminal responds to the most recent command.*

**3.18 Broadcast.** Operation of a data bus system such that information transmitted by the bus



controller or a remote terminal is addressed to more than one of the remote terminals connected to the data bus.

*The broadcast definition has been added to 1553B to describe a new protocol option. The use of this protocol allows a bus controller or a remote terminal to address more than one terminal connected to the system. This is accomplished by transmitting a dedicated terminal address (11111) and each receiver withholding the normal status word response.*

**3.19 Mode code.** A means by which the bus controller can communicate with the multiplex bus related hardware, in order to assist in the management of information flow.

*The mode code definition was added to 1553B because of the definition of several mode code operations in paragraph 4.3.3.5.1.7. These optional mode codes are used to manage the information transfer system. The basic philosophy of the data bus system is that it is a "transparent data communication link." This means that its operation and management does not involve the use of the sensor data that it is transmitting or receiving. However, overhead is required to manage such a data link. Therefore, command words, status words, and message gaps are required to provide this capability. The combination of command word, mode codes, and responses to these mode codes provide the basis for managing the multiplex system.*

#### 4. GENERAL REQUIREMENTS

*Several paragraphs have been added, changed, and renumbered in the requirements section of 1553B compared to 1553A.*

**4.1 Test and operating requirements.** All requirements as specified herein shall be valid over the environmental conditions which the multiplex data bus system shall be required to operate.

*This new paragraph of the 1553B was added to indicate that the performance requirements specified in this standard shall apply over the environmental conditions in which the multiplex data bus system shall be required to operate. It is anticipated that for most military applications this will be described by MIL-E-5400 Class II and some nuclear-hardening specifications. Because of the diversity of environmental conditions, the standard does not specify these requirements. Therefore, the system designer must determine, from appropriate vehicles or system*

*specifications, the environmental conditions imposed on the multiplex data bus system.*

**4.2 Data bus operation.** The multiplex data bus system in its most elemental configuration shall be as shown on figure 1. The multiplex data bus system shall function asynchronously in a command/response mode, and transmission shall occur in a half-duplex manner. Sole control of information transmission on the bus shall reside with the bus controller, which shall initiate all transmissions. The information flow on the data bus shall be comprised of messages which are, in turn, formed by three types of words (command, data, and status) as defined in 4.3.3.5.

*This paragraph is identical to paragraph 4.1 in 1553A with the exclusion of the reference to electromagnetic compatibility, which appears in paragraph 4.5.1.1.5.3 of 1553B.*

#### 4.3 Characteristics

**4.3.1 Data form.** Digital data may be transmitted in any desired form, provided that the chosen form shall be compatible with the message and word formats defined in this standard. Any unused bit positions in a word shall be transmitted as logic zeroes.

**4.3.2 Bit priority.** The most significant bit shall be transmitted first with the less significant bits following in descending order of value in the data word. The number of bits required to define a quantity shall be consistent with the resolution or accuracy required. In the event that multiple precision quantities (information accuracy or resolution requiring more than 16 bits) are transmitted, the most significant bits shall be transmitted first, followed by the word(s) containing the lesser significant bits in numerical descending order. Bit packing of multiple quantities in a single data word is permitted.

*This paragraph is identical to paragraph 4.2 in 1553A with the additional capability in paragraph 4.3.2 of 1553B concerning bit-packing of multiple quantities.*

*Bit-packing is a method used to improve transmission efficiency when subsystem data, which contain less than 16 bits of information per parameter (word), are collected and distributed in one word or message. Single-bit data and other parameters that are characterized by bit patterns of fewer than 16 bits will not fill the 16 bits of data allowed in 1553 data word format. Two approaches are used to utilize all bits in a word: (1) packing multiple parameters and words and (2) filling in zeros for all unused bits. In the*

first approach, the encoding and decoding cost must be considered, while in the second approach the inefficiency of sending as little as one bit per word must be considered.

### 4.3.3 Transmission Method

**4.3.3.1 Modulation.** The signal shall be transferred over the data bus in serial digital pulse code modulation form.

*This paragraph remained unchanged in both revisions of the standard.*

**4.3.3.2 Data code.** The data code shall be Manchester II bi-phase level. A logic one shall be transmitted as a bipolar coded signal 1/0 (i.e., a positive pulse followed by a negative pulse). A logic zero shall be a bipolar coded signal 0/1 (i.e., a negative pulse followed by a positive pulse). A transition through zero occurs at the midpoint of each bit time (see figure 2).

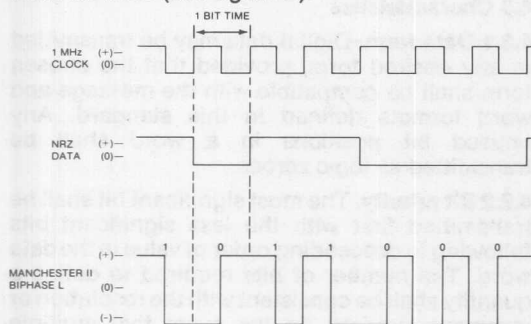


Figure 2 of 1553B. Data Encoding

*This paragraph remained unchanged in both revisions of the standard.*

**4.3.3.3 Transmission bit rate.** The transmission bit rate on the bus shall be 1.0 megabit per second with a combined accuracy and long-term stability of  $\pm 0.1$  percent (i.e.,  $\pm 1000$  Hertz (Hz)). The short-term stability (i.e., stability over 1.0 second interval) shall be at least 0.01 percent (i.e.,  $\pm 100$  Hz).

*The long- and short-term stability of the individual internal clocks used to transmit encoded data have been relaxed in 1553B. The order of magnitude reduction in transmission bit rate stability allows for the selection of multiplex bus interface clocks that can meet long-shelf-life requirements of some weapons.*

**4.3.3.4 Word size.** The word size shall be 16 bits plus the sync waveform and the parity bit for a total of 20 bits times as shown on figure 3.

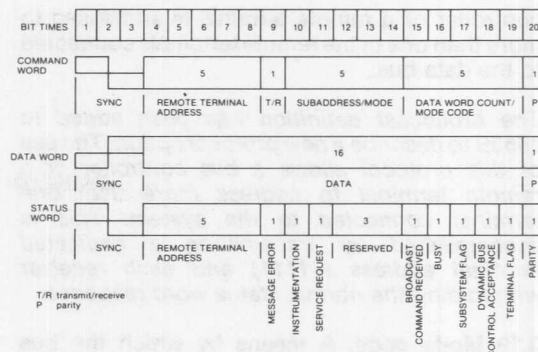


Figure 3 of 1553B. Word Formats

*The 20-bit word size was selected because it represented the minimum number of bits in a word, when 16 bits of data, a three-bit invalid Manchester sync pattern, and a single parity bit are used. Except for paragraph changes of 4.2.3.4 (1553A) to 4.3.3.4 (1553B) this paragraph remained unchanged. Three-bit invalid Manchester sync pattern is described in 1553B, paragraph 4.3.3.5.1.1 Figure 3 (referenced in this paragraph) is modified in 1553B to reflect the identification of status codes.*

**4.3.3.5 Word formats.** The word formats shall be as shown on figure 3 for the command, data, and status words.

*Three types of word formats were selected to operate the information transfer system. Each format and the changes reflected in 1553B will be discussed in the following paragraphs.*

**4.3.3.5.1 Command word.** A command word shall be comprised of a sync waveform, remote terminal address field, transmit/receive (T/R) bit, subaddress/mode field, word count/mode code field, and a parity (P) bit (see figure 3).

*The command word format is used to control and manage the information transfer system. Two basic additions were made to the command word by 1553B. These include the broadcast mode and the identification of the optional mode codes.*

**4.3.3.5.1.1 Sync.** The command sync waveform shall be an invalid Manchester waveform as shown on figure 4. The width shall be three bit times, with the sync waveform being positive for the first one and one-half bit times, and then negative for the following one and one-half bit times. If the next bit following the sync waveform is a logic zero, then the last half of the sync

waveform will have an apparent width of two clock periods due to the Manchester encoding.

*The sync pattern used in the standard remained unchanged.*

**4.3.3.5.1.2 Remote terminal address.** The next five bits following the sync shall be the RT address. Each RT shall be assigned a unique address. Decimal address 31 (11111) shall not be assigned as a unique address. In addition to its unique address, a RT shall be assigned decimal address 31 (11111) as the common address, if the broadcast option is used.

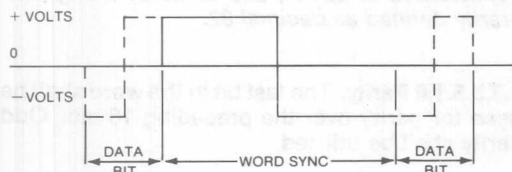


Figure 4 of 1553B. Command and Status Sync

Each remote terminal will be assigned a unique address for which it is responsible to respond when the address is transmitted as part of a command word on the data bus by the active bus controller. Only one remote terminal address cannot be assigned as a unique address (decimal address 31). This address has been assigned to all remote terminals as the common address for which they will receive broadcasted data if the system uses the broadcast option.

The broadcast mode provides a mechanism for transmitting information to multiple users with a single message. The mechanism for accomplishing this was to dedicate address 31 (11111) to be reserved for broadcast messages. Anytime a broadcast message is transmitted, the transmitting terminal will use address 31 rather than a unique terminal address. All other addresses can be assigned as in 1553A. Since multiple sets of broadcast messages can be responding status word must be suppressed. By choosing the address method to accomplish the broadcast mode, all the other formats of the command word are available for use. Broadcast messages can be used with subaddresses and mode codes. The subaddress in a broadcast message can allow multiple users with broadcast reception capability to sort out specific broadcast messages transmitted, if given this capability in hardware or software. Therefore, multiple sets of broadcast messages can be defined. In addition, the broadcast format can be used with mode codes. This allows simultaneous transmission of mode commands to users.

*Indiscriminate use of the broadcast technique is not advisable. Designers must question the benefit of discarding the command/response format, in which all message completion failures are known to the bus controller, to the benefits described below. Broadcast use may increase system operation complexity since subaddresses of broadcast address and addressed terminal will not likely be the same. This requires additional subaddresses. Finally, the broadcast technique, if used, adds a failure mode to the system if a terminal in a failure mode used address 31 for a message.*

*Proper use of the broadcast mode may yield several benefits:*

- Multiple terminals can be communicated with simultaneously, thereby permitting time synchronization of data or commands.*
- Bus duty cycle can be reduced by transmitting data required by multiple users simultaneously instead of sequentially.*
- Some error management can be enhanced by providing a single address by which all terminals can receive commands simultaneously. This permits the bus controller to immediately command a state for the system rather than polling each unit individually with the same command in a serial fashion.*

The broadcast message capability can produce considerable reduction in bus usage. This is particularly true for systems using multiple units for redundancy or systems dependent on parallel processing, thus requiring simultaneous data arrival at the processing units. As noted in 1553B, paragraph 10.6 (appendix to 1553B), improper use of the broadcast format can result in undesirable system operation. Since no status word response is allowed from the receiving terminal, discretion must be exercised when applying the capability. To provide message arrival verification, a bit in the status word is set when a valid broadcast message is received. This allows reporting of the reception if requested by the active bus controller using the mode code "transmit status word." In error situations, it may be advisable for the bus controller to request the last command word to verify that the broadcast command was received. There may be situations for which rebroadcast cannot be permitted. Asking for last command first preserves the last status word (i.e., the terminal does not reset or update status). In addition to data transfers, the ability to transmit a broadcast command message provides an effective method for managing the data bus system. This capability is performed using the broadcast address in combination with mode commands.

**4.3.3.5.1.3 Transmit/receive.** The next bit following the remote terminal address shall be the T/R bit, which shall indicate the action required of the RT. A logic zero shall indicate the RT is to receive, and a logic one shall indicate the RT is to transmit.

*The transmit/receive bit in the command word indicates the source of data flow in the information transfer system. Basically, the paragraph remained unchanged for both revisions of the standard except for wording changes and paragraph numbering differences.*

**4.3.3.5.1.4 Subaddress/mode.** The next five bits following the T/R bit shall be utilized to indicate an RT subaddress or use of mode control, as is dictated by the individual terminal requirements. The subaddress/mode values of 00000 and 11111 are reserved for special purposes, as specified in 4.3.3.5.1.7, and shall not be utilized for any other function.

*This field has two functions: (1) the subaddress identification of specific messages to a remote terminal and (2) reserved subaddresses that serve as the identification that a mode command to the information transfer system is being transmitted. Both of these capabilities were present in 1553A. However, an additional mode code designator has been established in 1553B (decimal 31). The use of either 00000 or 11111 in the subaddress/mode field will be decoded to indicate that a mode code command is present in the next five-bit field. This limits the subaddress range to a maximum of 30 unique addresses. If the instrumentation bit (par. 4.3.3.5.3) in the status word is implemented, the subaddresses will be limited to 15 unique subaddresses. The requirements for use of the instrumentation bit are in 1553B, paragraph 4.3.3.5.3.4 In complex remote terminals (i.e., terminals interfacing with several sensors or multiple interface types), the subaddress capacity of a terminal can be exceeded. In addition, messages to a given remote terminal-subaddress may contain "packed" data requiring additional decoding prior to distribution within the terminal. Both of these conditions can cause the remote terminal's design to incorporate a map (i.e., look-up table) approach for subaddress message distribution.*

**4.3.3.5.1.5 Data word count/mode code.** The next five bits following the subaddress/mode control shall be the quantity of data words to be either sent out or received by the RT or the optional mode code as specified in 4.3.3.5.1.7. A maximum of 32 data words may be transmitted or received in any one message block. All 1's shall indicate a

decimal count of 31, and all 0's shall indicate a decimal count of 32.

*The dual function of this field provides for the identification of message lengths for data message or mode codes for managing the information transfer system. The identification of both of these capabilities was provided in 1553B but only the word count was specified in 1553A (even though the mode code function has remained the same in both revisions). The five-bit field allows 32 data words to be transmitted in a message or 32 specific mode codes. This is accomplished by one data word being represented as 00001, and all zeros being arbitrarily defined as decimal 32.*

**4.3.3.5.1.6 Parity.** The last bit in the word shall be used for parity over the preceding 16 bits. Odd parity shall be utilized.

*The use of a single parity bit per word was provided to identify bit errors occurring during the transmission and detection of a word. According to the statement in the appendix to 1553B, "Theoretical and empirical evidence indicates that an undetected bit error rate of  $10^{-12}$  can be expected from a practical multiplex system built to this standard." See 1553B, paragraph 10.4. Also see noise test in 1553B, paragraph 4.5.2.1.2.4. This paragraph remained unchanged during both revisions.*

**4.3.3.5.1.7 Optional mode control.** For RT's exercising this option a subaddress/mode code of 00000 or 11111 shall imply that the contents of the word count field are to be decoded as a five bit mode command. The mode code shall only be used to communicate with the multiplex bus related hardware, and to assist in the management of information flow, and not to extract data from or feed data to a functional subsystem. Codes 00000 through 01111 shall only be used for mode codes which do not require transfer of a data word. For these codes, the T/R bit shall be set to 1. Codes 10000 through 11111 shall only be used for mode codes which require transfer of a single data word. For these mode codes, the T/R bit shall indicate the direction of data word flow as specified in 4.3.3.5.1.3. No multiple data word transfer shall be implemented with any mode code. The mode codes are reserved for the specific functions as specified in table I and shall not be used for any other purposes. If the designer chooses to implement any of these functions, the specific codes, T/R bit assignments, and use of a data word, shall be used as indicated. The use of the



Table I. Assigned Mode Codes

Transmit- receive bit	Mode code	Function	Associated data word	Broadcast command allowed
1	00000	Dynamic bus control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit status word	No	No
1	00011	Initiate self-test	No	Yes
1	00100	Transmitter shutdown	No	Yes
1	00101	Override transmitter shutdown	No	Yes
1	00110	Inhibit terminal flag bit	No	Yes
1	00111	Override inhibit terminal flag bit	No	Yes
1	01000	Reset remote terminal	No	Yes
1	01001	Reserved	No	TBD
1	01111	Reserved	No	TBD
1	10000	Transmit vector word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit last command	Yes	No
1	10011	Transmit bit word	Yes	No
0	10100	Selected transmitter shutdown	Yes	Yes
0	10101	Override selected transmitter shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
1 or 0	11111	Reserved	Yes	TBD

Note: TBD — to be determined.

broadcast command option shall only be applied to particular mode codes as specified in table I.

*The basic philosophy of the information transfer system is that it operates as a transparent communication link. "Transparent" means that an application's function does not need to be involved with the management of communication control. Obviously, the information transfer system requires management that introduces overhead into the transmission of data. The command words, status words, status word gaps, and message gaps are the overhead. Within the command word the mode codes provide data bus management capability. The mode codes have been divided into two groups: mode codes without a data word (00000-01111) and mode codes with a data word (10000-11111). The use of bit 15 in the command word to identify the two types was provided to aid in the decoding process. Also, the use of a single data word*

*instead of multiple data words was adopted to simplify the mode circuitry. Generally, with these two types of mode commands, all management requirements of an information transfer system can be met.*

*Control messages are identified by the subaddress/mode field in the command word being set to 32 (00000) or 31 (11111). (In this case, 1553B defines decimal subaddress 32 to be equal to binary 00000 so that decimal 1 through decimal 31 correspond to binary 00001 through 11111.) All control messages originate with the active bus controller and are received by a single receiver or by multiple receivers (broadcast). A terminal address value of 31 (11111) in the command word indicates a broadcast message, while any other terminal addresses are to identify unique messages to a terminal on the bus. The mode command information is contained completely in the mode code/word field of the command word.*

*Table I of 1553B should be examined carefully to*

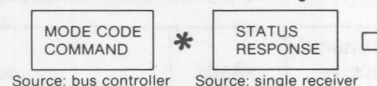
see the symmetry of the mode codes. The first 16 codes are not transmitted with a data word; the last 16 are. It is not appropriate to broadcast some of the mode codes because of the possibility of bus crashes -- simultaneous transmission by two or more terminals. Examples are requests for transmissions from RTs. Also, broadcast of dynamic bus control makes no sense. The T/R bit is important for mode codes 17 to 31 because it defines whether bus controller or RT is to transmit the associated data word.

The use of mode commands option is defined in both versions of the standard; however, 1553B defines each mode command while 1553A only defines dynamic bus control. There is no particular reason for the assignment of the mode codes, except for dynamic bus control (00000), which was previously defined in 1553A, and this separation of mode command by their use of a data word. The purpose of reserved mode commands in each category (with and without data words) is important to allow for controlled expansion of the standard. By controlling the mode code command number and its definition, commonality between various terminal can be maintained. Each mode code command identification is listed in 1553B, table I. All other mode codes are considered illegal commands. The message formats associated with mode commands are shown in figure II-1.

**4.3.3.5.1.7.1 Dynamic bus control.** The controller shall issue a transmit command to an RT capable of performing the bus control function. This RT shall respond with a status word as specified in 4.3.3.5.3. Control of the data bus passes from the offering bus controller to the accepting RT upon completion of the transmission of the status word by the RT. If the RT rejects control of the data bus, the offering bus controller retains control of the data bus.

The dynamic bus control mode command (00000) is provided to allow the active bus controller a mechanism (using the information transfer system message formats) to offer a potential bus controller (operating as a remote terminal) control of the data bus. Only the single receiver command request (unique address) is allowed to be issued by the active bus controller. The response to this offering of bus controller is provided by the receiving remote terminal using the dynamic bus control acceptance bit in the status word (par. 4.3.3.5.3). Rejection of this request by the remote terminal requires the presently active bus controller to continue offering control to other potential controllers or remain in control. When a remote terminal

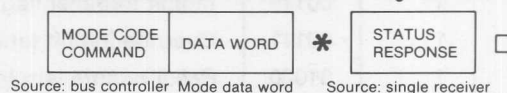
Mode Command Without Data Word to a Single Receiver



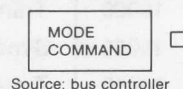
Transmit Mode Command With Data Word to a Single Receiver



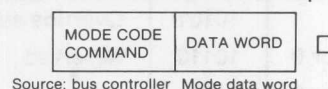
Receive Mode Command With Data Word to a Single Receiver



Transmit Mode Command Without Data Word to Multiple Receivers



Transmit Mode Command With Data Word to Multiple Receivers



- \* Response time delay or gap
- End of message delay or gap

Figure II-1. Mode Command Message Transfer Formats

accepts control of the data bus system by setting the dynamic bus control acceptance bit in the status word, control is relinquished by the presently active bus controller, and the potential bus controller begins bus control.

Note that the sequence above requires software (or firmware) implementation in all bus controllers.

**4.3.3.5.1.7.2 Synchronize (without data word).** This command shall cause the RT to synchronize (e.g., to reset the internal timer, to start a sequence, etc.) The RT shall transmit the status word as specified in 4.3.3.5.3.

**4.3.3.5.1.7.12 Synchronize (with data word).** The RT shall receive a command word followed by

data word as specified in 4.3.3.5.2. The data word shall contain synchronization information for the RT. After receiving the command and data word, the RT shall transmit the status word as specified in 4.3.3.5.3.

*Synchronization informs the terminal(s) of an event time to allow coordination between the active bus controller and receiving terminals. Synchronization information may be implicit in the command word (mode code 00001) or a data word (mode code 10001) may be used to follow the command word to provide the synchronization information. If a data word is used, the definition of the bit meanings is the responsibility of the system designer.*

**4.3.3.5.1.7.3 Transmit status word.** This command shall cause the RT to transmit the status word associated, with the last valid command word preceding this command. This mode command shall not alter the state of the status word.

*The status word associated with mode code (00010) is shown in figure II-2 and contains the following information:*

- a. Transmitting terminal address
- b. Message error bit
- c. Instrumentation bit
- d. Service request bit
- e. Broadcast command receive bit
- f. Busy bit
- g. Subsystem flag bit
- h. Terminal flag bit

*Details concerning the usage of the status bits are discussed in 1553B, paragraph 4.3.3.5.3. The only message format for acquiring the status word using this mode code is for the bus controller to request the status word from a single receiver. Note that use of this mode code by the bus controller causes the **last** status word to be transmitted. Some subtle conditions need to be examined by the designer who uses this mode command. For example, if the transmit built-in-test mode command is needed to verify the*

*terminal is operational, that request (see 4.3.3.5.1.7.14) must be issued after the transmit status word mode code to prevent loss of the previous message's status.*

**4.3.3.5.1.7.4 Initiate self test.** This command shall be used to initiate self test within the RT. The RT shall transmit the status as specified in 4.3.3.5.3.

*The initiate self-test mode command (00011) is provided to initiate built-in-test (BIT) circuitry within remote terminals. The mode code is usually followed, after sufficient time for test completion, by a transmit BIT word mode command yielding the results of the test. The message formats provided for this mode command allow for both individual requests and multiple requests. Notice that the initiate self-test mode command is associated with the multiplex system terminal hardware only.*

#### **4.3.3.5.1.7.14 Transmit built-in-test (BIT) word.**

This command shall cause the RT to transmit its status word as specified in 4.3.3.5.3 followed by a single data word containing the RT BIT data. This function is intended to supplement the available bits in the status words when the RT hardware is sufficiently complex to warrant its use. The data word, containing the RT BIT data, shall not be altered by the reception of a transmit last command or a transmit status word mode code. This function shall not be used to convey BIT data from the associated subsystem(s).

*The transmit BIT word mode command (10011) provides the BIT results available from a terminal, as well as the status word. Typical BIT word information for both embedded and standalone remote terminals includes encoder-decoder failure, analog T/R failures, terminal control circuitry failures, power failures, subsystem interface failures, and protocol errors (e.g., parity, Manchester, word count, status word errors, and status word exceptions). The internal contents of the BIT data word are provided to supplement the appropriate bits already available via the status word for complex terminals. Notice that the transmit BIT word within the remote terminal "... shall not be altered by the reception of a transmit last command or transmit status word mode code" received by the terminal. This allows error handling and recovery procedures to be used without changing the error data recorded in this word. However, the RT will only save the last command, and the status code field (of the status word) will not be changed if transmit last command or transmit status word mode commands are transmitted. If, however, any other transmissions are made to the RT, the*

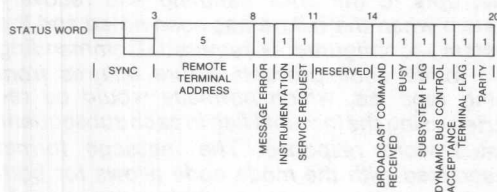


Figure II-2. Status Word

*Broadcast of this command by the bus controller is not allowed. See paragraphs 4.3.3.5.1.7.3 and 4.3.3.5.1.7.13*

*Another point worth noting is that the function of transmitting RT BIT data "... shall not be used to convey BIT data from the associated subsystem(s)." Subsystem fault investigation, when indicated by the subsystem flag, is not specified or otherwise restricted by 1553. Therefore, system designers must make the necessary provisions.*

**4.3.3.5.1.7.5 Transmitter shutdown.** This command (to only be used with dual redundant bus systems) shall cause the RT to disable the transmitter associated with the redundant bus. The RT shall not comply with a command to shut down a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word as specified in 4.3.3.5.3. after this command.

**4.3.3.5.1.7.6 Override transmitter shutdown.** This command (to only be used with dual redundant bus system) shall cause the RT to enable a transmitter which was previously disabled. The RT shall not comply with a command to enable a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word as specified in 4.3.3.5.3 after this command.

**4.3.3.5.1.7.15 Selected transmitter shutdown.** This command shall cause the RT to disable the transmitter associated with a specified redundant data bus. The command is designed for use with systems employing more than two redundant buses. The transmitter that is to be disabled shall be identified in the data word following the command word in the format as specified in 4.3.3.5.2.. The RT shall not comply with a command to shut down a transmitter on the bus from which this command is received. In all cases, the RT shall respond with a status word as specified in 4.3.3.5.3.

**4.3.3.5.1.7.16 Override selected transmitter shutdown.** This command shall cause the RT to enable a transmitter which was previously disabled. The command is designed for use with systems employing more than two redundant buses. The transmitter that is to be enabled shall be identified in the data word following the command word in the format as specified in 4.3.3.5.2. The RT shall not comply with a command to enable a transmitter on the bus from which this command is received. In all cases, the

Four mode code commands are provided to control transmitters associated with terminals in a system. These commands can be sent to a single receiver or broadcast to multiple users.

The transmitter shutdown mode code (00100) is used in a dual-redundant bus structure where the command causes the transmitter associated with the other redundant bus to terminate transmissions. No data word is provided for this mode.

The override transmitter shutdown mode code (00101) is used in a dual-redundant bus structure where the command allows the transmitter previously disabled associated with the redundant bus to transmit when commanded by a normal bus command initiated by the active bus controller. No data word is provided for this mode code.

The selected transmitter shutdown mode code (10100) is used in a multiple (greater than two) redundant bus structure where the command causes the selected transmitter to terminate transmissions on its bus. A data word is used to identify the selected transmitter.

The override selected transmitter shutdown mode code (10101) is used in a multiple (greater than two) redundant bus structure where the command allows the selected transmitter to transmit on its bus when commanded by a normal bus command initiated by the active bus controller. A data word is used to identify the selected transmitter.

**4.3.3.5.1.7.7 Inhibit terminal flag (T/F) bit.** This command shall cause the RT to set the T/F bit in the status word specified in 4.3.3.5.3 to logic zero until otherwise commanded. The RT shall transmit the status word as specified in 4.3.3.5.3.

The inhibit terminal flag mode code (00110) is used to set the terminal flag bit in the status word to an **unfailed** condition regardless of the actual state of the terminal being addressed. This mode code is primarily used to prevent continued interrupts to the error handling and recovery system when the failure has been noted and the system reconfigured as required. Commanding this mode code prevents future failures from being reported, which normally would be reported using the terminal flag in each subsequent status word response. The message format associated with the mode code allows for both single receivers and multiple receivers to respond. No data word is required with this mode code. Note that the terminal flag, which is used to



indicate an RT fault condition is implicitly limited to terminal faults.

**4.3.3.5.1.7.8 Override inhibit T/F bit.** This command shall cause the RT to override the inhibit T/F bit specified in 4.3.3.5.1.7.7. The RT shall transmit the status word as specified in 4.3.3.5.3.

*The override inhibit T/F flag mode command (00111) negates the inhibit function thus allowing the T/F flag bit in the status response to report present condition of the terminal. This mode code can be transmitted by the active bus controller to both single and multiple receivers. There is no data word associated with this mode code.*

**4.3.3.5.1.7.9 Reset remote terminal.** This command shall be used to reset the RT to a power up initialized state. The RT shall first transmit its status word, and then reset.

*The reset remote terminal mode code (01000) causes the addressed terminal to reset itself to a power-up initialized state. This mode code may be transmitted to an individual or to multiple terminals.*

**4.3.3.5.1.7.11 Transmit vector word.** This command shall cause the RT to transmit a status word as specified in 4.3.3.5.3 and a data word containing service request information.

*The transmit vector word mode code (10000) is associated with the service request bit in the status word and is used to determine specific service being required by the terminal. The service request bit and the transmit vector word provide the only means available for the terminal to request the scheduling of an asynchronous message if more than one service request exists per terminal. The message format for this single receiver operation contains a data word associated with the terminal's response. Figure II-3 illustrates the message formats associated with this mode command.*

**4.3.3.5.1.7.13 Transmit last command word.** This command shall cause the RT to transmit its status word as specified in 4.3.3.5.3 followed by a single data word which contains bits 4-19 of the last command word, excluding a transmit last command word mode code received by the RT. This mode command shall not alter the state of the RT's status word.

*The transmit last command mode code (10010) is used in the error handling and recovery process*

*to determine the last valid command received by the terminal, except for this mode code. Also this mode code will not change the state of the status word. The message format associated with the single receiver last command word contains a data word from the responding terminal. The data word contains the previous 16 bits of the last valid command word received. Notice that this mode command will not alter the state of the receiving terminals status word. This fact allows this mode command to be used in error handling and recovery operation without affecting the status word, which can have added error data.*

**4.3.3.5.1.7.10 Reserved mode codes (01001 to 01111).** These mode codes are reserved for future use and shall not be used.

**4.3.3.5.1.7.17 Reserved mode codes (10110 to 11111).** These mode codes are reserved for future use and shall not be used.

*Each of the mode code types (with and without data words) have several unused mode codes that are reserved for future use and cannot be used without the permission of the Military Standard's Controlling Agency.*

**4.3.3.5.2 Data word.** A data word shall be comprised of a sync waveform, data bits, and a parity bit (see figure 3).

*Figure II-4 illustrates the 1553 data word.*

**4.3.3.5.2.1 Sync.** The data sync waveform shall be an invalid Manchester waveform as shown on figure 5. The width shall be three bit times, with the waveform being negative for the first one and one-half bit times, and then positive for the following one and one-half bit times. Note that if the bits preceding and following the sync are logic ones, then the apparent width of the sync waveform will be increased to four bit times.

**4.3.3.5.2.2 Data.** The sixteen bits following the sync shall be utilized for data transmission as specified in 4.3.2.

**4.3.3.5.2.3 Parity.** The last bit shall be utilized for parity as specified in 4.3.3.5.1.6.

*Data words are used to transmit parameter data, which is the goal of the information transfer system. Data words are distinguished from command and status words by the inverted three-bit sync pattern. Both packed and unpacked data may be transmitted in the 16-bit data field. Odd parity on the data field provides data integrity identical to the command and status word formats. No changes in the 1553A or 1553B have*

Single Receiver Only — Bus Controller to Remote Terminal\*

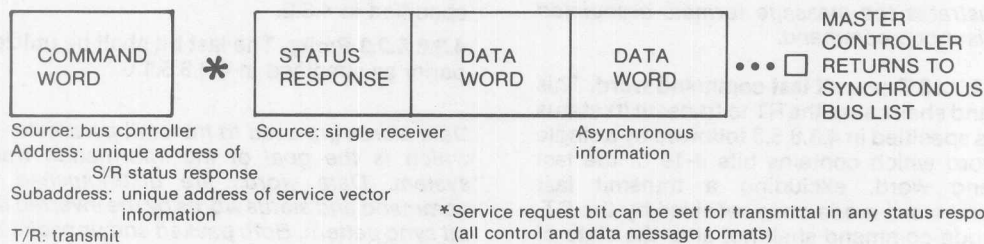
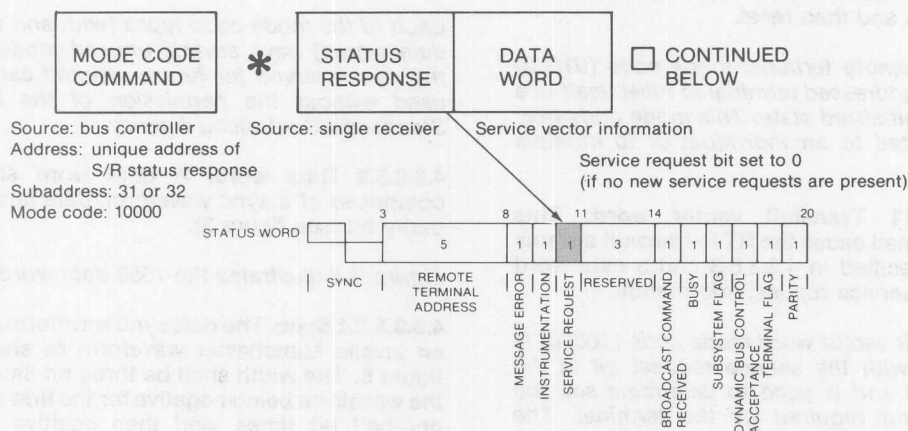
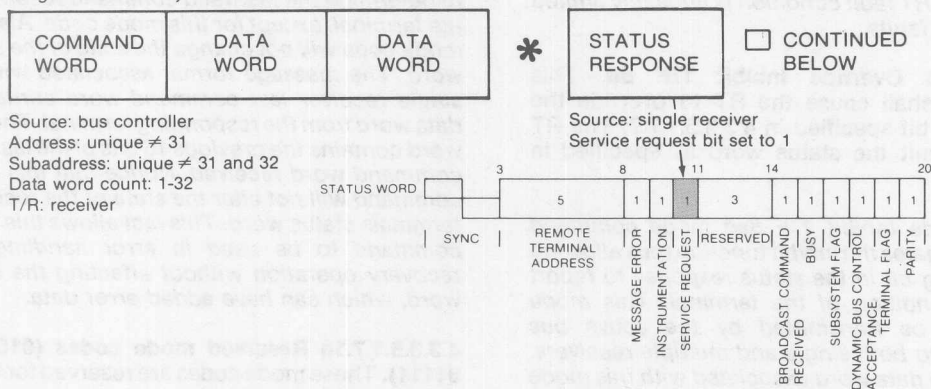


Figure II-3. Transmit Vector Word Transfer Format

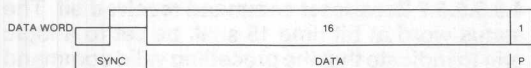


Figure II-4. 1553 Data Word

occurred in these paragraphs except for paragraph numbering (e.g., 4.2.3.5.2 for 1553A and 4.3.3.5.2 for 1553B).

**4.3.3.5.3. Status word.** A status word shall be comprised of a sync waveform, RT address, message error bit, instrumentation bit, service request bit, three reserved bits, broadcast command received bit, busy bit, subsystem flag bit, dynamic bus control bit, terminal flag bit, and a parity bit. For optional broadcast operation, transmission of the status word shall be suppressed as specified in 4.3.3.6.7.

**4.3.3.5.3.1 Sync.** The status sync waveform shall be as specified in 4.3.3.5.1.1.

**4.3.3.5.3.2 RT address.** The next five bits following the sync shall contain the address of the RT which is transmitting the status word as defined in 4.3.3.5.1.2.

The status word is part of the basic overhead requirements of the data bus system. The status word is shown in figure II-5 is divided into the following fields:

- Sync (same as command sync)
- Terminal address
- Status field
- Parity (P)

The five-bit address field identifies the transmitting terminal's address, while the remote terminal's status is based on bits set in the status field. The status field consists of the following information:

- Message error bit
- Instrumentation bit
- Service request bit
- Reserved field

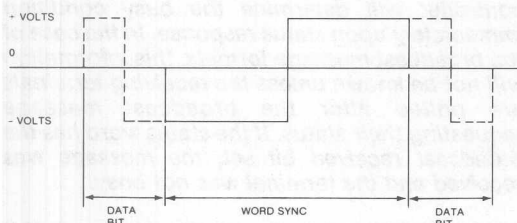


Figure 5 of 1553B. Data Sync

- Broadcast command received bit
- Busy bit
- Subsystem flag
- Dynamic bus control acceptance bit
- Terminal flag

**4.3.3.5.3.3 Message error bit.** The status word bit at bit time nine (see figure 3) shall be utilized to indicate that one or more of the data words associated with the preceding receive command word from the bus controller has failed to pass the RT's validity tests as specified in 4.4.1.1. This bit shall also be set under the conditions specified in 4.4.1.2, 4.4.3.4 and 4.4.3.6. A logic one shall indicate the presence of a message error, and a logic zero shall show its absence. All RT's shall implement the message error bit.

The message error bit is set to logic one to indicate that one or more of the data words associated with the preceding received message has failed to pass the message validity test. The message validity requirements are:

- Word validation -- word begins with valid sync, Manchester II code correctly transmitted, 16 data bits plus parity, and word parity odd
- Contiguous words within a message
- Address validation -- matches address unique terminal or broadcast address
- Illegal command -- a terminal with the illegal command detection circuitry detects an illegal command

The status word will be transmitted if the message validity requirements are met (see para. 4.4.3.5 and 4.4.3.6). When a message error occurs in a broadcast message format, the message error bit will be set in the status word and the status response withheld as required by broadcast message format.

**4.3.3.5.3.4 Instrumentation bit.** The status word bit time of 10 (see figure 3) shall be reserved for the instrumentation bit and shall always be a logic zero. This bit is intended to be used in conjunction with a logic one in bit time 10 of the

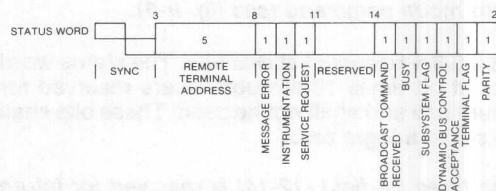


Figure II-5. Status Word

command word to distinguish between a command word and a status word. The use of the instrumentation bit is optional.

*The instrumentation bit in the status field is set to distinguish the status word from the command word. Since the sync field (three bits) is used to distinguish the command and status words from a data word, a mechanism to distinguish command and status is provided by the instrumentation bit. By setting this bit to logic zero for all conditions and setting the same bit position in the command word to a logic one, the command and status words are identifiable. If used, this approach reduces the possible subaddress in the command word to 15 and requires subaddress 31 (11111) to be used to identify mode commands (both 31 and 32 are allowed). If not used, the bit will remain set to logic zero in the status word for all conditions.*

*how is the bus used?*

**4.3.3.5.3.5 Service request bit.** The status word bit at bit time eleven (see figure 3) shall be reserved for the service request bit. The use of this bit is optional. This bit when used, shall indicate the need for the bus controller to take specific predefined actions relative to either the RT or associated subsystem. Multiple subsystems, interfaced to a single RT, which individually require a service request signal shall logically OR their individual signals into the single status word bit. In the event this logical OR is performed, then the designer must make provisions in a separate data word to identify the specific requesting subsystem. The service request bit is intended to be used only to trigger data transfer operations which take place on an exception rather than periodic basis. A logic one shall indicate the presence of a service request, and a logic zero its absence. If this function is not implemented, the bit shall be set to zero.

*The service request bit is provided to indicate to the active bus controller that a remote terminal requests service. When this bit in the status word is set to logic one, the active bus controller may take a predetermined action or use mode command (transmit vector word) to identify the specific request. The message format for acquiring this is discussed under transmit vector word mode command (see fig. II-3).*

**4.3.3.5.3.6 Reserved status bits.** The status word bits at bit times 12 through 14 are reserved for future use and shall not be used. These bits shall be set to a logic zero.

*The three bit-field (12-14) is reserved for future requirements and is set to logic zero. Any bit in this field not set to logic zero will be disregarded.*

**4.3.3.5.3.7 Broadcast command received bit.** The status word at bit time 15 shall be set to a logic one to indicate that the preceding valid command word was a broadcast command and a logic zero shall show it was not a broadcast command. If the broadcast command option is not used, this bit shall be set to a logic zero.

*The broadcast command received bit is set to logic one when the preceding valid command word was a broadcast command (address 31). Since broadcast message formats require the receiving remote terminals to suppress their status words, the broadcast command received bit is set to identify that the command was received properly. If the broadcast message validity is desired, the message format shown in figure II-6 is used to determine this information. The broadcast command received bit will be reset when the next valid command is received by the remote terminal, unless the next valid command is transmit status word or transmit last command.*

**4.3.3.5.3.8 Busy bit.** The status word bit at bit time 16 (see figure 3) shall be reserved for the busy bit. The use of this bit is optional. This bit, when used, shall indicate that the RT or subsystem is unable to move data to or from the subsystem in compliance with the bus controller's command. A logic one shall indicate the presence of a busy condition, and a logic zero its absence. In the event the busy bit is set in response to a transmit command, then the RT shall transmit its status word only. If this function is not implemented, the bit shall be set to logic zero.

*The busy bit in the status word is set to logic one to indicate to the active bus controller that the remote terminal is unable to move data to or from the subsystem in compliance with the bus controller's command. The message format associated with a busy condition is shown in figure II-7. A busy condition can exist within a remote terminal at any time causing it to be nonresponsive to a command to send data or to be unable to receive data. This condition can exist for all message formats. In each case except the broadcast message formats, the active bus controller will determine the busy condition immediately upon status response. In the case of the broadcast message formats, this information will not be known unless the receiving terminals are polled after the broadcast message requesting their status. If the status word has the broadcast received bit set, the message was received and the terminal was not busy.*

**4.3.3.5.3.9 Subsystem flag bit.** The status word bit at bit time 17 (see figure 3) shall be reserved for



**Multiple Receivers — Bus Controller to Remote Terminals**

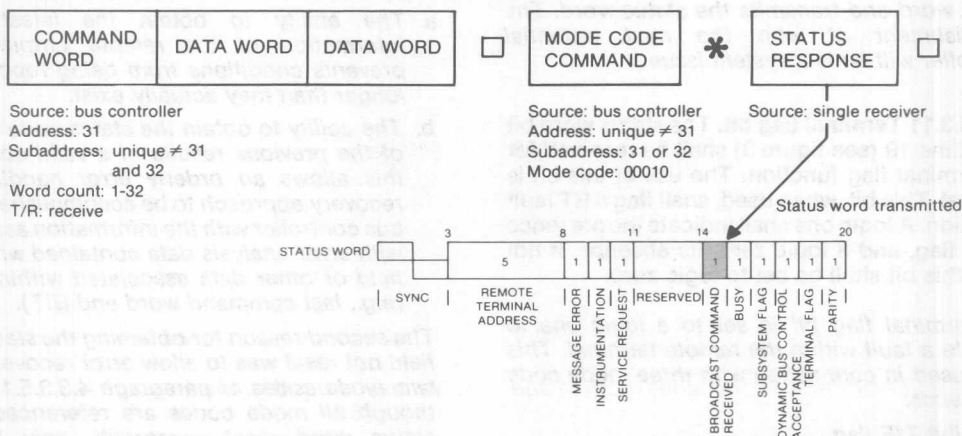


Figure II-6. Broadcast Command Receive Bit

the subsystem flag bit. The use of this bit is optional. This bit, when used, shall flag a subsystem fault condition, and alert the bus controller to potentially invalid data. Multiple subsystems, interfaced to a single RT, which individually require a subsystem flag bit signal shall logically OR their individual signals into the single status word bit. In the event this logical OR is performed, then the designer must make provisions in a separate data word to identify the specific reporting subsystem. A logic one shall indicate the presence of the flag, and a logic zero its absence. If not used, this bit shall be set to logic zero.

*The subsystem flag bit is provided to indicate to the active bus controller that a subsystem fault condition exists and that data being requested from the subsystem may be invalid. The subsystem flag may be set in any transmitted status word.*

**4.3.3.5.3.10 Dynamic bus control acceptance bit**

The status word bit at bit time 18 (see figure 3) shall be reserved for the acceptance of dynamic bus control. This bit shall be used if the RT implements the optional dynamic bus control function. This bit, when used, shall indicate acceptance or rejection of a dynamic bus control offer as specified in 4.3.3.5.1.7.1. A logic one shall indicate acceptance of control, and a logic zero shall indicate rejection of control. If this function is not used, this bit shall be set to logic zero.

*This bit is provided to indicate the acceptance of the bus controller offer by the active bus controller to become the next bus controller. The offer of bus control occurs when the presently active bus controller has completed its established message list and issues a dynamic bus control mode command to the remote terminal that is to be the next potential controller. To accept the offer the potential bus controller*

**Single Receiver — Bus Controller to Remote Terminal**

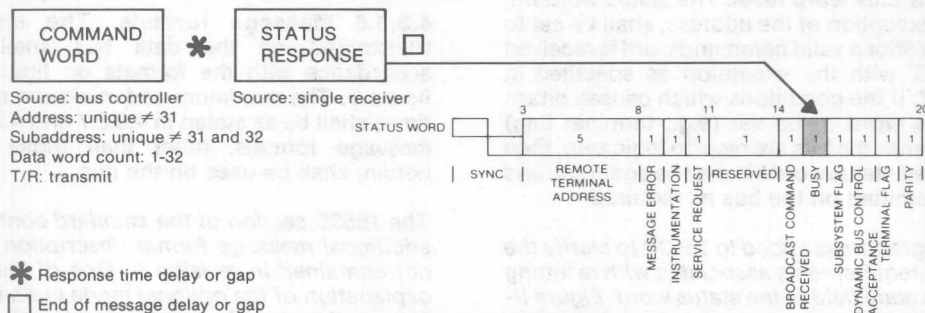


Figure II-7. Busy Bit

status word and transmits the status word. The establishment of who the next potential controller will be is a system issue.

**4.3.3.5.3.11 Terminal flag bit.** The status word bit at bit time 19 (see figure 3) shall be reserved for the terminal flag function. The use of this bit is optional. This bit, when used, shall flag a RT fault condition. A logic one shall indicate the presence of the flag, and a logic zero, its absence. If not used, this bit shall be set to logic zero.

*The terminal flag bit is set to a logic one to indicate a fault within the remote terminal. This bit is used in connection with three mode code commands:*

- a. Inhibit T/F flag
- b. Override inhibit T/F flag
- c. Transmit BIT word

*The first two mode code commands deactivate and activate the functional operation of the bit. The transmit BIT word mode code command is used to acquire more detailed information about the terminal's failure.*

**4.3.3.5.3.12 Parity bit.** The least significant bit in the status word shall be utilized for parity as specified in 4.3.3.5.1.6.

*The use of a single parity bit per word was provided to identify any bit errors occurring during the transmission and detection of a word. This odd parity check will detect an odd number of bit errors occurring in a word. This requirement produces an undetected bit error rate of  $10^{-12}$ , which was considered satisfactory for a general-purpose information transfer system. This paragraph remained unchanged during both revisions. See also 1553B, paragraph 4.3.3.5.1.6.*

**4.3.3.5.4. Status word reset.** The status word bit, with the exception of the address, shall be set to logic zero after a valid command word is received by the RT with the exception as specified in 4.3.3.5.1.7. If the conditions which caused bits in the status word to be set (e.g., terminal flag) continue after the bits are reset to logic zero, then the affected status word bit shall be again set, and then transmitted on the bus as required.

*This paragraph was added to 1553B to clarify the hardware requirements associated with resetting the status code field of the status word. Figure II-5 shows the status word and the information available in this field.*

*One reason for the reset definition is to provide--*

- a. The ability to obtain the latest status information of the remote terminal: this prevents conditions from being reported for longer than they actually exist.
- b. The ability to obtain the status code analysis of the previous results of a valid command: this allows an orderly error handling and recovery approach to be accomplished by the bus controller with the information associated with error analysis data contained within this field or other data associated within the RT (e.g., last command word and BIT).

*The second reason for obtaining the status code field not reset was to allow error recovery using two mode codes of paragraph 4.3.3.5.1.7. Even though all mode codes are referenced in the status word reset paragraph, only two are required to retain the last status word in the terminal:*

- a. Transmit status word
- b. Transmit last command word

*In other words, all other valid messages received, including mode commands, will allow the RT to reset the status word, except these two.*

*Both of these mode codes can be transmitted to the RT without changing the bits in the status code field of the last valid command word in question. Therefore, it is essential that an error recovery procedure be established for the bus controller that takes into account (1) the ability of the RT hardware to collect error data, (2) the format of the data that must be requested by the bus controller to prevent data lost, and (3) the ability of the bus controller hardware and software to receive and react to these data. As many as three mode codes may be involved in this process:*

- a. Transmit last command
- b. Transmit status word
- c. Transmit BIT word

**4.3.3.6 Message formats.** The messages transmitted on the data bus shall be in accordance with the formats on figure 6 and figure 7. The maximum and minimum response times shall be as stated in 4.3.3.7 and 4.3.3.8. No message formats, other than those defined herein, shall be used on the bus.

*The 1553B section of the standard contains two additional message format description that are not contained in revision A. One of these is an explanation of the optional mode code message format that is allowed in revision A but not described with message format diagrams. The*

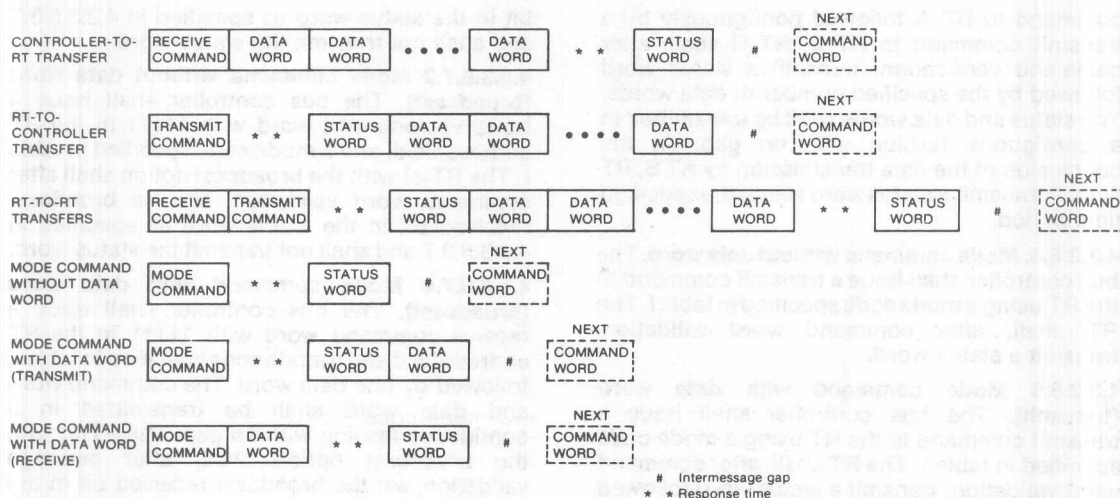


Figure 6 of 1553B. Information Transfer Formats

other description is the message formats associated with the optional broadcast protocol. The command/response protocol provides two types of message formats:

- a. Data messages
- b. Control messages

**4.3.3.6.1 Bus controller to remote terminal transfers.** The bus controller shall issue a receive command followed by the specified number of data words. The RT shall, after message validation, transmit a status word back to the controller. The command and data words shall be

transmitted in a contiguous fashion with no interword gaps.

**4.3.3.6.2 Remote terminal to bus controller transfers.** The bus controller shall issue a transmit command to the RT. The RT shall, after command word validation, transmit a status word back to the bus controller, followed by the specified number of data words. The status and data words shall be transmitted in a contiguous fashion with no interword gaps.

**4.3.3.6.3 Remote terminal to remote terminal transfers.** The bus controller shall issue a receive

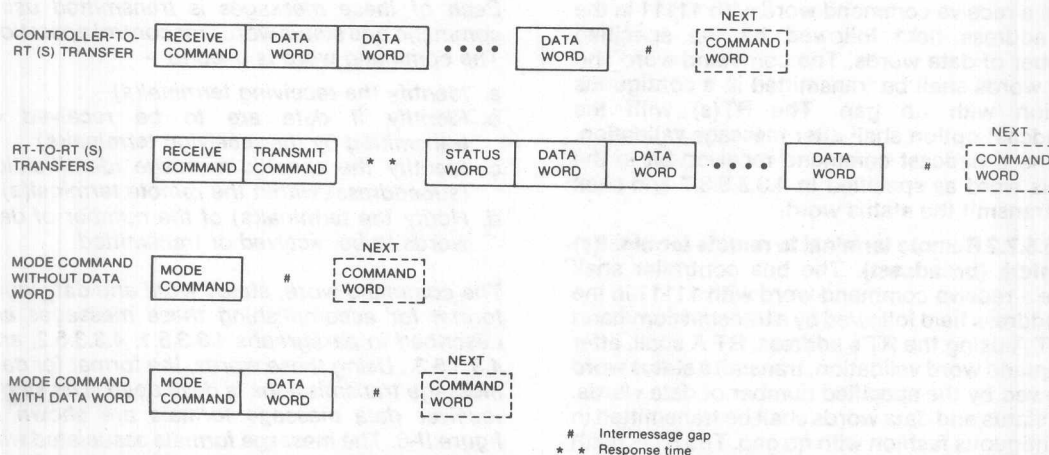


Figure 7 of 1553B. Broadcast Information Transfer Formats

command to RT A followed contiguously by a transmit command to RT B. RT B shall, after command verification, transmit a status word followed by the specified number of data words. The status and data words shall be transmitted in a contiguous fashion with no gap. At the conclusion of the data transmission by RT B, RT A shall transmit a status word within the specified time period.

**4.3.3.6.4. Mode command without data word.** The bus controller shall issue a transmit command to the RT using a mode code specified in table I. The RT shall, after command word validation, transmit a status word.

**4.3.3.6.5 Mode command with data word (transmit).** The bus controller shall issue a transmit command to the RT using a mode code specified in table I. The RT shall, after command word validation, transmit a status word followed by one data word. The status word and data word shall be transmitted in a contiguous fashion with no gap.

**4.3.3.6.6 Mode command with data word (receive).** The bus controller shall issue a receive command to the RT using a mode code specified in table I, followed by one data word. The command word and data word shall be transmitted in a contiguous fashion with no gap. The RT shall, after command and data word validation, transmit a status word back to the controller.

**4.3.3.6.7 Optional broadcast command.** See 10.6 for additional information on the use of the broadcast command.

**4.3.3.6.7.1 Bus controller to remote terminal(s) transfer (broadcast).** The bus controller shall issue a receive command word with 11111 in the RT address field followed by the specified number of data words. The command word and data words shall be transmitted in a contiguous fashion with no gap. The RT(s) with the broadcast option shall after message validation, set the broadcast command received bit in the status word as specified in 4.3.3.5.3.7 and shall not transmit the status word.

**4.3.3.6.7.2 Remote terminal to remote terminal(s) transfers (broadcast).** The bus controller shall issue a receive command word with 11111 in the RT address field followed by a transmit command to RT A using the RT's address. RT A shall, after command word validation, transmit a status word followed by the specified number of data words. The status and data words shall be transmitted in a contiguous fashion with no gap. The RT(s) with the broadcast option, excluding RT A, shall after message validation, set the broadcast received

bit in the status word as specified in 4.3.3.5.3.7 and shall not transmit the status word.

**4.3.3.6.7.3 Mode command without data word (broadcast).** The bus controller shall issue a transmit command word with 11111 in the RT address field, and a mode code specified in table I. The RT(s) with the broadcast option shall after command word validation, set the broadcast received bit in the status word as specified in 4.3.3.5.3.7 and shall not transmit the status word.

**4.3.3.6.7.4 Mode command with data word (broadcast).** The bus controller shall issue a receive command word with 11111 in the RT address field and a mode code specified in table I, followed by one data word. The command word and data word shall be transmitted in a contiguous fashion with no gap. The RT(s) with the broadcast option shall, after message validation, set the broadcast received bit in the status word as specified in 4.3.3.5.3.7 and shall not transmit the status word.

*Data messages are used to communicate subsystem data to meet the purpose of the integration. As in the control messages, there are two message types: single receiver and multiple receiver messages. These are transmitted in the following manner:*

*Single receiver*

- a. Bus controller to remote terminal
- b. Remote terminal to bus controller
- c. Remote terminal to remote terminal

*Multiple receivers*

- a. Bus controller to multiple remote terminals
- b. Remote terminal to multiple remote terminals

*Each of these messages is transmitted using command and status words for control operation. The command word is used to --*

- a. Identify the receiving terminal(s)
- b. Identify if data are to be received or transmitted by the receiving terminal(s)
- c. Identify the specific message identification (subaddress) within the remote terminal(s)
- d. Notify the terminal(s) of the number of data words to be received or transmitted

*The command word, status word and data word format for accomplishing these messages are described in paragraphs 4.3.3.5.1, 4.3.3.5.2, and 4.3.3.5.3. Using these words, the format for data message transmissions is developed. The single receiver data message formats are shown in figure II-8. The message formats associated with multiple receiving terminals are shown in figure II-9.*



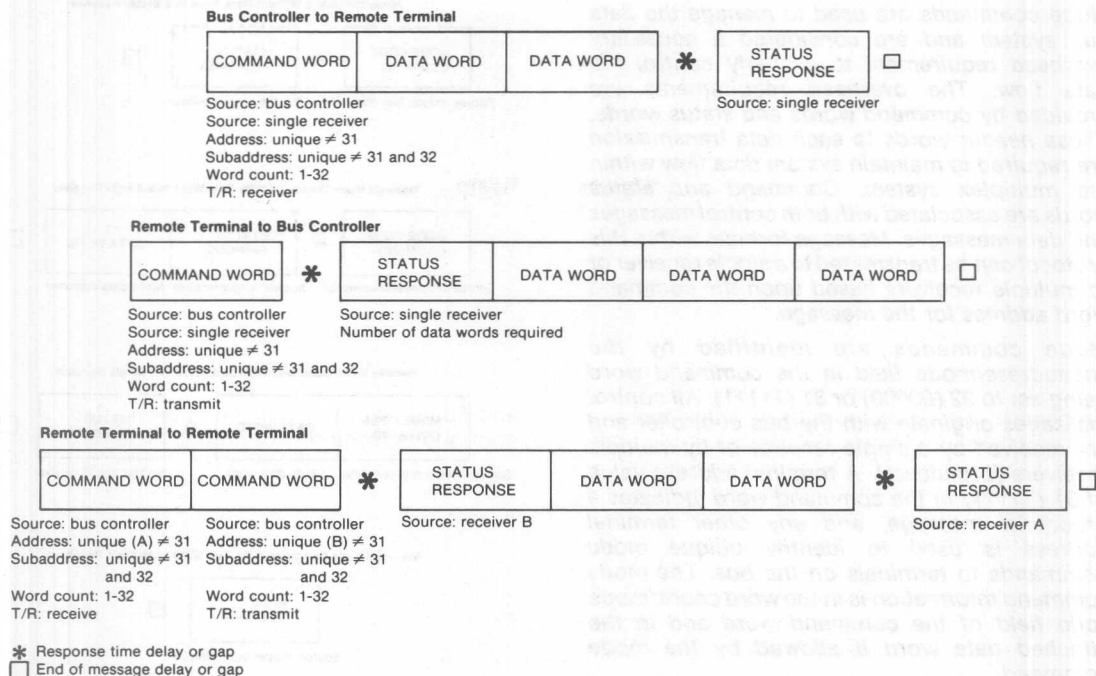


Figure II-8. Single-Receiver Data Message Formats

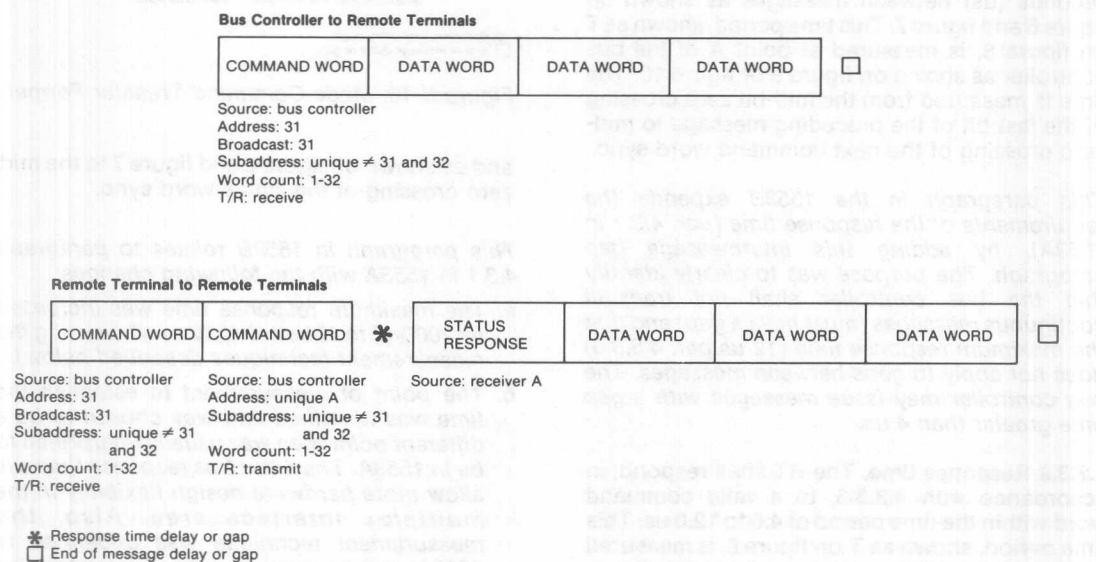


Figure II-9. Multiple-Receiver Data Message Formats



requirement to properly control the data flow. The overhead requirements are provided by command words and status words. These header words to each data transmission are required to maintain system data flow within the multiplex system. Command and status words are associated with both control messages and data messages. Message formats within this protocol can be transmitted to a single receiver or to multiple receivers based upon the command word address for the message.

Mode commands are identified by the subaddress/mode field in the command word being set to 32 (00000) or 31 (11111). All control messages originate with the bus controller and are received by a single receiver or by multiple receivers (broadcast). A terminal address value of 31 (11111) in the command word indicates a broadcast message, and any other terminal address is used to identify unique mode commands to terminals on the bus. The mode command information is in the word count/mode code field of the command word and in the attached data word if allowed by the mode command.

The various legal mode commands without and with data word are illustrated in figure II-10.

**4.3.3.7 Intermessage gap.** The bus controller shall provide a minimum gap time of 4.0 microseconds (us) between messages as shown on figure 6 and figure 7. This time period, shown as T on figure 8, is measured at point A of the bus controller as shown on figure 9 or figure 10. The time is measured from the mid-bit zero crossing of the last bit of the preceding message to mid-zero crossing of the next command word sync.

This paragraph in the 1553B expands the requirements of the response time (par. 4.3.1 in 1553A), by adding this intermessage gap paragraph. The purpose was to clearly identify that the bus controller shall not transmit contiguous messages (must have a gap) and that the maximum response time (12 us par. 4.3.3.8) does not apply to gaps between messages. The bus controller may issue messages with a gap time greater than 4 us.

**4.3.3.8 Response time.** The RT shall respond, in accordance with 4.3.3.6, to a valid command word within the time period of 4.0 to 12.0 us. This time period, shown as T on figure 8, is measured at point A of the RT as shown on figure 9 or figure 10. The time is measured from the mid-bit zero crossing of the last word as specified in 4.3.3.6

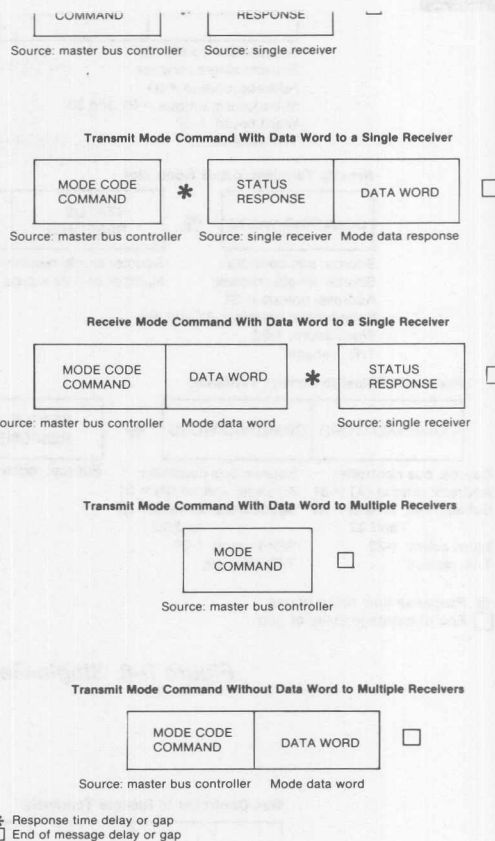


Figure II-10. Mode Command Transfer Formats

and as shown on figure 6 and figure 7 to the mid-zero crossing of the status word sync.

This paragraph in 1553B relates to paragraph 4.3.1 in 1553A with the following changes:

- The maximum response time was increased by 100% (5 to 10 us or 7 to 12 us when using the measurement techniques described below).
- The point of measurement to establish the time was identified and was chosen to be a different point than was usually interpreted to be in 1553A. The 4 to 12 us response time will allow more hardware design flexibility in the multiplex interface area. Also, the measurement technique was undefined in 1553A and because it is hard to determine when the multiplex line is quiet (dead), the measurement is easier to make if the previous

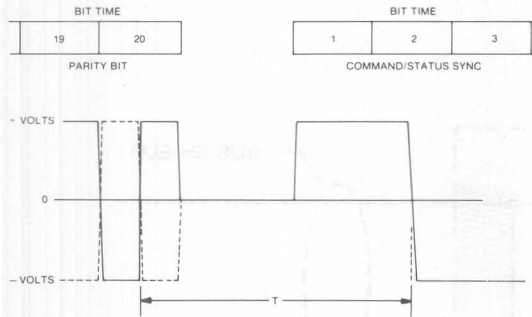


Figure 8 of 1553B. Intermessage Gap and Response Time

*mid-bit (zero) crossing and next mid-bit crossing are examined.*

**4.3.3.9 Minimum no-response time-out.** The minimum time that a terminal shall wait before considering that a response as specified in 4.3.3.8 has not occurred shall be 14.0 us. The time is measured from the mid-bit zero crossing of the last bit of the last word to the mid-zero crossing of the expected status word sync at Point A of the terminal as shown on figure 9 or figure 10.

*This new requirement of 1553B is provided to clarify the minimum time that a bus controller shall wait before concluding that the RT is not going to respond as requested. This is measured from the end of its transmission (last mid-bit crossing) to the expected response (first mid-bit crossing). Notice that this represents the minimum wait time on the same bus where the previous message was requested from the RT.*

#### 4.4 TERMINAL OPERATION

This paragraph in 1553B was provided to clarify the various terminals identified in the standard and their performance requirements. The first section covers common operational requirements that apply to all devices connected to the data bus system. Specific requirements include bus controller (par. 4.4.2), remote terminal (par. 4.4.3), and bus monitor (par. 4.4.4).

**4.4.1 Common operation.** Terminals shall have common operating capabilities as specified in the following paragraphs.

**4.4.1.1 Word validation.** The terminal shall insure that each word conforms to the following minimum criteria:

- The word begins with a valid sync field.
- The bits are a valid Manchester II code.
- The word parity is odd.

When a word fails to conform to the preceding criteria, the word shall be considered invalid.

**4.4.1.2 Transmission continuity.** The terminal shall verify that the message is contiguous as defined in 4.3.3.6. Improperly timed data syncs shall be considered a message error.

**4.4.1.3 Terminal fail-safe.** The terminal shall contain a hardware implemented time-out to preclude a signal transmission of greater than 800.0 us. This hardware shall not preclude a correct transmission in response to a command. Reset of this time-out function shall be performed by the reception of a valid command on the bus on which the time-out has occurred.

*This paragraph describes the common operation associated with terminals connected to the data bus system. The performance requirements include: word validation, transmission continuity, and terminal fail-safe.*

*The word validation paragraph has been modified to explain more fully the detection and response required. These requirements are contained in 1553B paragraphs (word validation, 4.4.1.1), (transmission continuity, 4.4.1.2), and (invalid data reception, 4.4.3.6). The new and modified paragraphs should provide sufficient information concerning invalid words or invalid messages.*

*The terminal fail-safe requirement prevents excessive transmissions on a data bus by a single transmitter, which would preclude its effective use. Changes in 1553B to 800 us (par 4.4.1.3) instead of 660 us (par. 4.3.2) will allow less accurate analog or relaxed digital timers with more independence of the timer circuits to be used in the current design. In addition, there were several mechanisms to reset this fail-safe timer described in 1553B. These include the following:*

- Reset of this timeout function shall be performed by the reception of a valid command on the bus on which the timeout has occurred (par. 4.4.1.3).*
- The mode command override transmitter shutdown (00101 for two-bus system or 10101 for multiple-bus system) on an alternative bus can also be used to reset the timer.*
- The mode command reset remote terminal (01000) causes the remote terminal to assume a power-up initialized state that can also be used to reset the timer.*

*Both b and c are optional ways to reset the timer and may depend on the system and hardware implementations. However, the preferred reset approach is to transmit the appropriate mode code.*

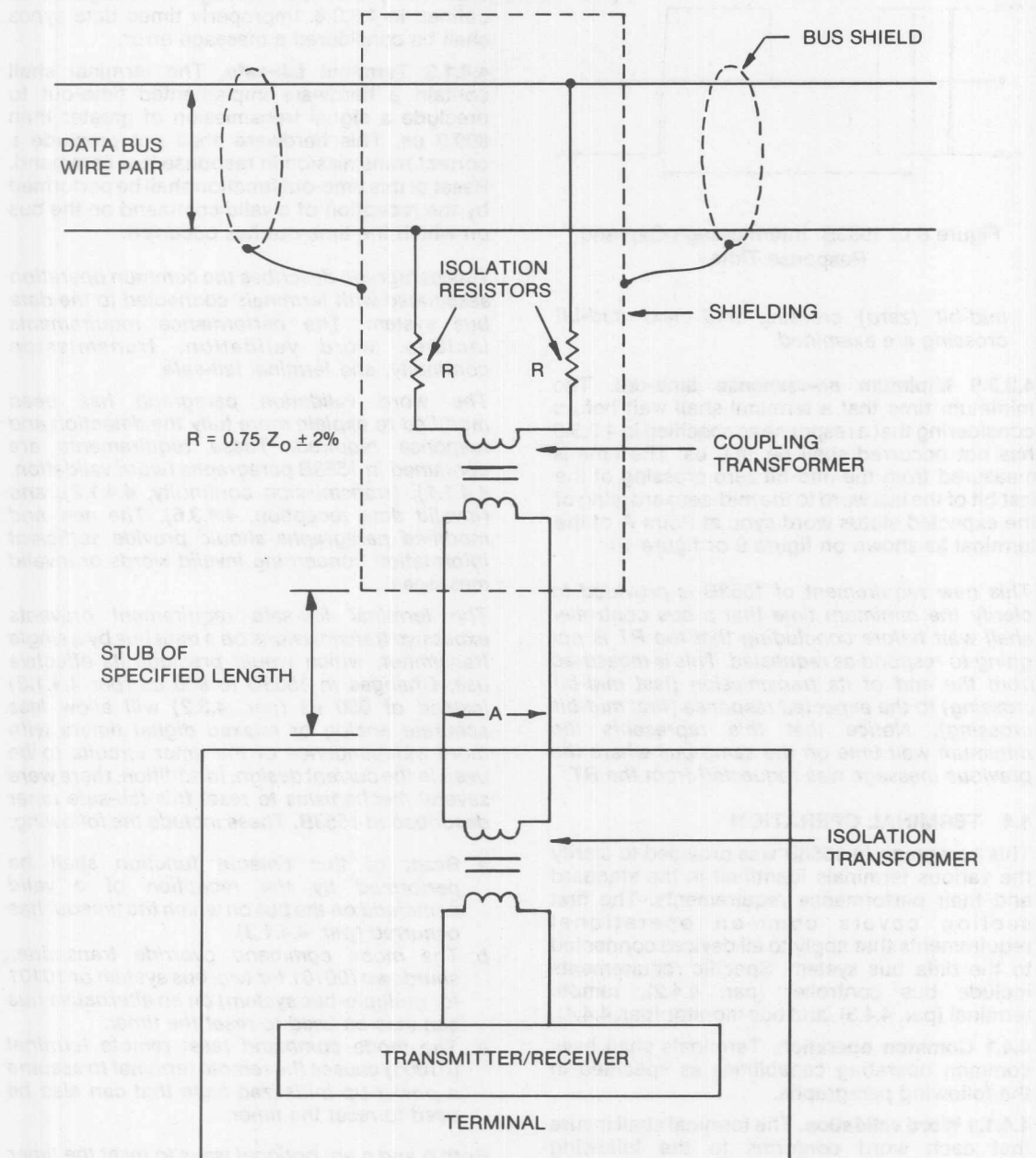


Figure 9 of 1553B. Data Bus Interface Using Transformer Coupling



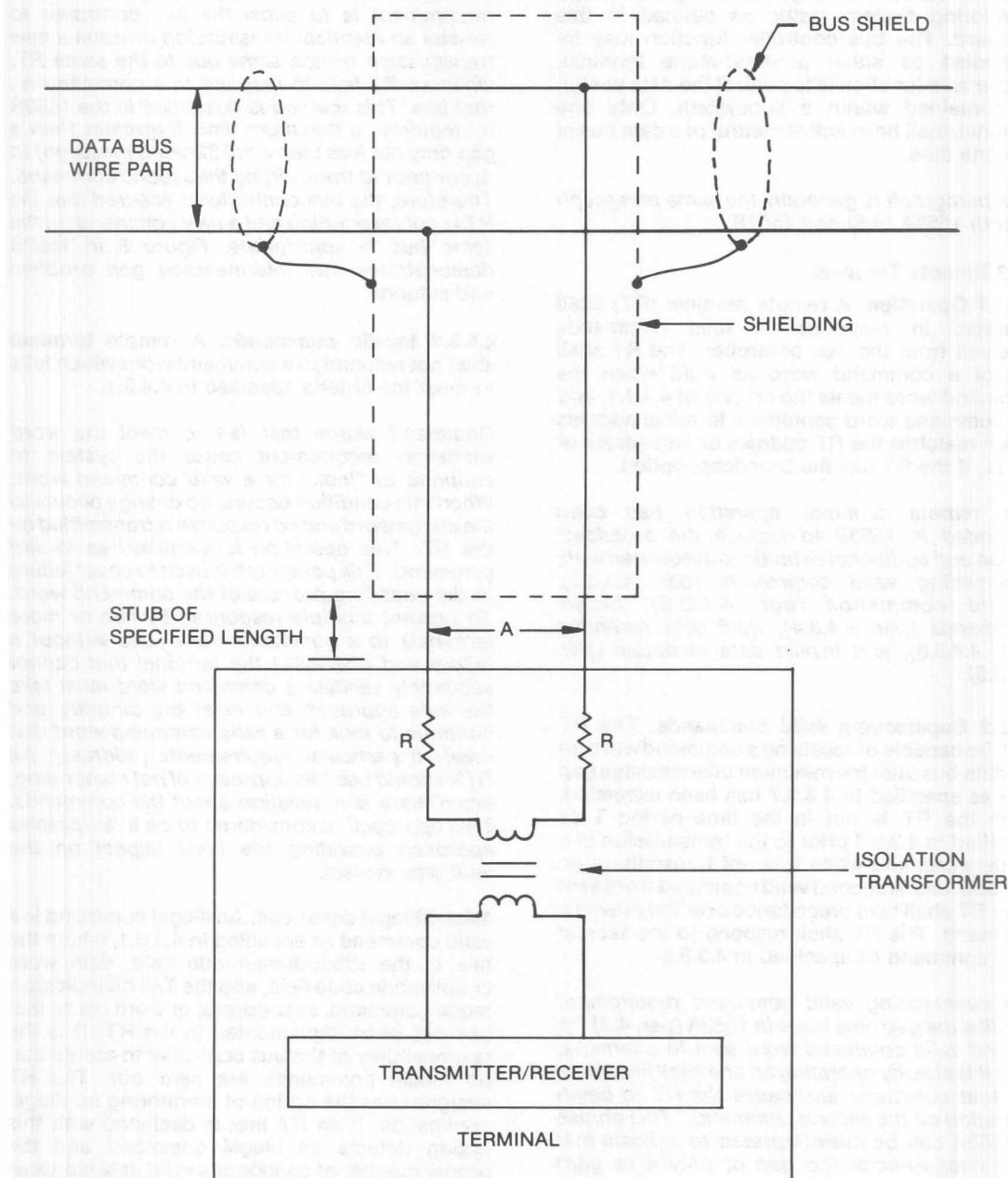


Figure 10 of 1553B. Data Bus Interface Using Direct Coupling

operating as a bus controller shall be responsible for sending data bus commands, participating in data transfers, receiving status responses, and monitoring system status as defined in this standard. The bus controller function may be embodied as either a stand-alone terminal, whose sole function is to control the data bus(s), or contained within a subsystem. Only one terminal shall be in active control of a data bus at any one time.

*This paragraph is generally the same paragraph in both 1553A (4.5) and 1553B.*

#### **4.4.3 Remote Terminal**

**4.4.3.1 Operation.** A remote terminal (RT) shall operated in response to valid commands received from the bus controller. The RT shall accept a command word as valid when the command word meets the criteria of 4.4.1.1, and the command word contains a terminal address which matches the RT address or an address of 11111, if the RT has the broadcast option.

*The remote terminal operation has been expanded in 1553B to include the broadcast option and additional definitions associated with: superseding valid commands (par. 4.4.3.2), invalid commands (par. 4.4.3.3), illegal commands (par. 4.4.3.4), valid data reception (par. 4.4.3.6), and invalid data reception (par. 4.4.3.6).*

**4.4.3.2 Superseding valid commands.** The RT shall be capable of receiving a command word on the data bus after the minimum intermessage gap time as specified in 4.3.3.7 has been exceeded, when the RT is not in the time period T as specified in 4.3.3.8 prior to the transmission of a status word, and when it is not transmitting on that data bus. A second valid command word sent to an RT shall take precedence over the previous command. The RT shall respond to the second valid command as specified in 4.3.3.8.

*The superseding valid command requirement clarifies the gap time issue in 1553A (par. 4.3). "A second valid command word sent to a terminal after it is already operating on one shall invalidate the first command and cause the RT to begin operation on the second command." This phrase in 1553A can be misinterpreted to indicate that near back-to-back (no gap or only 4 us gap) commands can be sent to a terminal on the same bus and the terminal will respond to the second command.*

*However, this was not the intention because in*

*word slightly greater than 4 us would collide with the second command being transmitted by the bus controller. The intended purpose for this requirement is to allow the bus controller to reissue an identical transmission or issue a new transmission on the same bus to the same RT, when an RT fails to respond to a command on that bus. This method is described in the 1553B by requiring a minimum time T (greater than a gap time but less than a full 32-word message) to occur prior to transmitting the second command. Therefore, the bus controller is assured that the RT is not responding and a new command on the same bus is appropriate. Figure 8 in 1553B demonstrates this intermessage gap problem and solution.*

**4.4.3.3 Invalid commands.** A remote terminal shall not respond to a command word which fails to meet the criteria specified in 4.4.3.1.

*Command words that fail to meet the word validation requirement cause the system to continue to "look" for a valid command word. When this condition occurs, no change occurs to the status word and no response is transmitted by the RT. This operation is identified as invalid command. This paragraph is used to cover failure in the decoding process of the command word. To prevent multiple responses by two or more terminals to a command word (one without a failure and one with) the terminal that cannot absolutely validate a command word must take the safe approach and reset the circuitry and continue to look for a valid command word that meets its particular requirements (address). All RT's should use this approach of not responding, when there is a question about the commands. This approach is considered to be a fail-passive approach providing the least impact on the multiplex system.*

**4.4.3.4 Illegal command.** An illegal command is a valid command as specified in 4.4.3.1, where the bits in the subaddress/mode field, data word count/mode code field, and the T/R bit indicate a mode command, subaddress, or word count that has not been implemented in the RT. It is the responsibility of the bus controller to assure that no illegal commands are sent out. The RT designer has the option of monitoring for illegal commands. If an RT that is designed with this option detects an illegal command and the proper number of contiguous valid data words as specified by the illegal command word, it shall respond with a status word only, setting the message error bit, and not use the information received.

*Illegal commands are command words that have passed the word validation test but do not comply with the system's capability. These include command words where the subaddress-mode field, data word/code code field, or the T/R bit are set so that they represent conditions not allowed in the system. These include both conditions not allowed by the standard and any additional condition not allowed in a particular system design. The responsibility for not allowing illegal commands to be transmitted is given to the bus controllers. Since the bus controller is responsible for all command/response message communications, it will be a design goal that the bus controller not transmit an invalid command.*

*Two methods can be provided to meet this requirement: (1) careful generation of bus controller commands in the development of the system and tight control of the change process during operational use and (2) examination of failure modes of the controller hardware and software to determine potentially illegal command generations and transmissions. An additional method of rejecting illegal commands in the multiplex system can only be provided by circuitry within the receiving remote terminal. This approach is an optional capability for remote terminals built to the 1553B standard. If an RT with this capability detects an illegal command that meets all other validation requirements, the RT shall respond with a status word with only the message error bit set and not use the information sent or disregard the request for information.*

**4.4.3.5 Valid data reception.** The remote terminal shall respond with a status word when a valid command word and the proper number of contiguous valid data words are received, or a single valid word associated with a mode code is received. Each data word shall meet the criteria specified in 4.4.1.1.

*The purpose of the valid data reception in 1553B was to clearly state when a message containing at least one data word would be responded to by the appropriate RT. Previous systems have taken different approaches to messages with various failures (e.g., under word count, over word count, parity errors in words, gaps in word transmissions). Therefore, this requirement was established to identify the only time status words would be transmitted by the RT after the reception of a data message with at least one data word. It should be noted that one other message format will produce a status word response: mode code without data word transmitted to a specific RT (not broadcast).*

**4.4.3.6 Invalid data reception.** Any data word(s) associated with a valid receive command that does not meet the criteria specified in 4.4.1.1 and 4.4.1.2 or an error in the data word count shall cause the remote terminal to set the message error bit in the status word to a logic one and suppress the transmission of the status word. If a message error has occurred, then the entire message shall be considered invalid.

*In contrast to the valid data reception status response, certain action is required when an invalid data reception occurs. This paragraph in 1553B is an expanded version of the two 1553A paragraphs 4.2.5.4.4 and 4.2.3.5.3.3. This again assumes message formats with associated data word(s), thus mode code commands without a data word are rightly excluded from this group; however, in contrast to valid data reception where broadcast message protocol were excluded, here they are included. Therefore, all message formats containing a least one data word (e.g., broadcast data messages, nonbroadcast data messages, broadcast mode codes with a data word, and mode codes with a data word) are included in this requirement. As stated in the requirement, the message command word has been validated and the error occurs in the data word portion of the message. The withholding or suppression of the status response alerts the bus controller error detection electronics to the fact that an incomplete message has occurred and some level of error recovery must occur. The setting of the message error bit in the status that remains in the RT will provide additional information to the error recovery circuitry only if the bus controllers request the status word using the appropriate mode code.*

*Also notice that the requirement is that the entire received message be considered invalid. This message invalidation requirement may cause some systems like electrical multiplex (EMUX) a problem. Since the EMUX system usually have bit-oriented data rather than word or multiple words (message) oriented data, errors in a word following the reception of good data will invalidate good data. It has been proposed that such a system invalidate all data words from the failure to the end of the message and use previously good data words. This approach, however, has not been allowed. Regardless of the approach, some system mechanisms will store the data and then tag the message as being invalid; others will not allow the user to receive the data. In the first case, it is the responsibility of the user to examine the message valid indication prior to using the data; however, in the second*

case, the user must recognize that the data has not been updated.

**4.4.4 Bus monitor operation.** A terminal operating as a bus monitor shall receive bus traffic and extract selected information. While operating as a bus monitor, the terminal shall not respond to any message except one containing its own unique address if one is assigned. All information obtained while acting as a bus monitor shall be strictly used for off-line applications (e.g., flight test recording, maintenance recording or mission analysis) or to provide the back-up bus controller sufficient information to take over as the bus controller.

*A terminal may operate in the bus monitor mode for two reasons: (1) information recording for offline analysis and (2) information source for backup bus controller. The unique feature of this mode is that it has the ability to decode and accept for data storage any or all messages transmitted on the data bus without the knowledge of or without affecting the operation of multiplex system or the terminal(s) attached to the bus. It also has the option of not being addressable as a terminal attached to the bus. If this is the case, it acts in the "listen capability only" to the system. In this implementation, data cannot be sent to it specifically, but the monitor may collect data by recording message traffic. However, the same terminal may operate in the remote terminal and potential bus controller (backup bus controller) mode as well as having the additional capability to monitor and store all message traffic or an internally derived subset of all messages. It is because of this second capability, its nonpassive nature, that a terminal with the monitor mode is an extremely powerful device in the multiplex system.*

#### 4.5 Hardware Characteristics

*The following discussion will provide a summary and comparison of MIL-STD-1553A/B requirements that have significant effect on the hardware characteristics (1553, par. 4.5). A detailed comparison of these subparagraphs in 1553A and 1553B is provided in tables II-2 and II-3.*

The hardware characteristic section of 1553B examines data bus characteristics (par. 4.5.1) and terminal characteristics (par. 4.5.2). This section is similar to the terminal operation paragraphs (4.3) and the transmission line (4.2.4) of 1553A. Paragraph 4.4 in 1553A (Terminal to Subsystem Interface) has been deleted from 1553B completely. This deletion was consistent

with the emphasis on a data bus protocol standard and an electrical multiplex interface requirement treating the terminals interfacing to the multiplex bus as black box interfaces and not defining any internal interfaces.

#### 4.5.1 Data Bus Characteristics

**4.5.1.1 Cable.** The cable used for the main bus and all stubs shall be a two conductor, twisted, shielded, jacketed cable. The wire-to-wire distributed capacitance shall not exceed 30.0 picofarads per foot. The cables shall be formed with not less than four twists per foot where a twist is defined as a 360 degree rotation of the wire pairs; and, the cable shield shall provide a minimum of 75.0 percent coverage.

**4.5.1.2 Characteristic impedance.** The nominal characteristic impedance of the cable ( $Z_0$ ) shall be within the range of 70.0 Ohms to 85.0 Ohms at a sinusoidal frequency of 1.0 megahertz (MHz).

**4.5.1.3 Cable attenuation.** At the frequency of 4.5.1.2, the cable power loss shall not exceed 1.5 decibels (dB)/100 feet (ft).

*Table II-4 contains a summary listing of the data bus and coupling requirements contained in 1553A and 1553B. The characteristics of the twisted shielded pair cable have been relaxed to allow selection of cable types from a variety of manufacturers. It has been shown that minor variations from the specified cable characteristics do not significantly affect the system performance.*

*A great deal of concern and confusion has resulted because of the cable network requirements, including bus length, coupling, and stubbing. 1553 and 1553A did not provide adequate guidelines for bus network design, especially for the transformer coupled stub. 1553A defined a maximum cable length of 300 ft for the main bus while 1553B chose not to specify a maximum main bus length since it is reasoned that the cable length, number of terminals, and length of stubs are all subject to trade-off and must be considered in the design for reliable system operation. In other words, an arbitrary limit of 300 ft should not be applied since all parameters of the network must be considered.*

**4.5.1.4 Cable termination.** The two ends of the cable shall be terminated with a resistance, equal to the selected cable nominal characteristic impedance ( $Z_0$ )  $\pm$  2.0 percent.

**4.5.1.5 Cable stub requirements.** The cable shall be coupled to the terminal as shown on figure 9 or figure 10. The use of long stubs is discouraged, and the length of a stub should be minimized.



Table II-2. Comparison of Data Bus Characteristics

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
1. Twisted, shielded, jacketed	Yes 4.2.4.1	Yes 4.5.1.1
2. Minimum cable shield coverage	80% 4.2.4.1	75% 4.5.1.1
3. Minimum cable twist	1 twist/in (12 twists/ft) 4.2.4.1	4 twists/ft 4.5.1.1
4. Wire-to-wire distributed capacitance (maximum)	30 pF/ft 4.2.4.1	30 pF/ft 4.5.1.1
5. Characteristic impedance of cable	70 $\pm$ 10% at 1 MHz 4.2.4.2	Nominal 70 to 85 at 1 MHz 4.5.1.2
6. Cable attenuation	1 dB/100 ft at 1 MHz 4.2.4.3	1.5 dB/100 ft at 1 MHz 4.5.1.3
7. Cable length	300 ft maximum 4.2.4.4	Unspecified —
8. Cable termination using a resistance at both ends	Characteristic impedance 4.2.4.6	Nominal characteristic impedance $\pm$ 2% 4.5.1.4
9. Cable stubbing	Transformer coupling for stubs longer than 1 ft but less than 20 ft; direct coupling if stub is less than 1 ft; maximum stub length of 20 ft 4.2.4.5 Figure II-14	Transformer coupling or direct coupling allowed; maximum stub length suggested 20 ft 4.5.1.5.1 or 4.5.1.5.2 Figures 9 or 10 or 1553B
10. Cable coupling (connector)	Compatible with Amphenol type 31-235 or Trompeter type TEI-14949-E137 receptacles and Amphenol type 31-224 or Trompeter type TEI-14949-PL36 plugs 4.2.4.6	Unspecified —

Table II-2. Comparison of Data Bus Characteristics (Continued)

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
11. Cable coupling shielded box	Shielded coupler box 4.2.4.6	75% coverage, minimum 4.5.1.5.1.3 and 4.5.1.5.2.2
12. Coupling transformer turns ratio	Unspecified —	1:1.4 $\pm$ 3% higher turns on isolation resistor side of stub 4.5.1.5.1.1
13. Transformer open circuit impedance	Unspecified —	3,000 ohms over frequency of 75 kHz -1 MHz with 1V RMS sine wave 4.5.1.5.1.1.1
14. Transformer waveform integrity	Unspecified —	Droop not to exceed 20% overshoot and ringing less than $\pm$ 1V peak undertest of figure 11 of 1553B 4.5.1.5.1.1.2
15. Transformer common mode rejection	Unspecified —	45 dB at 1MHz 4.5.1.5.1.1.3
16. Fault isolation — Isolation resistor in series with data bus cable (coupler)	$R = 0.75Z_o^* \pm 5\%$ 4.2.5.2	$R = 0.75Z_o^* \pm 2\%$ 4.5.1.5.1.2
Direct coupled case with the isolation resistor in the RT	Figure II-14	$R = 55 \text{ ohms} \pm 2\%$ 4.5.1.5.2.1 Figure 10 of 1553B
17. Impedance across the data bus for any failure of coupling transformer, cable stub, or terminal receiver and transmitter transformer coupling	No less than $1.5Z_o^*$ 4.2.5.2	No less than $1.5Z_o^*$ 4.5.1.5.1.2
Direct coupling		No less than 110 ohms 4.5.1.5.2.3
18. Stub voltage requirements and input level transformer coupling	**Range of the 0.5V to 10V peak; 1.0V to 20V p-p, I-I 4.2.5.4.1 Figure II-14	**Range of 1.0V to 14.0V p-p**, I-I with one fault as stated in 17 above 4.5.1.5.1.4 Figure 9 of 1553B

\* $Z_o$  = cable normal characteristic impedance

\*\*Assumes one fault of a coupling transformer, cable stub, or terminal receiver or transmitter

Table II-2. Comparison of Data Bus Characteristics (Concluded)

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
Direct coupling	**Range of the 0.5V to 10V peak; 1.0V to 20V p-p, I-I 4.2.5.4.1 Figure II-14	**Range of 1.4V to 20V p-p, I-I with one fault as stated in 17 above 4.5.1.5.2.3 Figure 10 of 1553B
19. Wiring and cabling for electromagnetic capability	MIL-E-6051 4.2.4.7 MIL-STD-1553A	MIL-E-6051 4.5.1.5.3 MIL-STD-1553B

\*\*Assumes one fault of a coupling transformer, cable stub, or terminal receiver or transmitter

Table II-3. Comparison of Terminal Characteristics

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
1. Output level — transformer coupling	$\pm 3.0\text{V}$ to $\pm 10\text{V}$ peak (6.0V to 20.0V p-p) I-I with no faults; with one fault of a coupling transformer, cable stub, or terminal receiver-transmitter, $\pm 2.25\text{V}$ to $\pm 11.25\text{V}$ peak (4.5V to 15V p-p) I-I 4.2.5.3.1	With $R_L = 70 \pm 2\%$ , 18.0V to 27.0V p-p, I-I  4.5.2.1.1.1 Figure 12 of 1553B With $R_L = 35 \pm 2\%$ , 6.0V to 9.0V p-p, I-I 4.5.2.2.1.1 Figure 12 of 1553B
Direct coupling		Figure 12 of 1553B $\pm 25\text{ ns}$ 4.5.2.1.1.2 Figure 12 of 1553B 100 to 300 ns 4.5.2.1.1.2 Figure 13 of 1553B $\pm 90\text{-mV}$ peak, I-I 4.5.2.1.1.2 Point A, figure 12 of 1553B $\pm 300\text{-mV}$ peak, I-I 4.5.2.2.1.2 Point A, figure 12 of 1553B 14-mV, RMS, I-I 4.5.2.1.1.3 Point A, figure 12 of 1553B
2. Output waveform — Zero crossing deviation	$\pm 25\text{ ns}$ 4.2.5.3.2 Point C, figure II-14 and figure 13 of 1553B	
Rise and fall time (10% to 90%)	$\geq 100\text{ ns}$ 4.2.5.3.2 Figure 13 of 1553B	
Transformer coupling distortion (including overshoot and ringing)	Unspecified	
Direct coupling distortion (including overshoot and ringing)	Unspecified	
3. Output noise — Transformer coupling	10-mV p-p, I-I 4.2.5.3.3 Point A, figure II-14	



Table II-3. Comparison of Terminal Characteristics (Continued)

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
Direct coupling		5-mV, RMS, I-I 4.5.2.2.1.3 Point A, figure 12 of 1553B
4. Output symmetry (after 2.5 $\mu$ s of midbit crossing of the last parity bit — Transformer coupling)	Unspecified	$\pm 250$ -mV peak, I-I 4.5.2.1.1.4 Point A, figure 12 of 1553B
Direct coupling	Unspecified	$\pm 90$ -mV peak, I-I 4.5.2.2.1.4 Point A, figure 12 of 1553B
5. Input waveform — Maximum zero crossing deviation	Unspecified	$\pm 150$ ns 4.5.2.1.2.1 Point A, figures 9 or 10 of 1553B
6. Input signal response range Transformer coupling	$\pm 0.5$ V to $\pm 10.0$ V peak (1.0V to 20V p-p), I-I 4.2.5.4.1 Point C, figure II-14	0.86V to 14.0V p-p, I-I 4.5.2.1.2.1 Point A, figure 9 of 1553B
Direct coupling		1.2V to 20V p-p, I-I 4.5.2.2.2.1 Point A, figure 10 of 1553B
7. Input signal no response range Transformer coupling	Unspecified	0.0V to 0.2V p-p, I-I 4.5.2.1.2.1 Point A, figure 9 of 1553B
Direct coupling	Unspecified	0.0V to 0.28V p-p, I-I 4.5.2.2.2.1 Point A, figure 10 of 1553B

Table II-3. Comparison of Terminal Characteristics (Concluded)

Requirement	Requirement and MIL-STD-1553A paragraph	Requirement and MIL-STD-1553B paragraph
8. Common mode rejection	$\pm 10.0\text{V}$ peak, line-to-ground, dc to 2 MHz 4.2.5.4.2 Point A, figure II-14	$\pm 10.0\text{V}$ peak, line-to-ground, dc to 2 MHz 4.5.2.1.2.2 or 4.5.2.2.2.2 Point A, figures 9 or 10 of 1553B
9. Input impedance — Transformer coupling	Minimum of 2,000 ohms over a frequency range of 100 kHz to 1 MHz, I-I 4.2.5.4.3 Point C, figure II-14	Minimum of 1,000 ohms over a frequency range of 75 kHz to 1 MHz, I-I 4.5.2.1.2.3 Point A, figure 9 of 1553B
Direct coupling		Minimum of 2,000 ohms over a frequency range of 75 kHz to 1 MHz, I-I 4.5.2.2.2.3 Point A, figure 10 of 1553B
10. Noise rejection or error rate — Transformer coupling	Maximum bit error rate of $10^{-12}$ and a maximum incomplete message rate of $10^{-6}$ in a configuration of one bus controller on a 20-ft stub with a minimum of 100 ft of main bus cable between coupling boxes; test is conducted in presence of magnetic field per MIL-STD-462 method RS02 (spike test) with the limits of MIL-STD-461 RS02 4.3.3	Maximum of one part in $10^7$ word error in the presence of additive white gaussian noise of 140-mV RMS over a bandwidth of 1.0 kHz to 4 MHz; input voltage 2.1V p-p, I-I Point A, figure 9 of 1553B and accept/reject Table II-6
Direct coupling		4.5.2.1.2.4 Maximum of one part in $10^7$ word error rate in the presence of additive white gaussian noise of 200-mV RMS over a bandwidth of 1.0 kHz to 4 MHz; input voltage 3.0V p-p, I-I Point A, figure 10 of 1553B and accept/reject Table II-6 4.5.2.2.2.4

Table II-4. Summary of Data Bus and Coupling Requirements

Parameter	MIL-STD-1553A	MIL-STD-1553B
Transmission line		
• Cable type	Twisted-shielded pair	Twisted-shielded pair
• Capacitance (wire-to-wire)	30 pF/ft, maximum	30 pF/ft, maximum
• Twist	1/in, minimum	4/ft (0.33/in), minimum
• Characteristic impedance ( $Z_o$ )	70 ohms $\pm$ 10% at 1.0 MHz	70 to 85 ohms at 1.0 MHz
• Attenuation	1.0 dB/100 ft at 1.0 MHz, maximum	1.5 dB/100 ft at 1.0 MHz, maximum
• Length of main bus	300 ft, maximum	Not specified
• Termination	Two ends terminated in resistors equal to $Z_o$	Two ends terminated in resistors equal to $Z_o \pm 2\%$
• Shielding	80% coverage, minimum	75% coverage, minimum
Cable coupling		
• Stub definition	Short stub < 1 ft Long stub > 1 to 20 ft (20 ft, maximum)	Short stub < 1 ft Long stub > 1 to 20 ft (may be exceeded)
• Coupler requirement	All connections use external coupler box; connectors specified (ref. <b>fig. I-1.6</b> )	Direct coupled, short stub transformer coupled, long stub (ref. <b>fig. I-1.7</b> )
• Coupler transformer		
• Turns ratio	Not specified	1 to 1.41
• Input impedance	Not specified	3,000 ohms, minimum (75.0 kHz to 1.0 MHz)
• Droop	Not specified	20% maximum (250 kHz)
• Overshoot and ringing	Not specified	$\pm 1.0V$ peak (250-kHz square wave with 100-ns maximum rise and fall time)
• Common mode rejection	Not specified	45.0 dB at 1.0 MHz
• Fault protection	Resistor in series with each connection equal to $(0.75Z_o) \pm 5\%$ ohms	Resistor in series with each connection equal to $(0.75Z_o) \pm 2.0\%$ ohms
• Stub voltage	$\pm 0.5V$ to $\pm 10.0V$ , peak, I-I (1.0V to 20.0V, p-p, I-I); nominal signal level for terminal response	1.0V to 14.0V p-p, I-I, minimum signal voltage (transformer coupled) 1.4V to 20.0V, p-p, I-I, minimum signal voltage (direct coupled)

stub lengths exceeding those lengths specified in 4.5.1.5.1 and 4.5.1.5.2 are permissible.

**4.5.1.5.1 Transformer coupled stubs.** The length of a transformer coupled stub should not exceed 20 feet. If a transformer coupled stub is used, then the following shall apply.

**4.5.1.5.1.1 Coupling transformer.** A coupling transformer, as shown on figure 9, shall be required. This transformer shall have a turns ratio of 1:1.41  $\pm$  3.0 percent, with the higher turns on the isolation resistor side of the stub.

*A generalized multiplex bus network configuration is shown in figure 1 of 1553B. The main bus is terminated at each end in the cable characteristic impedance to minimize reflections caused by transmission line mismatch. With no stubs attached, the main bus looks like an infinite length transmission line and therefore there are no disturbing reflections. When the stubs are added for connection of the terminals, the bus is loaded locally and a mismatch occurs with resulting reflections. The degree of mismatch and signal distortions caused by reflections are a function of the impedance (Z) presented by the stub and terminal input impedance. In order to minimize signal distortion, it is desirable that the stub maintain a high impedance. This impedance is reflected back to the main bus. At the same time the impedance needs to be kept low so that adequate signal power will be delivered to the receiver input. Therefore, a trade-off and compromise between these conflicting requirements is necessary to achieve the specified signal-to-noise ratio and system error rate performance. Two methods for coupling a terminal to the main bus are defined in 1553B, transformer coupling and direct coupling. The two methods are shown in figures 9 and 10 of 1553B. Transformer coupling is usually used with long stubs (1 to 20 ft) and requires a coupler box, separate from the terminal, located near the junction of the main bus and stub. Direct coupling is usually limited for use with stubs of less than 1 ft.*

*Fault isolation resistors (R) are included to provide protection for the main bus in case of a short circuit in the stub or terminal. The coupler-transformer characteristics defined in 1553B and listed in table 7-4 provide a compromise between the signal level and distortion characteristics delivered to the terminals. The coupler transformer turns ratio (1:1.41) provides impedance transformation for both terminal reception and transmission. The improvement of stub load impedance is a result of impedance*

*square of the turns ratio, assuming an ideal coupler transformer.*

*As indicated above, the 1:1.41 transformer also provides ideal termination of the stub for transmission of signals from the terminal to the main bus. The impedance at main bus is*

$$Z_B = \frac{Z_o}{2} + 2R \quad (1)$$

*where*

$$R = 0.75 Z_o$$

$$Z_B = 0.5Z_o + 1.5Z_o = 2Z_o \text{ ohms} \quad (2)$$

*The reflected impedance,  $Z_R$ , from the bus to the stub due to the transformer impedance transformation is*

$$Z_R = \frac{Z_B}{2} = \frac{2Z_o}{2} = Z_o \quad (3)$$

*Therefore, the coupler transformer specified in 1553B provides the characteristics desired for reducing reflections and maintaining signal levels for systems where long stubs are required.*

**4.5.1.5.1.1 Transformer input impedance.** The open circuit impedance as seen at point B on figure 11 shall be greater than 3000 Ohms over the frequency range of 75.0 kilohertz (kHz) to 1.0 megahertz (MHz), when measured with a 1.0V root-mean-square (RMS) sin wave.

*The transformer open circuit impedance ( $Z_{oc}$ ) is required to be greater than 3k ohms in 1553B systems. The measurement is made looking into the higher turns winding (1.41) with a 75 kHz to 1 MHz sine wave signal. The test amplitude at the transformer winding is adjusted to 1V rms. The critical factors in achieving the 3k ohm  $Z_{oc}$  is the distributed capacitance of the windings and the transformer primary inductance. The inductance of the transformer must be large enough to provide the open circuit impedance at 75 kHz, and the distributed capacitance should be small enough to maintain the open circuit impedance at the 1 MHz test frequency. The inductance may obviously be increased by increasing the number of turns on the transformer. This technique, however, tends to increase the distributed capacitance, degrading high frequency performance and therefore causing waveform integrity and common mode rejection to suffer.*

**4.5.1.5.1.2 Transformer waveform integrity.** The droop of the transformer using the test configuration shown on figure 11 at point B, shall



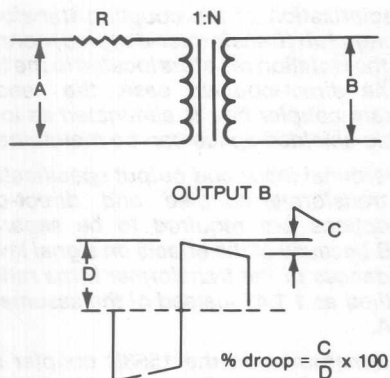


Figure 11 of 1553B. Coupling Transformer

not exceed 20.0 percent. Overshoot and ringing as measured at point B shall be less than  $\pm 1.0V$  peak. For this test, R shall equal 360.0 ohms  $\pm 5.0$  percent and the input A of figure 11 shall be a 250.0 kHz square wave, 27.0V peak-to-peak, with a rise and fall time no greater than 100 nanoseconds (ns).

The ability of the coupler transformer to provide a satisfactory signal is specified in the droop, overshoot, and ringing requirements of 1553B shown in figure II-11. Droop is specified at 20% maximum when driving the transformer with a 250 kHz, 27V p-p square wave. The test for the droop characteristic is made by driving the low turns winding through a 360 ohm resistor and measuring the signal at the open-circuited high side winding. The droop of the transformer is determined mainly by the primary inductance. Since the primary inductance also provides the 3k ohm open circuit impedance, the inductance should be made as high as possible without degrading the high-frequency performance of the transformer. Ringing and overshoot on the transformer signal is also shown in figures II-11. The  $\pm 1V$  limit on these high-frequency perturbations can be achieved through careful attention to leakage inductance and transformer capacitance.

**4.5.1.5.1.1.3 Transformer common mode rejection.** The coupling transformer shall have a common mode rejection ratio greater than 45.0 dB at 1.0 MHz.

The common mode rejection of the isolation transformer is required to be greater than 45.0dB. The common mode test shown in figure II-12 consists of driving the high turns winding while measuring the differential signal across the high

side. Common mode rejection can be improved by minimizing the interwinding capacitance and the core-to-winding capacitance.

**4.5.1.5.1.2 Fault isolation.** An isolation resistor shall be placed in series with each connection to the data bus cable. This resistor shall have a value of  $0.75 Z_o$  plus or minus 2.0 percent, where  $Z_o$  is the selected cable nominal characteristic impedance. The impedance placed across the data bus cable shall be no less than  $1.5Z_o$  failure of the coupling transformer, cable stub, or terminal transmitter/receiver.

**4.5.1.5.1.3 Cable coupling.** All coupling transformers and isolation resistors, as specified in 4.5.1.5.1.1 and 4.5.1.4.1.2, shall have continuous shielding which will provide a minimum of 75 percent coverage. The isolation resistors and coupling transformers shall be placed at minimum possible distance from the junction of the stub to the main bus.

**4.5.1.5.1.4 Stub voltage requirements.** Every data bus shall be designed such that all stubs at point A of figure 9 shall have a peak-to-peak amplitude, line-to-line within the range of 1.0 and 14.0V for a transmission by any terminal on the data bus. This shall include the maximum reduction of data bus signal amplitude in the event that one of the terminals has a fault which causes it to reflect a fault impedance specified in 4.5.1.5.1.2 on the data bus. This shall also include the worst case output voltage of the terminals as specified in 4.5.2.1.1.1 and 4.5.2.2.1.1.

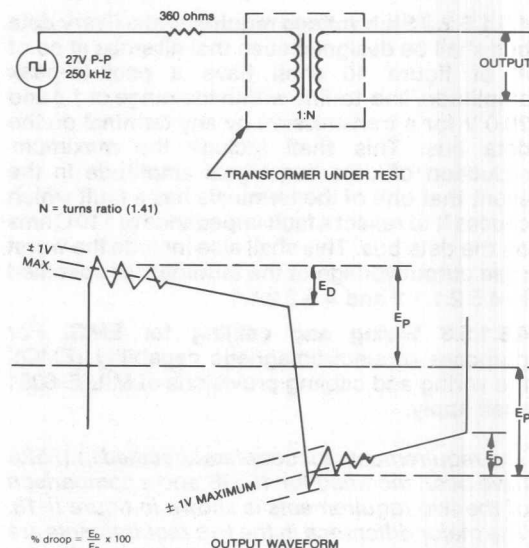


Figure II-11. Waveform Test

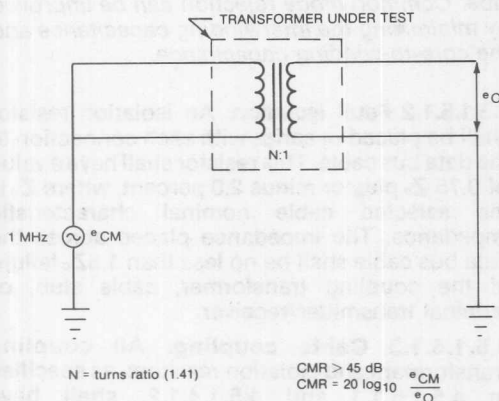


Figure 11-12. Common Mode Test

**4.5.1.5.2 Direct coupled stubs.** The length of a direct coupled stub should not exceed 1 foot. Refer to 10.5 for comments concerning direct coupled stubs. If a direct coupled stub is used, then the following shall apply.

**4.5.1.5.2.1 Fault isolation.** An isolation resistor shall be placed in series with each connection to the data bus cable. This resistor shall have a value of 55.0 Ohms plus or minus 2.0 percent. The isolation resistors shall be placed within the RT as shown on figure 10.

**4.5.1.5.2.2 Cable coupling.** All bus-stub junctions shall have continuous shielding which will provide a minimum of 75 percent coverage.

**4.5.1.5.2.3 Stub voltage requirements.** Every data bus shall be designed such that all stubs at point A of figure 10 shall have a peak-to-peak amplitude, line-to-line within the range of 1.4 and 20.0 V for a transmission by any terminal on the data bus. This shall include the maximum reduction of data bus signal amplitude in the event that one of the terminals has a fault which causes it to reflect a fault impedance of 110 Ohms on the data bus. This shall also include the worst case output voltage of the terminals as specified in 4.5.2.1.1.1 and 4.5.2.2.1.1.

**4.5.1.5.3 Wiring and cabling for EMC.** For purposes of electromagnetic capability (EMC), the wiring and cabling provisions of MIL-E-6051 shall apply.

*The requirements for couplers specified in 1553A have been modified for 1553B and a comparison of the two requirements is shown in figure 11-13. The major difference in the two requirements are the placement of the isolation resistors for the direct-coupled (short-stub) connection and the*

*characterization of the coupling transformer in the long-stub (transformer-coupled) connection. With the isolation resistors located in the terminal for the direct-coupled case, the need for a separate coupler box is eliminated as long as a reliable shielded splice can be maintained.*

*The terminal input and output specifications for the transformer-coupled and direct-coupled connections are required to be separated in 1553B because of the effects on signal levels and impedances of the transformer turns ratio being specified as 1:1.41 instead of the assumed 1:1 in 1553A.*

*The transformer in the 1553B coupler has the turns ratio of 1:1.41. This ratio, together with the 0.75Z fault isolation resistor provides the correct characteristic impedance for terminating the stub:*

$$Z_{stub} = \left( \frac{1}{1.41} \right)^2 (.75 Z_0 + .75 Z_0 + .5 Z_0)$$

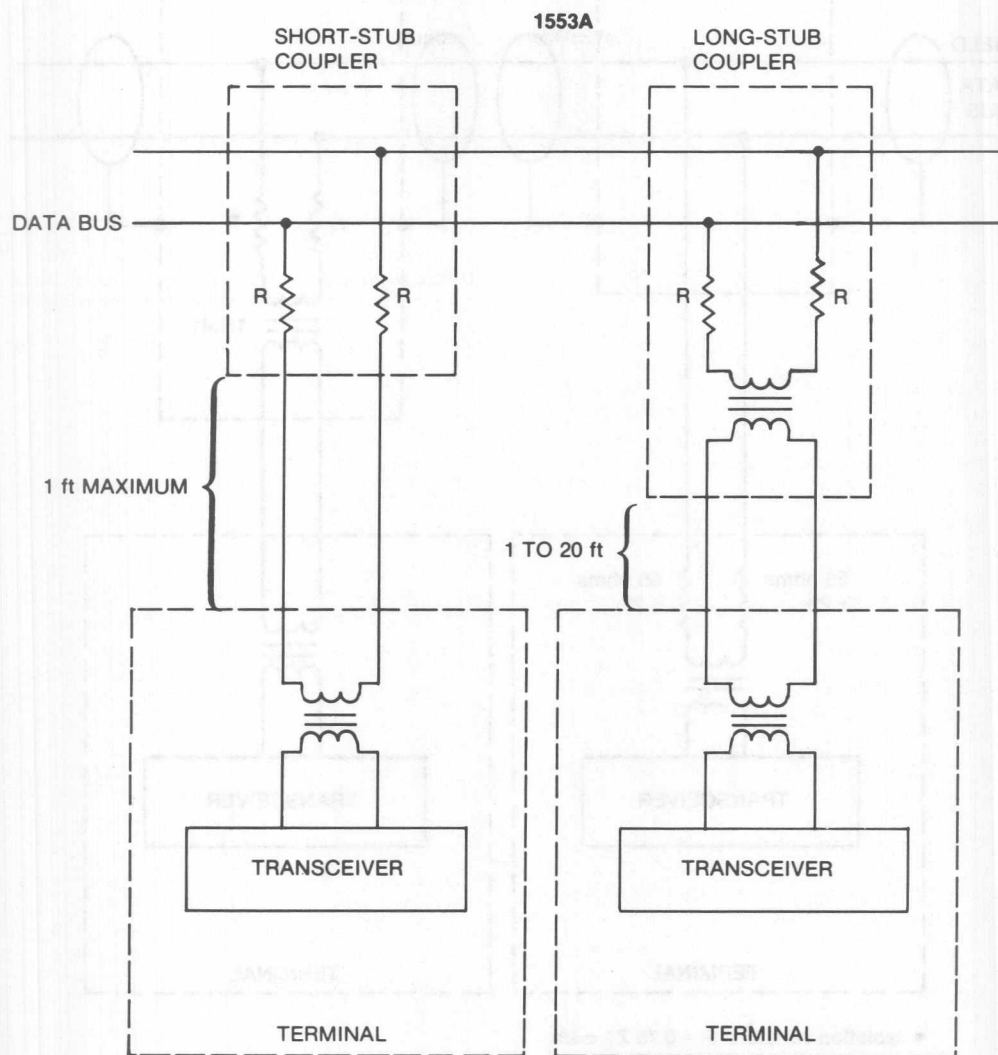
*The stub capacitance is also effectively decreased by the square of the turns ratio to lessen the loading problem. The 1:1.41 ratio of 1553B is a compromise between stub matching and decreased stub loading.*

*The connector type specified is important for severe environment military aircraft applications. MIL-STD-1553A specified the use of two-pin polarized connectors such as TEI BJ37 (reference to "TEL-14949-E137" is in error). The two-pin polarized connector employs an interface configuration with one male and one female contact. The female contact is embedded in one side of a step dielectric and the male contact is exposed. There are several inherent shortcomings to this design. MIL-STD-1553B does not specify connector types.*

*The coupling network provides bus connections for the transformer-coupled (external coupler) and direct-coupled cases defined in 1553B. Isolation resistors of 55 ohms value are included for the direct-coupled connection, and the proper transformer turns ratio is provided when the appropriate bus connection is selected. The turns ratio is different for the transformer-coupled and direct-coupled connections to compensate for the 1.41 to 1 reduction of signal level in the external coupler. This feature allows a threshold setting that is the same for both bus connections.*

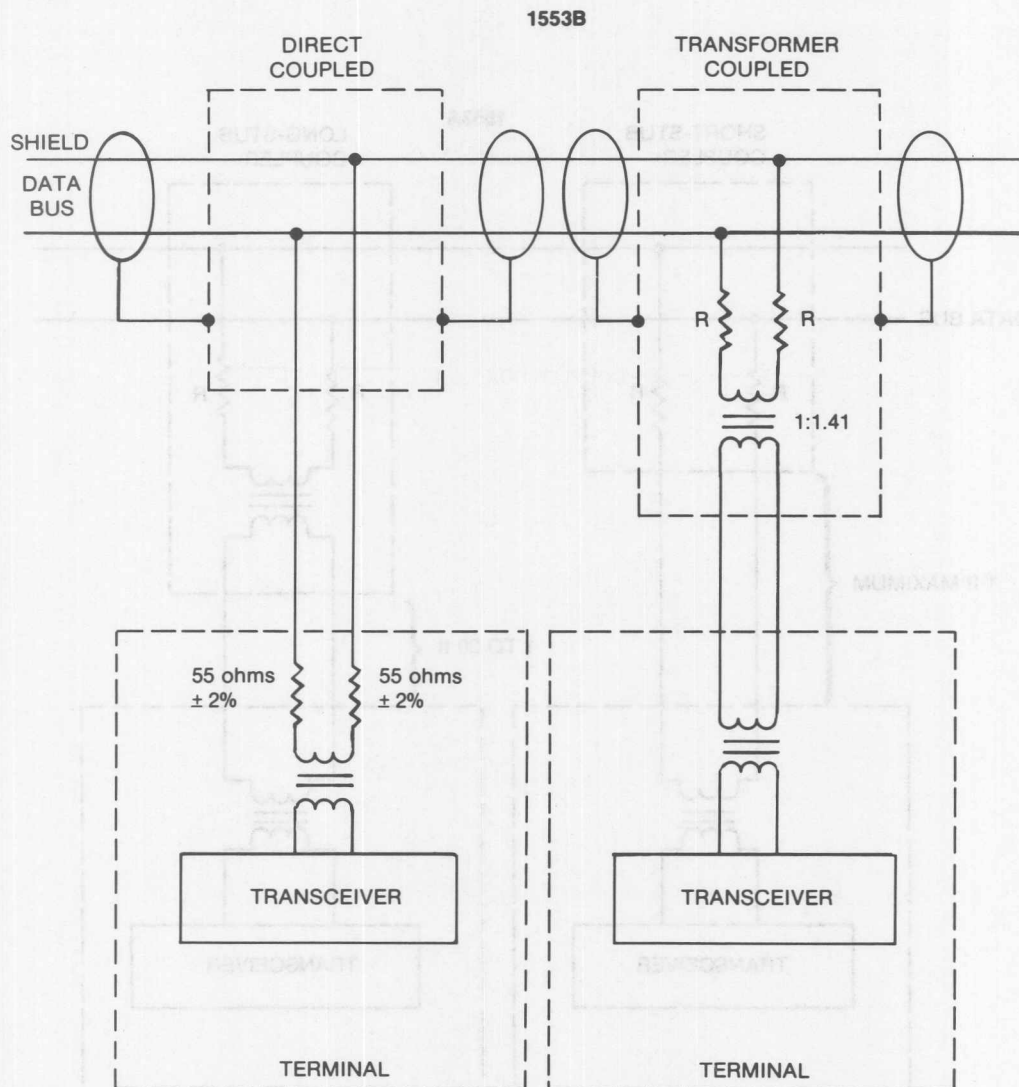
## 4.5.2 Terminal Characteristics

*An additional concern is the specification for the bus and terminal interface. This area of 1553A was significantly reworked to provide a more*



- Isolation resistors:  $R = 0.75 Z_0 \pm 5\%$
- Isolation transformer: (not specified)
- \*Nominal characteristic impedance of bus cable:  $Z_0 = 70 \pm 10\%$  at 1 MHz

Figure II-13. Coupler Characteristics



- Isolation resistors:  $R = 0.75 Z_0^* \pm 2\%$
  - Isolation transformer: turns ratio  $1:1.41 \pm 3\%$ 
    - (1—terminal winding)
    - (1.41—bus winding)
- $Z_{OC} > 3K$  at 75 kHz to 1 MHz  
1V rms sine wave
- Droop:  $< 20\%$   
 Overshoot/ringing:  $< \pm 1V$   
 CMR:  $> 45$  dB at 1 MHz
- } at 27V P-P 250 kHz square wave
- \*Nominal characteristic impedance of bus cable:  $Z_0 = 70$  to  $85$  at 1 MHz

Figure II-13. Coupler Characteristics (Continued)



complete definition of the terminal interface characteristics that are independent of network configuration. Figures II-14 and II-15 show the interface diagrams and the points where the signal measurement are defined in 1553A and 1553B. Table II-5 is a summary listing of the

terminal and data bus interface requirements specified in the two versions of the standard. The following discussion will relate some of the rationale for this approach to development of the updated requirements in 1553B.

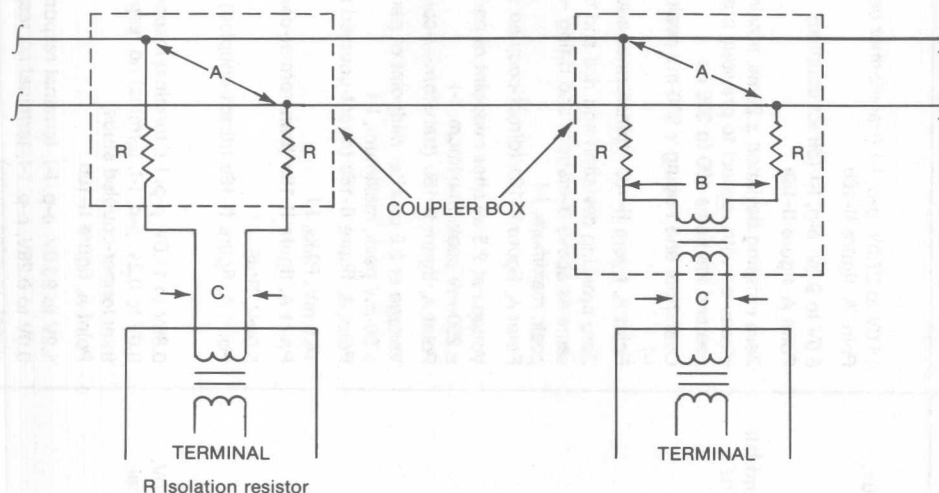


Figure II-14. MIL-STD-1553A Data Bus Interface

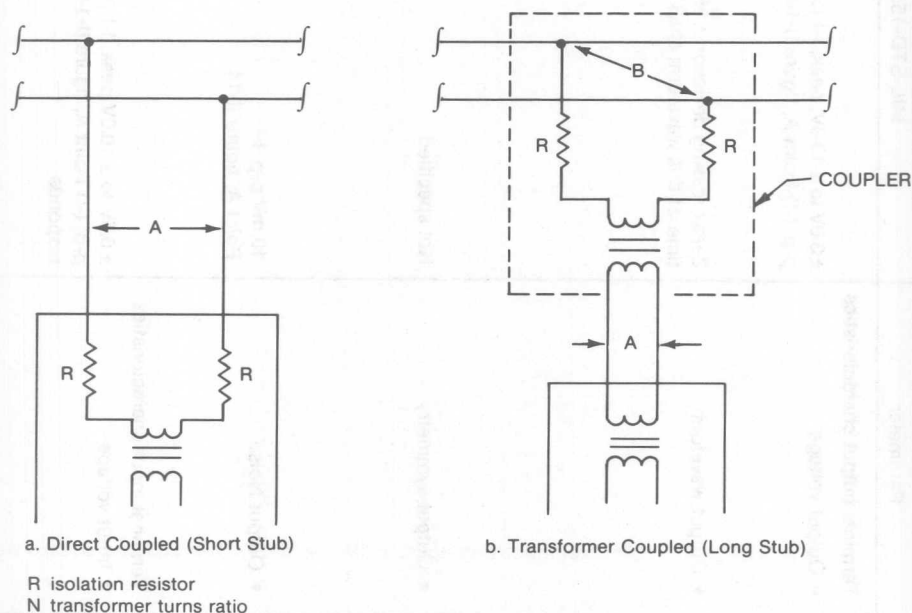


Figure II-15. MIL-STD-1553B Data Bus Interface

Table II-5. Summary of Terminal and Data Bus Interface Requirements

Parameter	MIL-STD-1553A	MIL-STD-1553B
Terminal output characteristics		
• Output voltage	$\pm 3.0\text{V}$ to $\pm 10.0\text{V}$ , peak, I-I (6.0V to 20.0V, p-p, I-I) Point A, figure II-14.	18.0V to 27.0V, p-p, I-I (transformer coupled) Point A, figure II-16b 6.0V to 9.0V, p-p, I-I (direct coupled) Point A, figure II-16a
• Output waveform	Zero crossing deviation $\pm 25$ ns; rise and fall time of this waveform shall be $\geq 100$ ns	Zero crossing deviation $\pm 25$ ns, maximum, measured with respect to previous crossing; rise and fall times 100 to 300 ns Overshoot and ringing $\pm 900$ -mV peak, maximum, I-I Point A, figure II-16b (transformer-coupled stub) Zero crossing deviation and rise and fall times same as above overshoot and rining — $\pm 300$ -mV peak, maximum, I-I Point A, figure II-16a (direct-coupled stub) Voltage at 2.5 $\mu\text{s}$ after midpoint of parity bit; $\pm 250$ -mV peak, maximum, I-I Point A, figure II-16b (transformer-coupled stub) Voltage at 2.5 $\mu\text{s}$ after midpoint of parity bit; $\pm 90$ -mV peak, maximum, I-I Point A, figure II-16a (direct-coupled stub)
• Output symmetry	Not specified	14.0 mV, RMS, I-I Point A, figure II-16b (transformer-coupled) 5.0mV, RMS, I-I Point A, figure II-16a (direct-coupled)
• Output Noise	10 mV p-p, I-I Point A, figure II-14	0.86V to 14.0V, p-p, I-I, terminal response required; 0.0V to 0.2V, p-p, I-I, terminal no response (with transformer-coupled stubs) Point A, figure II-15b 1.2V to 20.0V, p-p, I-I, terminal response required; 0.0V to 0.28V, p-p, I-I, terminal no response (with direct-coupled stubs) Point A, figure II-15a
Terminal input characteristics		
• Input voltage	$\pm 0.5\text{V}$ to $\pm 10.0\text{V}$ peak, I-I (1.0V to 20.0V, p-p, I-I) Point A, figure II-14 — terminal responds	

Table II-5. Summary of Terminal and Data Bus Interface Requirements (Concluded)

Parameter	MIL-STD-1553A	MIL-STD-1553B
<ul style="list-style-type: none"> <li>• Input impedance</li> </ul>	2,000 ohms, minimum, from 100 kHz to 1.0 MHz Point C, figure II-14	1,000 ohms, minimum, from 75 kHz to 1.0 MHz Point A, figure II-15b (transformer-coupled stub) 2,000 ohms, minimum, from 75 kHz to 1.0 MHz Point A, figure II-15a (direct-coupled)
<ul style="list-style-type: none"> <li>• Noise rejection</li> </ul>	BER — 1 in $10^{12}$ ; maximum, incomplete message rate 1 in $10^6$ ; test condition — bus controller connected to RT over 100-ft data bus using 20-ft stubs	Maximum word error rate of 1 in $10^7$ , AWG noise, 1.0 kHz to 4.0 MHz, 140 mV, RMS level; signal level — 2.1V, p-p, I-I Point A, figure II-15b (transformer-coupled stub) Maximum word error rate of 1 in $10^7$ , AWG noise, 1.0 kHz to 4.0 MHz, 200 mV, RMS level; signal level is 3.0V, p-p, I-I Point A, figure II-15a (direct-coupled stub)
<ul style="list-style-type: none"> <li>• Common mode rejection</li> </ul>	$\pm 10.0V$ peak, line-to-ground, dc to 2 MHz, shall not degrade performance Point A, figure II-14	$\pm 10.0V$ peak, line-to-ground, dc to 2.0 MHz, shall not degrade performance of the receiver Point A, figure II-15b (transformer-coupled stub) Same specification for direct-coupled stub Point A, figure II-15a

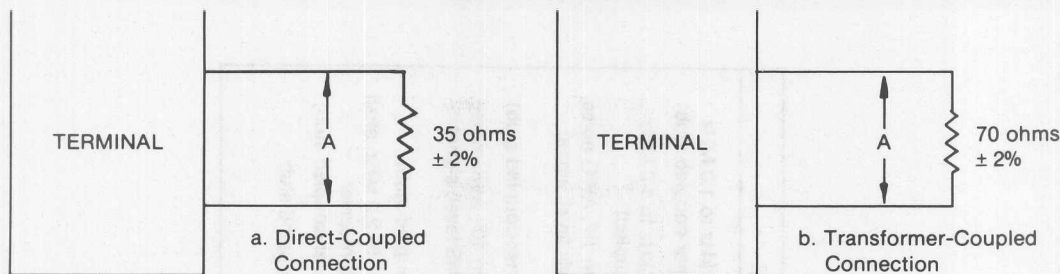


Figure II-16. Direct-Coupled and Transformer-Coupled Terminal Output Test Configuration

#### 4.5.2.1 Terminals with transformer coupled stubs

**4.5.2.1.1 Terminal output characteristics.** The following characteristics shall be measured with  $R_L$  as shown on figure 12, equal to 70.0 Ohms  $\pm 2.0$  percent.

**4.5.2.1.1.1 Output levels.** The terminal output voltage levels shall be measured using the test configuration shown on figure 12. The terminal output voltage shall be within the range of 18.0 to 27.0 V, peak-to-peak, line-to-line, when measured at point A on figure 12.

*The upper end of the bus voltage range (20V p-p) allowed by 1553A was considered to be excessive and if implemented would result in excessive power dissipation and most of the systems and hardware designed to 1553A use signal levels at or near the lower end (6.0V p-p) of the specified range. It should be noted that the measurement point in 1553A is at the main bus, point A on figure 7-14. This does not provide a specified level at the terminal connection point (c) and is especially troublesome to the terminal hardware designer since the characteristics of the coupler transformer are not specified. The approach taken for 1553B is to specify the terminal output for the two conditions, transformer-coupled and direct-coupled. This may require that each terminal have two sets of input-output pins for each bus cable connection. Therefore, the 18V to 27V p-p transmitter output applied to the stub and coupler results in a nominal 6.0V to 9.0V p-p signal level at the stub and bus connection (point B). This range is equivalent to that specified for the direct-coupled case shown in figure II-15. Test configurations are provided for both direct-coupled and transformer-coupled in figure II-16.*

**4.5.2.1.1.2 Output waveform.** The waveform, when measured at point A on figure 12 shall have zero crossing deviations which are equal to, or less than, 25.0 ns from the ideal crossing point,

measured with respect to the previous zero crossing (i.e.,  $.5 \pm .025$  us,  $1.0 \pm .025$  us,  $1.5 \pm .025$  us, and  $2.0 \pm .025$  us). The rise and fall time of this waveform shall be from 100.0 to 300.0 ns when measured from levels of 10 to 90 percent of full waveform peak-to-peak, line-to-line, voltage as shown on figure 13. Any distortion of the waveform including overshoot and ringing shall not exceed  $\pm 900.0$  millivolts (mV) peak, line-to-line, as measured at point A, figure 12.

*The transmitted waveform specified in 1553A is limited in the definition of signals that appear on the data bus. The zero crossing deviations allowed are not well defined for all possible patterns, and the rise and fall times specification is open ended. The waveform characteristics defined in 1553B provides control of the zero crossing deviations for all possible conditions and establishes a limit on distortion.*

**4.5.2.1.1.3 Output noise.** Any noise transmitted when the terminal is receiving or has power removed, shall not exceed a value of 14.0 mV, RMS, line-to-line, as measured at point A, figure 12.

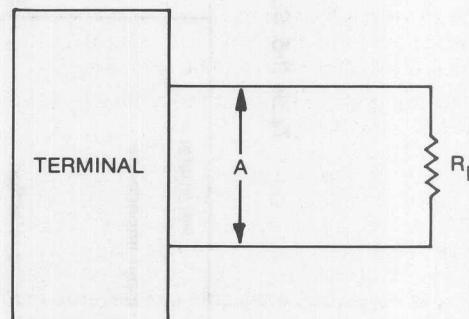


Figure 12 of 1553B. Terminal I/O Characteristics for Transformer-Coupled and Direct-Coupled Stubs



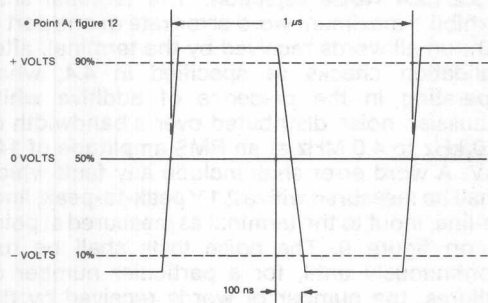


Figure 13 of 1553B. Output Waveform

*MIL-STD-1553A specified value of 10 mV p-p noise (4.2.5.3.3) is considered unrealistically low for practical hardware design. Also, noise is normally specified as an rms value since peak noise is difficult to measure. The output rms noise for the transformer-coupled and direct-coupled cases are specified in 1553B (4.5.2.1.1.3 and 4.5.2.2.1.3) and are consistent with the required system performance and practical terminal hardware design. The requirement for low output noise of 14 mVrms and 5 mVrms when not transmitting also places significant constraints on the length and routing of input-output wiring because of the induced power supply and logic noise generated in the terminal.*

**4.5.2.1.1.4 Output symmetry.** From the time beginning 2.5  $\mu$ s after the mid-bit crossing of the parity bit of the last word transmitted by a terminal, the maximum voltage at point A of figure 12 shall be no greater than  $\pm 250.0$  mV peak, line-to-line. This shall be tested with the terminal transmitting the maximum number of words it is designed to transmit, up to 33. This test shall be run six times with each word in a contiguous block of words having the same bit pattern. The six word contents that shall be used are 8000<sub>16</sub>, 7FFF<sub>16</sub>, 0000<sub>16</sub>, FFFF<sub>16</sub>, 5555<sub>16</sub>, and AAAA<sub>16</sub>.

The output of the terminal shall be as specified in 4.5.2.1.1.1 and 4.5.2.1.1.2.

*Symmetry of the transmitted waveform in time and amplitude was not adequately specified in 1553A. An ideal waveform is perfectly balanced so that the signal energy on both sides of zero (off) level is identical. If the positive or negative energy is not equal, problems can develop in the coupling transformers and the transmission line can acquire a charge that appears as a tail with overshoot and ringing when transmission is terminated. These considerations require that the symmetry of the transmitted waveform be*

*controlled within practical limits. This is accomplished in 1553B by specifying the signal level from a time beginning 2.5  $\mu$ s after the midbit zero crossing of the parity bit of the last word in a message transmitted by the terminal under test. The test messages contain the maximum number of words and defined bit patterns.*

**4.5.2.1.2 Terminal input characteristics.** The following characteristics shall be measured independently.

**4.5.2.1.2.1 Input waveform compatibility.** The terminal shall be capable of receiving and operating with the incoming signals specified herein, and shall accept waveform varying from a square wave to a sine wave with respect to the previous zero crossing of  $\pm 150$  ns, (i.e.,  $2.0 \pm .15$   $\mu$ s,  $1.5 \pm .15$   $\mu$ s,  $1.0 \pm .15$   $\mu$ s,  $.5 \pm .15$   $\mu$ s). The terminal shall respond to an input signal whose peak-to-peak amplitude, line-to-line, is within the range of .86 to 14.0 V. The terminal shall not respond to an input signal whose peak-to-peak amplitude, line-to-line, is within the range of 0.0 to .20V. The voltages are measured at point A on figure 9.

**4.5.2.1.2.2 Common mode rejections.** Any signals from direct current (DC) to 2.0 MHz, with amplitudes equal to or less than  $\pm 10.0$  V peak, line-to-ground, measured at point A on figure 9, shall not degrade the performance of the receiver.

*The input voltage specifications in 1553B have been revised to reflect the output voltage ranges for the transformer-coupled and direct-coupled connections to the terminal. The terminal-required response and no-response signal levels are specified so that the optimum threshold levels may be selected. It should be noted that the threshold setting has a significant effect on the noise rejection and error rate performance of the receiver. The maximum value for no-response signal level is 200mV p-p, and 280 mV p-p allows optimum threshold settings of  $\pm 125$  and  $\pm 175$  mV, respectively, for minimum bit error rate (BER) performance when subjected to the specified noise rejection test conditions.*

**4.5.2.1.2.3 Input impedance.** The magnitude of the terminal input impedance, when the RT is not transmitting, or has power removed, shall be a minimum of 1000.0 Ohms within the frequency range of 75.0 kHz to 1.0 MHz. This impedance is that measured line-to-line at point A on figure 9.

*As indicated in the data bus network requirement, input impedance is required to be maintained at a reasonable level to reduce the*

signal distortion effects when terminals are connected to the bus. Terminal input impedance is determined primarily by the following:

- a. Transformer impedance maintains inductance required to support low-frequency component of signal while controlling interwinding capacitance for high frequencies.
- b. Terminal wiring capacitance controls stray capacitance of wiring from terminal connector to receiver.
- c. Secondary impedance transformation, for the transformer-coupled case, a transformer with a turns ratio of 1:1.41 is implied. The impedance at the secondary is reflected to the terminal input reduced by a factor of 2.

The transformer is a very important element in determining the transceiver characteristics such as input impedance, signal waveform integrity, and common mode rejection required by 1553B. The considerations for transformer and associated input-output circuit design are to --

- a. provide the specified input impedance at high frequencies (terminal input impedance 1,000 ohms and 2,000 ohms at 1 MHz)
- b. Design for low interwinding capacitance to achieve the common mode rejection (45 db CMR at  $\pm 10V$  peak, dc to 2.0 MHz)

These considerations are directly applicable to the design of the transceiver transformer. In addition to the transformer characteristics, other considerations for maintaining the terminal minimum input impedance specified in 1553B are as follows:

- a. Minimize stray capacitance of wiring from the external connector and on the circuit card to the buffer amplifier (every 100 pF results in approximately 1,600 ohms of shunt impedance).
- b. Maintain high impedance at the receiver limiter and filter circuit inputs and transmitter driver outputs in the "off" state. These impedances must be maintained with the terminal (transceiver) power off.

The factor of 2 difference in the impedance specified for the transformer-coupled and direct-coupled cases is based primarily on the effect of c. The frequency range was changed to reduce the lower frequency limit from 100 kHz (1553A) to 75 kHz (1553B). This provides additional assurance that adequate transformer volt-time product (inductance) is available to support the lower frequencies of the signal without approaching saturation.

**4.5.2.1.2.4 Noise rejection.** The terminal shall exhibit a maximum word error rate of one part in  $10^7$ , on all words received by the terminal, after validation checks as specified in 4.4, when operating in the presence of additive white Gaussian noise distributed over a bandwidth of 1.0 kHz to 4.0 MHz at an RMS amplitude of 140 mV. A word error shall include any fault which shall be measured with a 2.1 V peak-to-peak, line-to-line, input to the terminal as measured at point A on figure 9. The noise tests shall be run continuously until, for a particular number of failures, the number of words received by the terminal, including both command and data words, exceeds the required number for acceptance of the terminal, or is less than the required number for rejection of the terminal, as specified in table II. All data words used in the tests shall contain random bit patterns. These bit patterns shall be unique for each data word in a message, and shall change randomly from message to message.

The noise rejection specification and test conditions defined in 1553A requires extensive system-type evaluation testing of the terminal employing a bus controller and data bus radiated with certain of the EMI fields specified in MIL-STD-461 and 462. Extensive test time is required to verify a BER of  $10^{-12}$  and the test must be performed in a screen room.

The test conditions of signal and noise specified in 1553B were selected to produce a corresponding value of word error rate (WER) which is sufficiently high ( $10^{-7}$ ) to permit performance verification of a terminal receiver within a reasonable test period. The noise rejection is a figure-of-merit test and can be performed in a normal laboratory using actual transmitters (Manchester waveform output) with a typical test setup as shown in figure II-17. The verification of detector performance should consider the measurement of both detected and undetected errors. To measure undetected errors that do not correlate with the transmitted signal and are not detected by the terminal under test, it is necessary to compare the transmitted and received data. Therefore, a reference of transmitted data is provided to the comparator for comparison with the detected data from the terminal under test.

Externally generated noise on board an aircraft can take many forms with a wide variety of power and frequencies. It is recognized that impulse noise having either random or periodic impulse duration, frequency of occurrences, and burst interval are more typical of noise sources that have major impact on aircraft digital data

Table II-6. Criteria for Acceptance or Rejection of a Terminal for the Noise Rejection Test

Total words received by terminal  
(in multiples of  $10^7$ )

No. of errors	Reject (equal or less)	Accept (equal or more)
0	NA	4.40
1	NA	5.21
2	NA	6.02
3	NA	6.83
4	NA	7.64
5	NA	8.45
6	0.45	9.27
7	1.26	10.08
8	2.07	10.89
9	2.88	11.70
10	3.69	12.51
11	4.50	13.32
12	5.31	14.13
13	6.12	14.94
14	6.93	15.75
15	7.74	16.56
16	8.55	17.37
17	9.37	18.19
18	10.18	19.00
19	10.99	19.81
20	11.80	20.62
21	12.61	21.43
22	13.42	22.24
23	14.23	23.05
24	15.04	23.86
25	15.85	24.67
26	16.66	25.48
27	17.47	26.29
28	18.29	27.11
29	19.10	27.92
30	19.90	28.73
31	20.72	29.54
32	21.53	30.35
33	22.34	31.16
34	23.15	31.97
35	23.96	32.78
36	24.77	33.00
37	25.58	33.00
38	26.39	33.00
39	27.21	33.00
40	28.02	33.00
41	33.00	NA

Note: NA — not applicable.

systems. Relay switching is generally regarded as the most severe source of impulse noise on a typical aircraft. This type of noise defies accepted forms of analysis, such as that performed utilizing additive white gaussian (AWG) noise model. Because of the difficulty of error performance analysis using the impulsive noise model, a worst-case gaussian model has been formulated. This model offers an analysis and test tool for evaluation of terminal receiver performance considering the effects of impulsive noise. This approach is reflected in the noise rejection test conditions and word error rate versus signal-to-noise ratio (SNR) performance requirements of 1553B, paragraphs 4.5.2.1.2.4 and 4.5.2.2.2.4.

#### 4.5.2.2 Terminals with direct coupled stubs

**4.5.2.2.1 Terminal output characteristics.** The following characteristics shall be measured with  $R_L$ , as shown on figure 12, equal to 35.0 Ohms  $\pm$  2.0 percent.

**4.5.2.2.1.1 Output levels.** The terminal output voltage levels shall be measured using the test configuration shown on figure 12. The terminal output voltage shall be within the range of 6.0 to 9.0 V, peak-to-peak, line-to-line, when measured at point A on figure 12.

**4.5.2.2.1.2 Output waveform.** The waveform, when measured at point A on figure 12, shall have zero crossing deviations which are equal to, or less than, 25.0 ns from the ideal crossing point, measured with respect to the previous zero crossing (i.e.,  $.5 \pm .025$  us,  $1.0 \pm .025$  us,  $1.5 \pm .025$  us and  $2.0 \pm .025$  us). The rise and fall time of this waveform shall be from 100.0 to 300.0 ns when measured from levels of 10 to 90 percent of full waveform peak-to-peak, line-to-line, voltage as shown on figure 13. Any distortion of the waveform including overshoot and ringing shall not exceed  $\pm 300.0$  mV peak, line-to-line, as measured at point A on figure 12.

**4.5.2.2.1.3 Output noise.** Any noise transmitted when the terminal is receiving or has power removed, shall not exceed a value of 5.0 mV, RMS, line-to-line, as measured at point A on figure 12.

**4.5.2.2.1.4 Output symmetry.** From the time beginning 2.5 us after the mid-bit crossing of the parity bit of the last word transmitted by a terminal, the maximum voltage at point A on figure 12, shall be no greater than  $\pm 90.0$  mV peak, line-to-line. This shall be tested with the terminal transmitting the maximum number of words it is designed to transmit, up to 33. This test shall be run six times with each word in a contiguous block of words having the same bit pattern. The

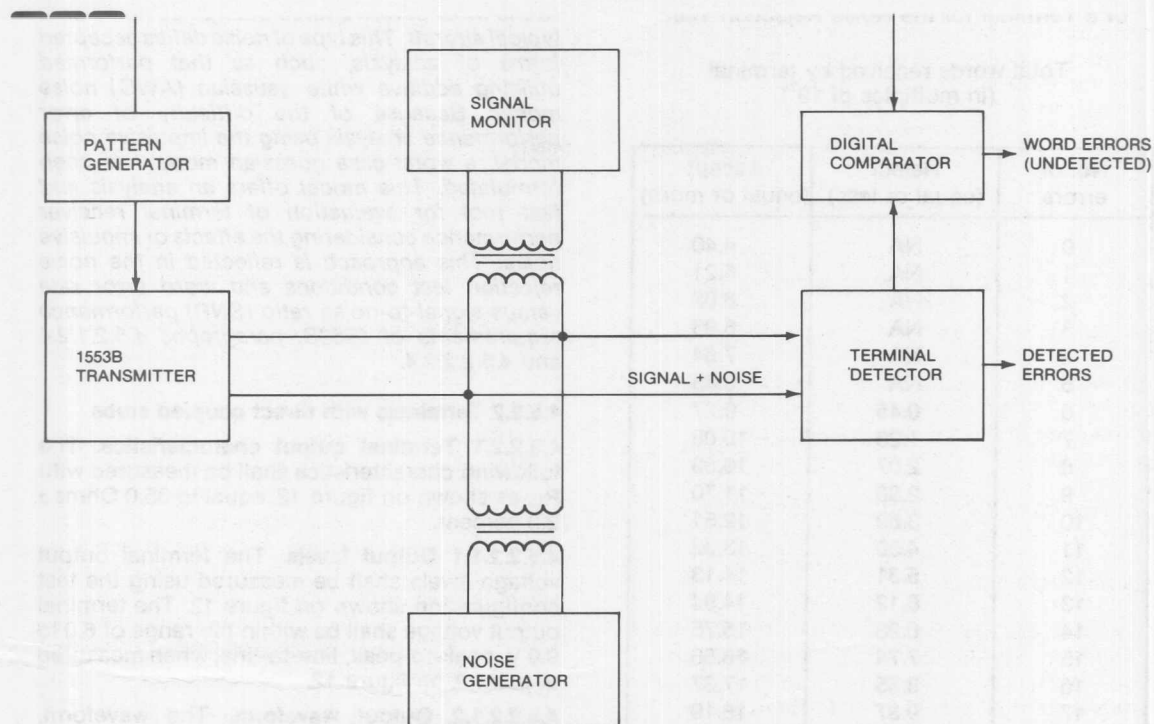


Figure II-17. Typical Noise Rejection Test Setup

six word contents that shall be used are 8000<sub>16</sub>, 7FFF<sub>16</sub>, 0000<sub>16</sub>, FFFF<sub>16</sub>, 5555<sub>16</sub>, and AAAA<sub>16</sub>. The output of the terminal shall be as specified in 4.5.2.2.1.1 and 4.5.2.2.1.2.

**4.5.2.2.2 Terminal input characteristics.** The following characteristics shall be measured independently.

**4.5.2.2.2.1 Input waveform compatibility.** The terminal shall be capable of receiving and operating with the incoming signals specified herein, and shall accept waveform varying from a square wave to a sine wave with a maximum zero crossing deviation from the ideal with respect to the previous zero crossing of plus or minus 150 ns, (i.e.,  $2.0 \pm .15 \mu\text{s}$   $1.5 \pm .15 \mu\text{s}$ ,  $1.0 \pm .15 \mu\text{s}$   $.5 \pm .15 \mu\text{s}$ ). The terminal shall respond to an input signal whose peak-to-peak amplitude, line-to-line, is within the range of 1.2 to 20.0V. The terminal shall not respond to an input signal whose peak-to-peak amplitude, line-to-line, is within the range of 0.0 to .28 V. The voltages are measured at point A on figure 10.

**4.5.2.2.2.2 Common mode rejections.** Any signals from DC to 2.0 MHz, with amplitudes equal to or

less than  $\pm 10.0$  volts peak, line-to-ground, measured at point A on figure 10, shall not degrade the performance of the receiver.

**4.5.2.2.2.3 Input impedance.** The magnitude of the terminal input impedance, when the RT is not transmitting, or has power removed, shall be a minimum of 2000.0 ohms within the frequency range of 75.0 kHz to 1.0 MHz. This impedance is that measured line-to-line at point A on figure 10.

**4.5.2.2.2.4 Noise rejection.** The terminal shall exhibit a maximum word error rate of one part in  $10^7$ , on all words received by the terminal, after validation checks as specified in 4.4, when operating in the presence of additive white Gaussian noise distributed over a bandwidth of 1.0 kHz to 4.0 MHz at an RMS amplitude of 200 mV. A word error shall include any fault which causes the message error bit to be set in the terminal's status word, or one which causes a terminal to not respond to a valid command. The word error rate shall be measured with a 3.0V peak-to-peak, line-to-line, input to the terminal as measured at point A on figure 10. The noise tests shall be run continuously until, for a



particular number of failures, the number of words received by the terminal, including both command and data words, exceeds the required number for acceptance of the terminal, or is less than the required number for rejection of the terminal, as specified in table II. All data words used in the tests shall contain random bit patterns. These bit patterns shall be unique for each data word in a message, and shall change randomly from message to message.

*A discussion of "terminals with direct coupled stubs" are covered in the preceding section, which discusses "terminals with transformer coupled stubs" (4.5.2.1).*

**4.6 Redundant data bus requirements.** If redundant data buses are used, the requirements as specified in the following shall apply to those data buses.

*This section of the standard was added to 1553B. The purpose was to clarify requirements relating to the electrical characteristics and operation of redundant data buses.*

**4.6.1 Electrical isolation.** All terminals shall have a minimum of 45 dB isolation between data buses. Isolation here means the ratio in dB between the output voltage on the active data bus and the output voltage on the inactive data bus. This shall be measured using the test configuration specified in 4.5.2.1.1 or 4.5.2.2.1 for each data bus. Each data bus shall be alternately activated with all measurements being taken at point A on figure 12 for each data bus.

*Although the data bus is commonly used in a dual-redundant manner, 1553A did not specify electrical isolation characteristics between redundant buses. This paragraph was added in 1553B to provide a ratio of the maximum transmitted signal on one bus to the minimum*

*received threshold on the redundant bus. Test conditions that are specified in the referenced paragraphs correspond to terminals with transformer-coupled stubs and with direct-coupled stubs.*

**4.6.2 Single event failures.** All data buses shall be routed to minimize the possibility that a single event failure to a data bus shall cause the loss of more than that particular data bus.

*This is an obvious requirement unique to military aircraft. This paragraph was added in 1553B.*

**4.6.3 Dual standby redundant data bus.** If a dual redundant data bus is used, then it shall be a dual standby redundant data bus as specified in the following paragraphs.

**4.6.3.1 Data bus activity.** Only one data bus can be active at any given time except as specified in 4.6.3.2.

**4.6.3.2 Reset data bus transmitter.** If while operating on a command, a terminal receives another valid command, from either data bus, it shall reset and respond to the new command on the data bus on which the new command is received. The terminal shall respond to the new command as specified in 4.3.3.8.

*These new paragraphs in 1553B reflect the common practice in current aircraft of using the dual bus as one active, one standby, and it was the intent to restrict the operation of a dual data bus connected to terminal to a "one-at-a-time" operation. However, provision had to be made for a bus controller to override one bus to respond on the redundant bus. The requirement for this is in paragraph 4.6.3.2 above, and the reference to paragraph 4.3.3.8 is the response time requirement of a remote terminal to a valid command word.*

## APPENDIX

**10. General.** The following paragraphs in this appendix are presented in order to discuss certain aspects of the standard in a general sense. They are intended to provide a user of the standard more insight into the aspects discussed.

**10.1 Redundancy.** It is intended that this standard be used to support rather than to supplant the system design process. However, it has been found, through application experience in various aircraft, that the use of a dual standby redundancy technique is very desirable for use in integrating mission avionics. For this reason, this redundancy scheme is defined in 4.6 of this standard. None the less, the system designer should utilize this standard as the needs of a particular application dictate. The use of redundancy, the degree to which it is implemented, and the form which it takes must be determined on an individual application basis. Figures 10.1 and 10.2 illustrate some possible approaches to dual redundancy. These illustrations are not intended to be inclusive, but rather representative. It should be noted that analogous approaches exist for the triple and quad redundant cases.

**10.2 Bus controller.** The bus controller is a key part of the data bus system. The functions of the bus controller, in addition to the issuance of commands, must include the constant monitoring of the data bus and the traffic on the bus. It is envisioned that most of the routine minute details of bus monitoring (e.g., parity checking, terminal non-response time-out, etc.) will be embodied in hardware, while the algorithms for bus control and decision making will reside in software. It is also envisioned that, in general, the bus controller will be a general purpose airborne computer with a special input/output (I/O) to interface with the data bus. It is of extreme importance in bus controller

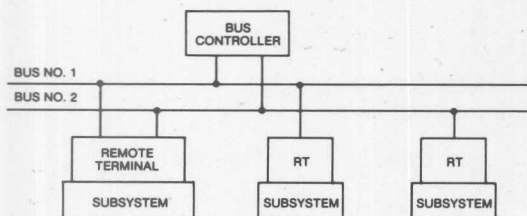
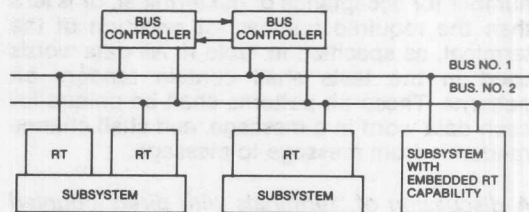


Figure 10.1 Illustration of possible redundancy.



NOTE: RT - Remote Terminal

Figure 10.2 Illustration of possible redundancy.

design that the bus controller be readily able to accommodate terminals of differing protocol's and status word bits used. Equipment designed to MIL-STD-1553A will be in use for a considerable period of time; thus, bus controllers must be capable of adjusting to their differing needs. It is also important to remember that the bus controller will be the focal point for modification and growth within the multiplex system, and thus the software must be written in such a manner as to permit modification with relative ease.

**10.3 Multiplex selection criteria.** The selection of candidate signals for multiplexing is a function of the particular application involved, and criteria will in general vary from system to system. Obviously, those signals which have bandwidths of 400 Hz or less are prime candidates for inclusion on the bus. It is also obvious that video, audio, and high speed parallel digital signals should be excluded. The area of questionable application is usually between 400 Hz and 3 kHz bandwidth. The transfer of these signals on the data bus will depend heavily upon the loading of the bus in a particular application. The decision must be based on projected future bus needs as well as the current loading. Another class of signals which in general are not suitable for multiplexing are those which can be typified by a low rate (over a mission) but possessing high priority or urgency. Examples of such signals might be a nuclear event detector output or a missile launch alarm from a warning receiver. Such signals are usually better left hardwired, but they may be accommodated by the multiplex system if a direct connection to the bus controller's interrupt hardware is used to trigger a software action in response to the signal.

**10.4 High reliability requirements.** The use of simple parity for error detection within the

multiplex bus system was dictated by a compromise between the need for reliable data transmission, system overhead, and remote terminal simplicity. Theoretical and empirical evidence indicated that an undetected bit error rate of  $10^{-12}$  can be expected from a practical multiplex system built to this standard. If a particular signal requires a bit error rate which is better than that provided by the parity checking, then it is incumbent upon the system designer to provide the reliability within the constraints of the standard or to not include this signal within the multiplex bus system. A possible approach in this case would be to have the signal source and sink provide appropriate error detection and correction encoding/decoding and employ extra data words to transfer the information. Another approach would be to partition the message, transmit a portion at a time, and then verify (by interrogation) the proper transfer of each segment.

**10.5 Stubbing.** Stubbing is the method wherein a separate line is connected between the primary data bus line and a terminal. The direct connection of stub line causes a mismatch which appears on the waveforms. This mismatch can be reduced by filtering at the receiver and by using bi-phase modulation. Stubs are often employed not only as a convenience in bus layout but as a means of coupling a unit to the line in such a manner that a fault on the stub or terminal will not greatly affect the transmission line operation. In this case, a network is employed in the stub line to provide isolation from the fault. These networks are also used for stubs that are of such length that

the mismatch and reflection degrades bus operation. The preferred method of stubbing is to use transformer coupled stubs, as defined in 4.5.1.5.1. This method provides the benefits of DC isolation, increased common mode protection, a doubling of effective stub impedance, and fault isolation for the entire stub and terminal. Direct coupled stubs, as defined in 4.5.1.5.2 of this standard, should be avoided if at all possible. Direct coupled stubs provide no DC isolation or common mode rejection for the terminal external to its subsystem. Further, any shorting fault between the subsystems internal isolation resistors (usually on a circuit board) and the main bus junction will cause failure of that entire bus. It can be expected that when the direct coupled stub length exceeds 1.6 feet, that it will begin to distort the main bus waveforms. Note that this length includes the cable runs internal to a given subsystem.

**10.6 Use of broadcast option.** The use of a broadcast message as defined in 4.3.3.6.7 of this standard represents a significant departure from the basic philosophy of this standard in that it is a message format which does not provide positive closed-loop control of bus traffic. The system designer is strongly encouraged to solve any design problems through the use of the three basic message formats without resorting to use of the broadcast. If system designers do choose to use the broadcast command, they should carefully consider the potential effects of a missed broadcast message, and the subsequent implications for fault or error recovery design in the remote terminals and bus controllers.

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THE FOLLOWING TABLE SETS OUT THE DATA FOR THE MONTHS OF SEPTEMBER AND OCTOBER 1978	
DATE	NO. OF CASES
1 September 1978	12
15 September 1978	11
31 September 1978	10

THE FOLLOWING TABLE SETS OUT THE DATA FOR THE MONTHS OF SEPTEMBER AND OCTOBER 1978

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[REDACTED]

MIL-STD-1553B  
NOTICE 1(USAF)  
12 February 1980

MILITARY STANDARD

AIRCRAFT INTERNAL TIME DIVISION  
COMMAND/RESPONSE MULTIPLEX DATA BUS

TO ALL HOLDERS OF MIL-STD-1553B.

1. THE FOLLOWING PAGES OF MIL-STD-1553B HAVE BEEN REVISED AND SUPERSEDE THE PAGES LISTED:

<u>NEW PAGE</u>	<u>SUPERSEDED PAGE</u>	<u>DATE</u>
iii	iii	21 September 1978
viii	viii	21 September 1978
34	34	21 September 1978

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5. This notice is applicable to all U.S. Air Force internal avionics activities.

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Preparing activity  
Air Force - 11

Project MISC-FD32

MIL-STD-1553B  
12 February 1980

# FOREWARD

This standard contains requirements for aircraft internal time division command/response multiplex data bus techniques which will be utilized in systems integration of aircraft subsystems. Even with the use of this standard, subtle differences will exist between multiplex data buses used on different aircraft due to particular aircraft mission requirements and the designer options allowed in this standard. The system designer must recognize this fact, and design the multiplex bus controller hardware and software to accommodate such differences. These designer selected options must exist, so as to allow the necessary flexibility in the design of specific multiplex systems in order to provide for the control mechanism, architecture redundancy, degradation concept and traffic patterns peculiar to the specific aircraft mission requirements. \* Appendix Section 20 selects those options which shall be required and further restricts certain portions of the standard for use in Air Force aircraft internal avionics applications.

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MIL-STD-1553B  
12 February 1980

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10.6 Use of broadcast option. The use of a broadcast message as defined in 4.3.3.6.7 of this standard represents a significant departure from the basic philosophy of this standard in that it is a message format which does not provide positive closed-loop control of bus traffic. The system designer is strongly encouraged to solve any design problems through the use of the three basic message formats without resorting to use of the broadcast. If system designers do choose to use the broadcast command, they should carefully consider the potential effects of a missed broadcast message, and the subsequent implications for fault or error recovery design in the remote terminals and bus controllers.

\*20. General. This appendix is applicable to all U.S. Air Force aircraft internal avionics activities. The intent of the appendix is to select those options which shall be required and to further restrict certain portions of the standard for use in Air Force avionics. References in parenthesis are to the paragraphs in the standard that are affected.

\*20.1 Mode codes. (4.3.3.5.1.7) The mode codes for dynamic bus control, inhibit terminal flag bit, override inhibit terminal flag bit, selected transmitter shutdown and override selected transmitter shutdown shall not be transmitted on the data bus by bus controllers in Air Force avionics applications. However, these mode codes may be implemented in a remote terminal for Air Force avionics applications.

\*20.2 Broadcast command. (4.3.3.6.7) The broadcast command shall not be transmitted on the data bus by bus controllers in Air Force avionics applications. However, this message format may be implemented in remote terminals. If the broadcast message format is implemented in a remote terminal, then that terminal shall also implement the transmit status word mode code as specified in 4.3.3.5.1.7.3. Note that the remote terminal address of 11111 is still reserved for broadcast, and shall not be used for any other purpose in Air Force Avionics applications.

\*20.3 Mode code indicators.

\*20.3.1 Bus controllers. (4.4.2) In Air Force avionics applications, the bus controller shall be able to utilize both 00000 and 11111 in the subaddress/mode field as defined in 4.3.3.5.1.7. In addition, if a bus controller is required to utilize any mode code in its operation, then it shall be required to implement the capacity to utilize all mode codes.

\*20.3.2 Remote terminals. (4.4.3.1) All RT's which are designed for Air Force avionics applications, and which implement mode codes, shall respond properly to a mode code command, as defined in 4.3.3.5.1.7, with 00000 in the subaddress/mode field. In addition, such RT's may also respond to 11111 in the subaddress/mode field as a designer option. See section 20.8.1 for design consideration relating to the 11111 mode code indicator.

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\*20.4 Data bus cable.

\*20.4.1 Shielding. (4.5.1.1) The cable shield shall provide a minimum of 90.0 percent coverage.

\*20.4.2 Characteristic impedance. (4.5.1.2) The actual (not nominal) characteristic impedance shall be within the range of 70.0 Ohms to 85.0 Ohms at a sinusoidal frequency of 1.0 megahertz (MHz).

\*20.5 Cable coupling. (4.5.1.5.1.3) For Air Force avionics applications, the continuous shielding shall provide a minimum of 90.0 percent coverage.

\*20.6 Direct coupled stubs. (4.5.1.5.2) Direct coupled stubs shall not be utilized in Air Force avionics applications.

\*20.7 Redundant data bus requirements. (4.6) Dual standby redundant data buses as defined in 4.6.3 shall be utilized. There may be more than two data buses utilized but the buses must operate in dual redundant data bus pairs. 4.6.1 and 4.6.2 shall also apply.

\*20.8 Design considerations. Avionics designed for Air Forces applications may be required to interface to existing avionics systems which were designed to preceding versions of the standard (e.g., the F-16 avionics suite). In this case, downward compatibility problems between the new avionics and the existing system can be minimized through the consideration of three key items:

\*20.8.1 Mode code indicator. In some existing systems, such as the F-16, the bus controller uses 11111 to indicate a mode code command. The designer may wish to implement the capability in the new avionics to respond to 11111 mode code commands, in addition to the required capability for 00000 mode code commands.

\*20.8.2 Clock stability. Since this version of the standard relaxed the transmission bit rate stability requirements (4.3.3.3), the avionics designer may wish to return to the stability requirements of the preceding version of the standard. The previous requirements were  $\pm 0.01$  percent long term and  $\pm 0.001$  percent short term stability.

\*20.8.3 Response time. This version of the standard also expanded the maximum response time to 12.0 microseconds (4.3.3.8). The designer may also wish to return to the previous maximum response time of 7.0 microseconds as defined in 4.3.3.8 of this version of the standard.

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IV.  
NOTICE II

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MIL-STD-1553B  
NOTICE 2  
8 September 1986

MILITARY STANDARD

DIGITAL TIME DIVISION

COMMAND/RESPONSE MULTIPLEX DATA BUS

TO ALL HOLDERS OF MIL-STD-1553B:

1. MAKE THE FOLLOWING PEN AND INK CHANGES:

Page i

Delete title and substitute: "DIGITAL TIME DIVISION COMMAND/RESPONSE MULTIPLEX DATA BUS".

Page ii

Delete title and substitute: "Digital Time Division Command/Response Multiplex Data Bus".

Page 1

Paragraph 1.1, second line: Delete "on aircraft".

Paragraph 1.2, third line: Delete "an aircraft" and substitute "a".

Page 3

Paragraph 3.11, first line, after "Bus controller": Insert "(BC)".

Paragraph 3.12, first line, after "Bus monitor": Insert "(BM)".

Page 21

Paragraph 4.4.3.1, add: "No combination of RT address bits, T/R bit, subaddress/mode bits, and data word count/mode code bits of a command word shall result in invalid transmissions by the RT. Subsequent valid commands shall be properly responded to by the RT."

Page 30

Paragraph 4.6.3.2, first line: Delete "Reset data-bus transmitter" and substitute "Superseding valid commands".

Paragraph 4.6.3.2, second line: Delete "from either data bus" and substitute "from the other data bus".

Page 31

Paragraph 10.2, eighth line: Delete "airborne".

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33	21 September 1978	33	Reprinted Without Change
34	8 September 1986	34	12 February 1980
35	8 September 1986	35	12 February 1980
36	8 September 1986	INITIAL PUBLICATION	
37	8 September 1986	INITIAL PUBLICATION	
38	8 September 1986	INITIAL PUBLICATION	

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Air Force - 11

Preparing activity:  
Air Force - 11

Project No. MCCR-0008

FOREWORD

This standard contains requirements for a digital time division command/response multiplex data bus for use in systems integration. Even with the use of this standard, differences may exist between multiplex data buses in different system applications due to particular application requirements and the designer options allowed in this standard. The system designer must recognize this fact and design the multiplex bus controller hardware and software to accommodate such differences. These designer selected options must exist to allow the necessary flexibility in the design of specific multiplex systems in order to provide for the control mechanism, architectural redundancy, degradation concept and traffic patterns peculiar to the specific application requirements. Appendix, Section 30 selects those options which shall be required and further restricts certain portions of the standard for the use in all dual standby redundant applications for the Army, Navy, and Air Force.

Supersedes page iii dated 12 February 1980.



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10.3 Multiplex selection criteria. The selection of candidate signals for multiplexing is a function of the particular application involved, and criteria will in general vary from system to system. Obviously, those signals which have bandwidths of 400 Hz or less are prime candidates for inclusion on the bus. It is also obvious that video, audio, and high speed parallel digital signals should be excluded. The area of questionable application is usually between 400 Hz and 3KHz bandwidth. The transfer of these signals on the data bus will depend heavily upon the loading of the bus in a particular application. The decision must be based on projected future bus needs as well as the current loading. Another class of signals which in general are not suitable for multiplexing are those which can be typified by a low rate (over a mission) but possessing a high priority or urgency. Examples of such signals might be a nuclear event detector output or a missile launch alarm from a warning receiver. Such signals are usually better left hardwired, but they may be accommodated by the multiplex system if a direct connection to the bus controller's interrupt hardware is used to trigger a software action in response to the signal.

10.4 High reliability requirements. The use of simple parity for error detection within the multiplex bus system was dictated by a compromise between the need for reliable data transmission, system overhead, and remote terminal simplicity. Theoretical and empirical evidence indicates that an undetected bit error rate of  $10^{-12}$  can be expected from a practical multiplex system built to this standard. If a particular signal requires a bit error rate which is better than that provided by the parity checking, then it is incumbent upon the system designer to provide the reliability within the constraints of the standard or to not include this signal within the multiplex bus system. A possible approach in this case would be to have the signal source and sink provide appropriate error detection and correction encoding/decoding and employ extra data words to transfer the information. Another approach would be to partition the message, transmit a portion at a time, and then verify (by interrogation) the proper transfer of each segment.

10.5 Stubbing. Stubbing is the method wherein a separate line is connected between the primary data bus line and a terminal. The direct connection of a stub line causes a mismatch which appears on the waveforms. This mismatch can be reduced by filtering at the receiver and by using bi-phase modulation. Stubs are often employed not only as a convenience in bus layout but as a means of coupling a unit to the line in such a manner that a fault on the stub or terminal will not greatly affect the transmission line operation. In this case, a network is employed in the stub line to provide isolation from the fault. These networks are also used for stubs that are of such length that the mismatch and reflection degrades bus operation. The preferred method of stubbing is to use transformer coupled stubs, as defined in 4.5.1.5.1. This method provides the benefits of DC isolation, increased common mode protection, a doubling of effective stub impedance, and fault isolation for the entire stub and terminal. Direct coupled stubs, as defined in 4.5.1.5.2 of this standard, should be avoided if at all possible. Direct coupled stubs provide no DC isolation or common mode rejection for the terminal external to its subsystem. Further, any shorting fault between the subsystems internal isolation resistors (usually on a circuit board) and the main bus junction will cause failure of that entire bus. It can be expected that when the direct coupled stub length exceeds 1.6 feet, that it will begin to distort the main bus waveforms. Note that this length includes the cable runs internal to a given subsystem.

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- \* 10.6 Use of broadcast option. The use of a broadcast message as defined in 4.3.3.6.7 of this standard represents a significant departure from the basic philosophy of this standard in that it is a message format which does not provide positive closed-loop control of bus traffic. The system designer is strongly encouraged to solve any design problems through the use of the three basic message formats without resorting to use of the broadcast option. If system designers do choose to use the broadcast command, they should carefully consider the potential effects of a missed broadcast message, and the subsequent implications for fault or error recovery design in the remote terminals and bus controllers.
- \* 10.7 Other related documents. Several documents exist which are related to this standard. MIL-HDBK-1553 describes implementation practices for this standard and other related data. This standard is embodied in or referenced by the following international documents: NATO STANAG 3838, ASCC Air Standard 50/2, and UK DEF STAN 00-18 (PART 2)/Issue 1.
- \* 20. REFERENCED DOCUMENTS  
  
Not applicable.
- \* 30. GENERAL REQUIREMENTS
- \* 30.1 Option selection. This section of the appendix shall select those options required to further define portions of the standard to enhance tri-service interoperability. References in parentheses are to paragraphs in this standard which are affected.
- \* 30.2 Application. Section 30 of this appendix shall apply to all dual standby redundant applications for the Army, Navy, and Air Force. All Air Force aircraft internal avionics applications shall be dual standby redundant, except where safety critical or flight critical requirements dictate a higher level of redundancy.
- \* 30.3 Unique address (4.3.3.5.1.2). All remote terminals shall be capable of being assigned any unique address from decimal address 0 (00000) through decimal address 30 (11110). The address shall be established through an external connector, which is part of the system wiring and connects to the remote terminal. Changing the unique address of a remote terminal shall not require the physical modification or manipulation of any part of the remote terminal. The remote terminal shall, as a minimum, determine and validate its address during power-up conditions. No single point failure shall cause a terminal to validate a false address. The remote terminal shall not respond to any messages if it has determined its unique address is not valid.

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\* 30.4 Mode codes (4.3.3.5.1.7)

\* 30.4.1 Subaddress/mode (4.3.3.5.1.4). An RT shall have the capability to respond to mode codes with both subaddress/mode of 00000 and 11111. Bus controllers shall have the capability to issue mode commands with both subaddress/mode of 00000 and 11111. The subaddress/mode of 00000 and 11111 shall not convey different information.

\* 30.4.2 Required mode codes (4.3.3.5.1.7)

\* 30.4.2.1 Remote terminal required mode codes. An RT shall implement the following mode codes as a minimum:

<u>Mode Code</u>	<u>Function</u>
00010	Transmit status word
00100	Transmitter shutdown
00101	Override transmitter shutdown
01000	Reset remote terminal

\* 30.4.2.2 Bus controller required mode codes. The bus controller shall have the capability to implement all of the mode codes as defined in 4.3.3.5.1.7. For Air Force applications, the dynamic bus control mode command shall never be issued by the bus controller.

\* 30.4.3 Reset remote terminal (4.3.3.5.1.7.9). An RT receiving the reset remote terminal mode code shall respond with a status word as specified in 4.3.3.5.1.7.9 and then reset. While the RT is being reset, the RT shall respond to a valid command with any of the following: no response on either data bus, status word transmitted with the busy bit set, or normal response. If any data is transmitted from the RT while it is being reset, the information content of the data shall be valid. An RT receiving this mode code shall complete the reset function within 5.0 milliseconds following transmission of the status word specified in 4.3.3.5.1.7.9. The time shall be measured from the mid-bit zero crossing of the parity bit of the status word to the mid-sync zero crossing of the command word at point A on figures 9 and 10.

\* 30.4.4 Initiate RT self test (4.3.3.5.1.7.4). If the initiate self test mode command is implemented in the RT, then the RT receiving the initiate self test mode code shall respond with a status word as specified in 4.3.3.5.1.7.4 and then initiate the RT self test function. Subsequent valid commands may terminate the self-test function. While the RT self test is in progress, the RT shall respond to a valid command with any of the following: no response on either data bus, status word transmitted with the busy bit set, or normal response. If any data is transmitted from the RT while it is in self test, the information content of the data shall be valid. An RT receiving this mode code shall complete the self test function and have the results of the self test available within 100.0 milliseconds following transmission of the status word specified in 4.3.3.5.1.7.4. The time shall be measured from the mid-bit zero crossing of the parity bit of the status word to the mid-sync zero crossing of the command word at point A on figures 9 and 10.

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\* 30.5 Status word bits (4.3.3.5.3)

30.5.1 Information content. The status word transmitted by an RT shall contain valid information at all times, e.g., following RT power up, during initialization, and during normal operation.

\* 30.5.2 Status bit requirements (4.3.3.5.3). An RT shall implement the status bits as follows:

Message error bit (4.3.3.5.3.3) - Required

Instrumentation bit (4.3.3.5.3.4) - Always logic zero

Service request bit (4.3.3.5.3.5) - Optional

Reserved status bits (4.3.3.5.3.6) - Always logic zero

Broadcast command received bit (4.3.3.5.3.7) - If the RT implements the broadcast option, then this bit shall be required.

Busy bit (4.3.3.5.3.8) - As required by 30.5.3

Subsystem flag bit (4.3.3.5.3.9) - If an associated subsystem has the capability for self test, then this bit shall be required.

Dynamic bus control acceptance bit (4.3.3.5.3.10) - If the RT implements the dynamic bus control function, then this bit shall be required.

Terminal flag bit (4.3.3.5.3.11) - If an RT has the capability for self test, then this bit shall be required.

\* 30.5.3 Busy bit (4.3.3.5.3.8). The existence of busy conditions is discouraged. However, any busy condition, in the RT or the subsystem interface that would affect communication over the bus shall be conveyed via the busy bit. Busy conditions, and thus the setting of the busy bit, shall occur only as a result of particular commands/messages sent to an RT. Thus for a non-failed RT, the bus controller can, with prior knowledge of the remote terminal characteristics, determine when the remote terminal can become busy and when it will not be busy. However, the RT may also set the busy bit (in addition to setting the terminal flag bit or subsystem flag bit) as a result of failure/fault conditions within the RT/subsystem.

\* 30.6 Broadcast (4.3.3.6.7). The only broadcast commands allowed to be transmitted on the data bus by the bus controller shall be the broadcast mode commands identified in table 1. The broadcast option may be implemented in remote terminals. However, if implemented, the RT shall be capable of distinguishing between a broadcast and a non-broadcast message to the same subaddress for non-mode command messages. The RT address of 11111 is still reserved for broadcast and shall not be used for any other purpose.



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- \* 30.7 Data wrap-around (4.3.3.5.1.4). Remote terminals shall provide a receive subaddress to which one to N data words of any bit pattern can be received. Remote terminals shall provide a transmit subaddress from which a minimum of N data words can be transmitted. N is equal to the maximum word count from the set of all messages defined for the RT. A valid receive message to the data wrap-around receive subaddress followed by a valid transmit command to the data wrap-around transmit subaddress, with the same word count and without any intervening valid commands to that RT, shall cause the RT to respond with each data word having the same bit pattern as the corresponding received data word. A data wrap-around receive and transmit subaddress of 30 (11110) is desired.
- \* 30.8 Message formats (4.3.3.6). Remote terminals shall, as a minimum, implement the following non-broadcast message formats as defined in 4.3.3.6: RT to BC transfers, BC to RT transfers, RT to RT transfers (receive and transmit), and mode command without data word transfers. For non-broadcast messages, the RT shall not distinguish between data received during a BC to RT transfer or data received during a RT to RT transfer (receive) to the same subaddress. The RT shall not distinguish between data to be transmitted during an RT to BC transfer or data to be transmitted during an RT to RT transfer (transmit) from the same subaddress. Bus controllers shall have the capability to issue all message formats defined in 4.3.3.6.
- \* 30.9 RT to RT validation (4.3.3.9). For RT to RT transfers, in addition to the validation criteria specified in 4.4.3.6, if a valid receive command is received by the RT and the first data word is received after 57.0 plus or minus 3.0 microseconds, the RT shall consider the message invalid and respond as specified in 4.4.3.6. The time shall be measured from the mid-bit zero crossing of the parity bit of the receive command to the mid-sync zero crossing of the first expected data word at point A as shown on figures 9 and 10. It is recommended that the receiving RT of an RT to RT transfer verify the proper occurrence of the transmit command word and status word as specified in 4.3.3.6.3.
- \* 30.10 Electrical characteristics (4.5)
  - \* 30.10.1 Cable shielding (4.5.1.1). The cable shield shall provide a minimum of 90.0 percent coverage.
  - \* 30.10.2 Shielding (4.5.1). All cable to connector junctions, cable terminations, and bus-stub junctions shall have continuous 360 degree shielding which shall provide a minimum of 75.0 percent coverage.
  - \* 30.10.3 Connector polarity. For applications that use concentric connectors or inserts for each bus, the center pin of the connector or insert shall be used for the high (positive) Manchester bi-phase signal. The inner ring shall be used for the low (negative) Manchester bi-phase signal.
  - \* 30.10.4 Characteristic impedance (4.5.1.2). The actual (not nominal) characteristic impedance of the data bus cable shall be within the range of 70.0 ohms to 85.0 ohms at a sinusoidal frequency of 1.0 megahertz.



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- \* 30.10.5 Stub coupling (4.5.1.5). For Navy applications, each terminal shall have both transformer and direct coupled stub connections externally available. For Navy systems using these terminals, either transformer or direct coupled connections may be used. For Army and Air Force applications, each terminal shall have transformer coupled stub connections, but may also have direct coupled stub connections. For Army and Air Force systems, only transformer coupled stub connections shall be used. Unused terminal connections shall have a minimum of 75 percent shielding coverage.
- \* 30.10.6 Power on/off noise. A terminal shall limit any spurious output during a power-up or power-down sequence. The maximum allowable output noise amplitude shall be  $\pm 250$  mV peak, line-to-line for transformer coupled stubs and  $\pm 90$  mV peak, line-to-line for direct coupled stubs, measured at point A of figure 12.

**V.  
PRODUCTION  
TEST PLAN  
FOR REMOTE TERMINALS**

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## 1. SCOPE:

This test plan is broken into two major sections for the production testing of remote terminals: Electrical and Protocol.

1.1 General: This production test plan defines the test requirements for verifying that Remote Terminals meet the requirements of MIL-STD-1553B, "Digital Time Division Command/Response Multiplex Data Bus."

1.2 Application: This is a general test plan for any remote terminal designed to meet the requirements of MIL-STD-1553B. These requirements shall apply to the remote terminal under test, when invoked in a specification or statement of work.

Tests specified may be performed in any order, combined with one another or combined with other tests of the subsystem in which the Remote Terminal may be embedded.

The Remote Terminal which is under test must also have its design validated per the "Validation Test Plan for the Digital Time Division Command/Response Multiplex Data Bus Remote Terminals."

The tests specified are to be used in production test of a remote terminal chip, module or function within an equipment. It is intended that all stimuli and measurements be made via external connections and/or test points. No required access to any other points is intended.

Special requirements such as those needed to meet armament bus requirements when specified in the individual equipment specification may, when within 1553B requirements, replace values or tolerances specified in this test plan for the purpose of generating a UUT production test procedure.

## 2. APPLICABLE DOCUMENTS:

2.1 Standards, Military: MIL-STD-1553B, 21 Sep 1978, "Aircraft Internal Time Division Command/Response Multiplex Data Bus" with Notice 2, 8 September 1986.

2.2 Other Documents: MIL-HDBK-1553, Notice 1, 24 September 1986 "Validation Test Plan for the Digital Time Division Command/Response Multiplex Data Bus Remote Terminals."

## 3. DEFINITIONS:

3.1 Responses: The following are definitions of the responses of the RT as used in this test plan. In each case, the status word must have the correct terminal address and unused status bits set to zero.

3.1.1 BCR - Broadcast Command Received: The broadcast command received bit (bit time 15) is set in status word.

3.1.2 BUSY - Busy: The busy bit (bit time 16) is set in the status word.

- 3.1.3 CS - Clear Status: The status word may have the busy bit or service request bit set, or both. All other status code bits in the status word must be zero and the associated message must have the proper word count.
- 3.1.4 DBA - Dynamic Bus Acceptance: The dynamic bus control acceptance bit (bit time 18) is set in the status word.
- 3.1.5 ME - Message Error: The message error bit (bit time 9) is set in the status word.
- 3.1.6 NR - No Response: The addressed terminal does not produce any response to the command.
- 3.1.7 Respond in Form: A terminal is said to "respond in form" if its response to an illegal command as defined in 4.4.3.4 of MIL-STD-1553B consists of a response formatted as though it were a legal command.
- 3.1.8 SF - Subsystem Flag: The subsystem flag bit (bit time 17) is set in the status word.
- 3.1.9 TF - Terminal Flag: The terminal flag bit (bit time 19) is set in the status word.
- 3.2 Other Definitions:
  - 3.2.1 UUT - Unit Under Test.
  - 3.2.2 RT - Remote Terminal.
  - 3.2.3 BC - Bus Controller.
- 4. GENERAL TEST REQUIREMENTS:

The following paragraphs define the configurations, pass/fail criteria, and general procedures for testing remote terminals. Specifically, this document contains the test configurations and procedures for the Electrical Tests (5.1) and the Protocol Tests (5.2) for MIL-STD-1553B remote terminals. The remote terminal under test is referred to as the unit under test (UUT). Proper terminal responses are defined in each test paragraph.

- 4.1 General Monitoring Requirements: In addition to the specific tests that follow, certain RT parameters must be continuously monitored throughout all tests. These parameters are:

1. response time
2. contiguous data
3. proper Manchester encoding
4. proper bit count
5. odd parity
6. proper word count
7. proper terminal address in the status word
8. reserved status and instrumentation bits in the status word are set to zero
9. proper sync

The UUT shall have failed the test if at any time during the test any of these parameters fail to meet the requirements of MIL-STD-1553B.

5. DETAILED REQUIREMENTS:

- 5.1 Electrical Tests: All tests shall use Fig. 1, General Test Configuration, with all measurements taken at point "A", unless otherwise noted. Each test paragraph contains the requirements for both transformer and direct coupled stubs. A UUT which provides both transformer and direct coupled stubs must be tested on both stubs. Electrical tests shall be performed on all buses for UUTs with redundant bus configurations.

- 5.1.1 Output Characteristics: The following tests are designed to verify that all UUT output characteristics comply with MIL-STD-1553B. These tests shall be performed after establishing communications between the test equipment and the UUT.

If necessary, use the Optional Test Configuration, Fig. 2, in order to isolate the UUT output from any reactive load presented by the Tester.

- 5.1.1.1 Amplitude: A valid, legal transmit command shall be transmitted to the UUT, requesting the maximum number of words that it is capable of sending. The amplitude of the waveform transmitted by the UUT shall be measured, peak-to-peak, as shown in Fig. 3. The pass criteria for  $V_{pp}$  for transformer coupled stubs shall be 18.0 V minimum and 27.0 V maximum. The pass criteria for  $V_{pp}$  for direct coupled stubs shall be 6.0 V minimum and 9.0 V maximum.
- 5.1.1.2 Rise and Fall Times: A valid, legal transmit command shall be sent to the UUT, requesting at least one data word. The rise and fall time of the UUT waveform shall be measured between the 10 and 90% points of the waveform as shown in Fig. 3. The measurements shall be taken at both the rising and falling edges of a sync waveform and a data bit waveform. The rise time ( $T_R$ ) and the fall time ( $T_F$ ) shall be measured. The pass criteria shall be  $100 \text{ ns} \leq T_R \leq 300 \text{ ns}$  and  $100 \text{ ns} \leq T_F \leq 300 \text{ ns}$ .

5.1.1.2 (Continued):

Note: The rise time of the sync waveform shall be measured at the mid-crossing of a data word sync, and the fall time of the sync waveform shall be measured at the mid-crossing of the status word sync. The rise and fall times of the data bit waveform shall be measured at a zero crossing where the prior zero crossing and next zero crossing are at 500 ns intervals from the measured zero crossing.

5.1.1.3 Zero Crossing Stability: Selected valid legal transmit commands shall be sent to the UUT, requesting the UUT to transmit words having zero crossing time intervals of 500, 1000, 1500 and 2000 ns. The zero crossing time ( $T_{ZC}$ ) shall be measured for both the positive to negative and the negative to positive waveforms as shown in Fig. 4. The pass criteria shall be that  $T_{ZC} = 500 \pm 25$ ,  $1000 \pm 25$ ,  $1500 \pm 25$  and  $2000 \pm 25$  ns.

5.1.1.4 Distortion, Overshoot and Ringing: A valid legal transmit command shall be sent to the UUT, requesting the UUT to transmit at least one data word. The distortion of the waveform, distortion voltage ( $V_D$ ), shall be measured as indicated in Fig. 3. Pass criterion shall be  $V_D < = 900$  mV, for transformer coupled stubs and  $V_D < = 300$  mV, for direct coupled stubs.

5.1.1.5 Output Symmetry: A valid legal transmit command shall be sent to the UUT requesting the maximum number of data words that the UUT is capable of transmitting. The output symmetry is determined by measuring the waveform tail-off at the end of each message. The maximum residual voltage ( $V_R$ ) shall be measured as shown in Fig. 3. The intermessage gap time shall be a minimum of 1 ms. The pass criterion shall be  $V_R < = 250$  mV peak for transformer coupled stubs and  $V_R < = 90$  mV peak for direct coupled stubs after time  $T_T$  (the time beginning 2.5  $\mu$ s after the mid-bit zero crossing of the last parity bit). This test shall be run six times with each data word in the message having the same bit pattern.

The six data word patterns that shall be used are:

8000(HEX), 7FFF(HEX), 0000(HEX), FFFF(HEX),  
5555(HEX), and AAAA(HEX)

Note: For terminals that cannot transmit data words, the output symmetry test shall be performed on the status word response to a receive command or mode command.

5.1.1.6 Output Noise: The test configuration shown in Fig. 5 shall be used to test the UUT inactive bus output noise levels. The test shall be conducted while the UUT is in the power-on receive state. The output noise ( $V_{rms}$ ) shall be measured at point "A" as shown in Fig. 5. Measurements shall be made with an instrument that has a minimum frequency bandwidth of from DC to 10 MHz. The pass criterion shall be  $V_{rms} < = 14$  mV for transformer coupled stubs and  $V_{rms} < = 5.0$  mV for direct coupled stubs.

- 5.1.1.7 Power On/Off Noise: A UUT shall not emit any spurious differential output during a power-up or power-down sequence. Power shall be applied to the UUT and any outputs from the UUT to the bus shall be measured. Power shall be removed from the UUT and any output to the bus from the UUT shall be measured.

The pass criterion shall be:

1. For transformer coupled stubs, any spurious noise pulses produced shall be less than  $\pm 250$  mV peak.
2. For direct coupled stubs, any spurious noise pulses produced shall be less than  $\pm 90$  mV peak.

NOTE: Use normal on/off power sequence of UUT.

- 5.1.2 Input Characteristics: The input tests are designed to verify that multiplex devices can properly decode bi-phase data.

5.1.2.1 Input Waveform Compatibility:

- 5.1.2.1.1 Amplitude Variations: A sequence of valid legal receive commands shall be transmitted to the UUT. The test shall be performed for input voltage levels of 0.20, 0.86, and 6.0 Vpp for transformer coupled stubs, and at 0.28, 1.2, and 9.0 Vpp for direct coupled stubs. A minimum of 1000 commands shall be transmitted to the UUT at each input level. The response of the UUT shall be monitored for every message at each input level.

The pass criteria shall be:

1. NR for transformer coupled stub inputs of 0.20 Vpp.
2. CS for transformer coupled stub inputs of 0.86 Vpp.
3. CS for transformer coupled stub inputs of 6.0 Vpp.
4. NR for direct coupled stub inputs of 0.28 Vpp.
5. CS for direct coupled stub inputs of 1.2 Vpp.
6. CS for direct coupled stub inputs of 9.0 Vpp.

- 5.1.2.1.2 Input Impedance: The input impedance of the UUT shall be measured first with the power on and repeated with the UUT power off. The input impedance,  $Z_{in}$ , shall be measured with a sinusoidal waveform having an amplitude 1.0 to 2.0 Vrms, at a frequency of 1.0 MHz. The pass criterion shall be  $Z_{in} \geq 1000 \Omega$  for transformer coupled stubs and  $Z_{in} \geq 2000 \Omega$  for direct coupled stubs.

For this test, do not use Fig. 1; remove all loads from UUT.

- 5.2 Protocol Tests: All tests in this section shall use the test configuration shown in Fig. 1. The test signal amplitude shall be 3.0 Vpp for direct coupled stubs and 2.1 Vpp for transformer coupled stubs measured at point A. For UUTs having both direct and transformer coupled stubs, the protocol tests need only be performed on one stub type per bus. Any condition, which causes the UUT to respond other than as called out in MIL-STD-1553B, to lock up or require a power cycle in order to recover from a failure, shall automatically cause that UUT to fail the test. The protocol tests shall be performed on all buses for UUTs with redundant bus configurations.



## 5.2.1 RT Response to Command Words:

5.2.1.1 RT Address: The purpose of this test is to verify that the UUT responds only to valid legal commands, that is, those that contain the address of the UUT.

5.2.1.1.1 Valid RT Address: The test equipment shall transmit to the UUT one valid legal transmit command and one valid legal receive command with the minimum word count for the UUT. Associated data may be random or controlled depending on UUT requirements. The pass criteria shall be that the UUT responds with CS for each command. If the UUT has variable address capability, this test shall be repeated for the following addresses:

00001, 00010, 00100, 01000, 10000, 00000

5.2.1.1.2 Invalid RT Address: The test equipment shall transmit to the UUT receive commands and transmit commands using all RT addresses not assigned to the UUT (with the exception of address 11111). Subaddress and word count fields shall be identical to those used in 5.2.1.1.1. The pass criteria shall be NR for each command.

5.2.1.2 Word Count: The purpose of the test is to verify that the UUT responds properly to all word counts implemented. During the test, the test equipment will transmit one valid, legal, non-mode transmit command and one valid, legal, non-mode receive command for each implemented word count. Only one subaddress is needed for any word count. The pass criteria shall be CS for each command.

5.2.1.3 Subaddress: The purpose of this test is to verify that the UUT responds properly to all subaddresses implemented. During this test, the test equipment shall transmit one valid, legal, non-mode transmit command and one valid, legal, non-mode receive command for each implemented subaddress. Only one word count is needed for any subaddress. The pass criteria shall be CS for each command.

5.2.1.4 Error Injection: These tests are intended to examine the UUT response when specific errors are forced into the message stream. The UUT shall not respond with a status word. If the data words it decodes fail any of the validity tests, the UUT should internally set the message error bit in its status word buffer. If the command word it decodes fails any of the validity tests, it shall ignore the command and wait for the next command (the ME bit should not be internally set in this case). For this test, valid legal commands will be sent to the UUT for Steps 1 and 3 in the test sequence below. Each error condition listed in Table 1 shall be injected in Step 2 of the test sequence. One error per test sequence shall be implemented.

1. Transmit a valid, legal command to the UUT.
2. Transmit to the UUT a message which contains one of the error conditions listed in Table 1.
3. Transmit a valid, legal command to the UUT.

5.2.1.4 (Continued):

The pass criteria shall be:

1. The UUT shall respond with CS for Steps 1 and 3 in the test sequence above.
2. The UUT shall not respond to commands for Step 2 in the test sequence above.

5.2.2 Optional Operation: This section provides for testing the optional requirements of MIL-STD-1553B. If a remote terminal implements any of the options, it shall be tested in accordance with the test identified for the option.

5.2.2.1 Dual Redundant Operation: This test shall be performed only if the UUT is configured with dual redundant buses. The requirements are as follows:

1. The UUT is required to accept a valid command received on the alternate bus while responding to a command on the original bus.
2. The UUT is required to respond to the valid command occurring later in time when overlapping valid commands are received on both buses.
3. When Step 1 or 2 occurs, the UUT shall reset and respond to the new command on the alternate bus.

Legal messages shall be used in this test. The following test sequence shall be performed twice for each interrupting command, once for each redundant bus:

- Step 1. Send a valid command to the UUT requesting the maximum number of data words that the UUT is designed to transmit.
- Step 2. Send the interrupting command on the alternate bus beginning no sooner than 4.0  $\mu$ s after the beginning of the first command.
- Step 3. Send a valid "Transmit Status" mode command on the first bus after the messages on both buses have been completed. (If "Transmit Status" is not used, delete this step.)

The pass criteria shall be: Step 1 - NR, truncated message or CS, Step 2 - CS, and Step 3 - CS if transmit status is implemented.

5.2.2.2 Mode Commands: The purpose of these tests is to verify that the UUT responds properly to implemented mode commands. The tests are not intended to verify the mission aspects stated in the equipment specification. The UUT shall be tested for each mode code implemented with a subaddress field mode code indicator of all zeros and repeated with a subaddress field of all ones. The pass criteria are defined in each test paragraph.

TABLE 1 - Error Formats

ERROR TYPE	LOCATION
Parity	Receive command word
Parity	Transmit command word
Parity	Data word
Bit Count (-1 bit)	Receive command word
Bit Count (+2 bits)	Receive command word
Bit Count (-1 bit)	Transmit command word
Bit Count (+2 bits)	Between two data words
Bit Count (-1 bit)	Between two data words
Bi-phase (high)	Ripple through transmit command
Bi-phase (high)	Ripple through receive command
Bi-phase (low)	Ripple through transmit command
Bi-phase (low)	Ripple through receive command
Bi-phase (low)	Ripple through data word
Bi-phase (high)	Ripple through data word
Sync	Command word, patterns: 111100 110000 111001 011000 000111
Sync	Data word, patterns: 000011 001111 000110 100111 111000
Contiguous data	Between command and data words
Contiguous data	Between two data words
Message length (+)	Receive message plus one data word
Message length (-)	Receive message minus one data word
Message length (+)	Transmit command plus one data word

NOTE: For contiguous data errors, receive commands shall be used and the contiguous data error shall be 4.0  $\mu$ s as measured from the mid-bit zero crossing of the parity bit of the preceding word to the mid-sync zero crossing of the following word.

5.2.2.2.1 Dynamic Bus Control: The purpose of this test is to verify that the UUT has the ability to recognize the "Dynamic Bus Control" mode command and to take control of the data bus. A valid legal dynamic bus control mode command shall be sent to the UUT. The pass criteria shall be that the UUT responds with a DBA upon acceptance of bus control or a CS upon rejection of bus control. The UUT shall take control of the data bus when its response is DBA as required in the UUT's design specification.

5.2.2.2.2 Synchronize: The following paragraphs provide the test criteria for the "Synchronize" mode commands:

5.2.2.2.2.1 Synchronize (Without Data Word): The purpose of this test is to verify that the UUT has the ability to recognize a "Synchronize" mode command without a data word. A valid legal "Synchronize" (without data word) mode command shall be sent to the UUT. The pass criterion shall be that the UUT responds with CS.

5.2.2.2.2.2 Synchronize (With Data Word): The purpose of this test is to verify that the UUT has the ability to recognize a "Synchronize" mode command with a data word. A valid legal "Synchronize" (with data word) mode command shall be sent to the UUT. The pass criterion shall be that the UUT responds with CS.

5.2.2.2.3 Transmit Status: The purpose of this test is to verify that the UUT has the ability to recognize the "Transmit Status" mode command and respond with its last status word. The following sequence shall be performed:

- Step 1. A valid legal message shall be sent to the UUT.
- Step 2. A legal receive command with a parity error in a data word shall be sent to the UUT.
- Step 3. A valid legal "Transmit Status" mode command shall be sent to the UUT.
- Step 4. Repeat Step 3.
- Step 5. A valid legal receive command shall be sent to the UUT.

The pass criteria for the above steps shall be as follows: Step 1 - CS; Step 2 - NR; Step 3 - ME; Step 4 - ME; Step 5 - CS.

5.2.2.2.4 Initiate Self-Test: The purpose of this test is to verify that the UUT has the ability to recognize the "Initiate Self-Test" mode command. A valid legal "Initiate Self-Test" mode command shall be sent to the UUT. The pass criterion shall be that the UUT responds with CS.

Note: Normal UUT operation may be affected during the Self-Test execution time. Detailed requirements shall be as defined by the UUT's design specification.

5.2.2.2.5 Transmit BIT Word: The purpose of this test is to verify that the UUT has the ability to recognize the "Transmit BIT Word" mode command. A valid legal "Transmit BIT Word" mode command shall be sent to the UUT. The pass criterion shall be that the UUT responds with a CS followed by a valid data word.

5.2.2.2.6 Transmitter Shutdown and Override: The purpose of this test is to verify that the UUT has the ability to recognize the "Transmitter Shutdown" and "Override Transmitter Shutdown" mode commands. The pass criterion for each individual test is contained in one of the paragraphs below. To test all bus combinations, in this sequence each bus in turn shall be identified as the primary bus. All other buses shall be tested in turn as the selected alternate bus using Steps 1 through 10.

- Step 1. A valid legal command shall be sent on the primary bus to the UUT. A CS response shall be verified.
- Step 2. A valid legal command shall be sent on the selected alternate bus to the UUT. A CS response shall be verified.
- Step 3. A valid legal mode command to shut down the transmitter shall be sent to the UUT on the primary bus. A CS response shall be verified.
- Step 4. A valid legal command shall be sent on the selected alternate bus to the UUT. A NR shall be verified.
- Step 5. A valid legal command shall be sent on the primary bus to the UUT. A CS response shall be verified.
- Step 6. A valid legal mode command to override the transmitter shutdown shall be sent to the UUT on the selected alternate bus. A NR shall be verified.
- Step 7. A valid legal command shall be sent to the UUT on the selected alternate bus. A NR shall be verified.
- Step 8. A valid legal mode command to override transmitter shutdown shall be sent to the UUT on the primary bus. A CS shall be verified.
- Step 9. A valid legal command shall be sent on the selected alternate bus to the UUT. A CS shall be verified.
- Step 10. A valid legal command shall be sent on the primary bus to the UUT. A CS shall be verified.

5.2.2.2.6.1 Dual Redundant Shutdowns and Overrides: This test shall verify that the UUT recognizes the dual redundant mode commands to shut down the alternate bus transmitter and to override the shutdown.

A valid legal "Transmitter Shutdown" mode command shall be encoded into the command word to cause an alternate bus transmitter shutdown. A valid legal "Override Transmitter Shutdown" mode command shall be encoded into the command word to cause an override of the transmitter shutdown. The test sequence in 5.2.2.2.6 shall be used for each case including verification of the UUT response indicated. The pass criterion shall be that the UUT performs as defined in each step.



5.2.2.2.6.2 Selective Bus Shutdowns and Overrides: This test shall verify that the UUT recognizes the multi-redundant mode commands to shut down a selected bus transmitter and to override the shutdown. A valid legal "Selected Transmitter Shutdown" receive mode command shall be encoded, accompanied by the appropriate data word, to cause a selective bus transmitter shutdown. A valid legal "Override Selected Transmitter Shutdown" receive mode command shall be encoded accompanied by the appropriate data word to cause an override of the selected bus transmitter shutdown. The test sequence in 5.2.2.2.6 shall be used for each case including verification of the UUT response indicated. The pass criteria shall be that the UUT performs as defined in each step.

5.2.2.2.7 Terminal Flag Bit Inhibit and Override: This test verifies that the UUT recognizes and responds properly to the mode commands of "Inhibit Terminal Flag Bit" and "Override Inhibit Terminal Flag Bit." Beginning in Step 2 of the test sequence below, the UUT shall be caused to set the terminal flag bit.

- Step 1. A valid legal receive command with at least one data word shall be transmitted to the UUT and a CS response verified.
- Step 2. Introduce a condition that will set the terminal flag in the UUT status response. Send a valid legal receive command with at least one data word to the UUT and verify that the TF bit is set in the returned status word.
- Step 3. A valid legal "Inhibit Terminal Flag" mode command shall be transmitted to the UUT and a CS or TF response verified.
- Step 4. Repeat Step 1 and verify a CS response.
- Step 5. A valid legal "Override Inhibit Terminal Flag" mode command shall be transmitted to the UUT and a CS or TF verified in the returned status word.
- Step 6. A valid legal receive command with at least one data word shall be transmitted and a TF verified in the returned status word.
- Step 7. Procedures, as defined for the UUT, shall be performed which reset the TF bit.
- Step 8. Repeat Step 1.

The pass criterion shall be that the UUT performs as defined in each step.

5.2.2.2.8 Reset Remote Terminal: This test shall verify that the UUT has the capability to recognize the mode command to reset itself to a power up initialized state. For this test, a reset mode command shall be transmitted to the UUT and a CS response verified.

Note: Normal UUT operation may be affected during the reset execution time. Detailed requirements shall be as defined by the UUT's design specification.

5.2.2.2.9 Transmit Vector Word: This test verifies the capability of the UUT to recognize and respond properly to a "Transmit Vector Word" mode command. A valid legal "Transmit Vector Word" mode command shall be transmitted to the UUT and a CS response shall be verified.

5.2.2.2.10 Transmit Last Command: This test verifies that the UUT recognizes and responds properly to a "Transmit Last Command" mode command. The following test sequence shall be used:

Step 1. A valid legal receive command with at least one data word shall be transmitted to the UUT and a CS response verified.

Step 2. A valid legal receive command, different from that used in Step 1 above with at least one data word, shall be transmitted to the UUT and a parity error shall be encoded into the first data word. A NR shall be the proper UUT action.

Step 3. A valid legal "Transmit Last Command" mode command shall be transmitted to the UUT and a status response of ME followed by a data word containing the last command (command word from Step 2) shall be verified.

Step 4. A valid legal "Transmit Status" mode command shall be transmitted to the UUT and a status response with a ME set shall be verified.

Step 5. A valid legal "Transmit Last Command" mode command shall be transmitted to the UUT and a status response of ME followed by a data word containing the last command (command word from Step 4) shall be verified.

Step 6. A valid legal "Transmit Last Command" mode command shall be transmitted to the UUT and a status response of ME followed by a data word containing the last command (command word from Step 4) shall be verified.

Step 7. A valid legal receive command with at least one data word shall be transmitted to the UUT and a CS response verified.

Step 8. A valid legal "Transmit Last Command" mode command shall be transmitted to the UUT and a status response of CS followed by a data word containing the last command (command word from Step 7) shall be verified.

5.2.2.3 Status Word: The following tests verify that all implemented status word bits are properly used and cleared. The UUT has failed a test sequence if it does not respond as indicated in each test paragraph for any implemented status word bit.

5.2.2.3.1 Service Request: This test verifies that the UUT sets the service request bit as necessary and clears it when appropriate. The UUT shall set bit time 11 of the status word when a condition in the UUT warrants the RT to be serviced. A reset of the bit shall occur as defined by each RT. The following steps shall be performed and the appropriate responses verified:

- Step 1. A valid legal receive command with at least one data word shall be transmitted to the UUT and a CS response with the service request bit reset verified.
- Step 2. A condition, which causes the service request bit to be set, shall be introduced into the UUT. A valid legal receive command with at least one data word shall be transmitted to the UUT and a status response having the service request bit set shall be verified.
- Step 3. A valid legal receive command with at least one data word shall be transmitted to the UUT and a status response having the service request bit set shall be verified.
- Step 4. Procedures, as defined for the UUT, shall be performed which reset the service request bit. A valid legal receive command with at least one data word shall be transmitted to the UUT and a CS response with the service request bit reset shall be verified.

The pass criterion for this test shall be the successful completion of Steps 1 through 4.

5.2.2.3.2 Broadcast: This test verifies that the UUT sets the broadcast command received bit of the status word after receiving a broadcast command. The UUT shall set status bit 15 to a logic one after receiving the broadcast command. The following test sequence shall be performed using either the "Transmit Last Command" or "Transmit Status" mode command to verify the bit condition.

- Step 1. A valid legal broadcast receive message shall be transmitted to the UUT. A NR shall be verified.
- Step 2. A valid legal "Transmit Last Command" or "Transmit Status" mode command shall be transmitted to the UUT. In either case, verify BCR. If the "Transmit Last Command" mode command is used, the data word containing the broadcast command shall be verified.
- Step 3. A valid, legal, non-broadcast command shall be transmitted to the UUT and a status word with the broadcast command received bit reset shall be verified.
- Step 4. A broadcast receive message with a parity error in one of the data words shall be transmitted to the UUT. A NR shall be verified.

5.2.2.3.2 (Continued):

Step 5. A valid legal "Transmit Last Command" or "Transmit Status" mode command shall be transmitted to the UUT. In either case, a status word with the message error bit set shall be verified. (BCR may be set.) If the "Transmit Last Command" mode command is used, the data word containing the broadcast command shall be verified.

The pass criterion for this test shall be the successful completion of Steps 1 through 5.

5.2.2.3.3 Busy: This test verifies the capability of the UUT to set the busy bit of the status word. Bit time 16 of the status word shall be set when the UUT is busy.

Step 1. Procedures as defined for the UUT shall be performed which set the busy bit.

Step 2. A valid legal transmit command shall be transmitted to the UUT and only a status word response with the busy bit set shall be verified. The UUT shall not transmit the requested data words when the busy bit is set.

Step 3. Procedures, as defined for the UUT, shall be performed which reset the busy bit.

Step 4. A valid legal transmit command shall be transmitted to the UUT and a status word with the busy bit reset shall be verified. The UUT shall have responded with the correct number of data words.

Step 5. Repeat Step 1.

Step 6. A valid legal receive command shall be transmitted to the UUT and a status word response with the busy bit set shall be verified.

Step 7. Repeat Step 3.

Step 8. A valid legal receive command shall be transmitted to the UUT and a status word response with the busy bit reset shall be verified.

The pass criterion for this test shall be the successful completion of Steps 1 through 8.

5.2.2.3.4 Subsystem Flag: This test verifies the capability of the UUT to set the subsystem flag bit of the status word. Bit time 17 of the status word shall be set to a logic one when a subsystem fault has been determined. Prior to performing the test sequence below, a condition, which sets the subsystem flag bit, must be activated.

Step 1. A valid legal transmit command shall be transmitted to the UUT and a status response having the subsystem flag bit set shall be verified.

Step 2. Procedures, as defined for the UUT, shall be performed which reset the subsystem flag bit.

5.2.2.3.4 (Continued):

Step 3. A valid legal transmit command shall be transmitted to the UUT and a status word with the subsystem flag bit reset shall be verified.

The pass criterion for this test shall be the successful completion of Steps 1 through 3.

5.2.2.3.5 Terminal Flag: This test verifies that the UUT sets the terminal flag bit as necessary and clears it when appropriate. The UUT shall set bit time 19 of the status word when an occurrence in the UUT causes a terminal fault condition. Prior to performing the test sequence below, a condition which sets the terminal flag bit must be activated.

Step 1. A valid legal receive command with at least one data word shall be transmitted to the UUT and a status response with the TF bit set shall be verified.

Step 2. Procedures, as defined for the UUT, shall be performed which reset the TF bit.

Step 3. A valid legal transmit command shall be transmitted to the UUT and a status word with the TF bit reset shall be verified.

The pass criterion for this test shall be the successful completion of Steps 1 through 3.

5.2.2.4 Broadcast Messages: The following tests verify that the UUT responds properly to broadcast messages.

Note: In the following test sequences, a "Transmit Last Command" mode command shall be used to verify the reception of the broadcast message by the UUT. If the "Transmit Last Command" mode command is not implemented, the "Transmit Status" mode command shall be used. If neither mode command is implemented, this test will not be performed.

5.2.2.4.1 Response to Broadcast Commands: The purpose of this test is to verify that the UUT responds properly to broadcast commands. The commands are classified into three categories. BC to RT broadcast commands, broadcast mode commands, and RT to RT broadcast commands. Each category is tested separately in the following paragraphs. Use the following test sequence unless otherwise noted:

Step 1. A valid legal receive message shall be sent to the UUT.

Step 2. A valid legal broadcast message shall be sent to the UUT.

Step 3. A "Transmit Last Command" mode command shall be sent to the UUT.



- 5.2.2.4.1.1 BC to RT Broadcast Commands: All possible broadcast commands meeting the criteria of 4.4.1.1 of MIL-STD-1553B except broadcast mode commands shall be sent to the UUT. Each command word shall be followed by the proper number of contiguous valid data words.

The pass criteria are as follows: Step 1 - CS; Step 2 - NR; Step 3 - BCR and the data word contains the broadcast command sent in Step 2.

- 5.2.2.4.1.2 Broadcast Mode Commands: The purpose of this test is to verify that the UUT responds properly to implemented broadcast mode commands. This test is not intended to verify the mission aspects stated in the equipment specification. The UUT shall be tested for each mode code implemented with a subaddress field mode code indicator of all zeros and repeated with a subaddress field of all ones. The pass criteria are defined in each test paragraph.

- 5.2.2.4.1.2.1 Broadcast Synchronize (Without Data Word): The purpose of this test is to verify that the UUT has the ability to recognize a broadcast "Synchronize" (without data word) mode command. The test sequence defined in 5.2.2.4.1 shall be used with a broadcast "Synchronize" (without data word) mode command in Step 2. The pass criteria for the above steps shall be as follows: Step 1 - CS; Step 2 - NR; Step 3 - BCR and the data word contains the broadcast command sent in Step 2.

- 5.2.2.4.1.2.2 Broadcast Synchronize (With Data Word): The purpose of this test is to verify that the UUT has the ability to recognize a broadcast "Synchronize" (with data word) mode command. The test sequence defined in 5.2.2.4.1 shall be used with a broadcast "Synchronize" (with data word) mode command in Step 2. The pass criteria for the above steps shall be as follows: Step 1 - CS; Step 2 - NR; Step 3 - BCR and the data word contains the broadcast command sent in Step 2.

- 5.2.2.4.1.2.3 Broadcast Initiate Self-Test: The purpose of this test is to verify that the UUT has the ability to recognize the broadcast "Initiate Self-Test" mode command. The test sequence defined in 5.2.2.4.1 shall be used with a broadcast "Initiate Self-Test" mode command in Step 2. The pass criterion for each of the above steps shall be as follows: Step 1 - CS; Step 2 - NR; Step 3 - BCR and the data word contains the broadcast command sent in Step 2.

Note: Normal UUT operation may be affected during the Self-Test execution time. Detailed requirements shall be as defined by the UUT's design specification.

5.2.2.4.1.2.4 Broadcast Transmitter Shutdown and Overrides: The purpose of this test is to verify that the UUT has the ability to recognize and properly execute these broadcast mode commands. The pass criterion for each individual test is contained in one of the paragraphs below. The following sequence shall be performed for each test:

- Step 1. A valid legal command shall be sent on the primary bus to the UUT. A CS response shall be verified.
- Step 2. A valid legal command shall be sent on the selected alternate bus to the UUT. A CS response shall be verified.
- Step 3. A valid legal "Broadcast Transmitter Shutdown" mode command shall be sent to the UUT on the primary bus. A NR response shall be verified.
- Step 4. A "Transmit Last Command" mode command shall be sent on the primary bus to the UUT. A BCR response shall be verified, followed by the data word transmitted in Step 3.
- Step 5. A valid legal command shall be sent on the selected alternate bus to the UUT. A NR shall be verified.
- Step 6. A valid legal command shall be sent on the primary bus to the UUT. A CS response shall be verified.
- Step 7. A valid legal broadcast "Override Transmitter Shutdown" mode command shall be sent to the UUT on the selected alternate bus. A NR shall be verified.
- Step 8. A valid legal command shall be sent to the UUT on the selected alternate bus. A NR shall be verified.
- Step 9. A valid legal broadcast "Override Transmitter Shutdown" mode command shall be sent to the UUT on the primary bus. A NR shall be verified.
- Step 10. A "Transmit Last Command" mode command shall be sent on the primary bus to the UUT. A BCR response shall be verified, followed by the data word from Step 9.
- Step 11. A valid legal command shall be sent on the selected alternate bus to the UUT. A CS shall be verified.
- Step 12. A valid legal command shall be sent on the primary bus to the UUT. A CS shall be verified.

5.2.2.4.1.2.4.1 Broadcast Dual Redundant Shutdowns and Overrides: This test shall verify that the UUT recognizes the dual redundant broadcast mode commands to shut down the alternate bus transmitter and to override the shutdown. In a dual redundant system, each bus must be tested as the alternate bus and as the primary bus. A valid legal broadcast "Transmitter Shutdown" mode command shall be used in Step 3. A valid legal broadcast "Override Transmitter Shutdown" mode command shall be used in Steps 7 and 9. The test sequence in 5.2.2.4.1.2.4 shall be used for each case, including verification of the UUT response indicated. The pass criteria shall be that the UUT performs as defined in each step.

5.2.2.4.1.2.4.2 Broadcast Selective Bus Shutdowns and Overrides: This test shall verify that the UUT recognizes the multi-redundant broadcast mode commands to shut down a selected bus transmitter and to override the shutdown. In a multi-redundant system, each bus must be tested as the alternate bus and each as the primary bus. A valid legal broadcast "Selected Transmitter Shutdown" mode code shall be encoded accompanied by the appropriate data word in Step 3 to cause a selective bus transmitter shutdown. A valid legal broadcast "Override Selected Transmitter Shutdown" mode shall be encoded accompanied by the appropriate data word in Steps 7 and 9 to cause an override of the selected bus transmitter shutdown. The test sequence in 5.2.2.4.1.2.4 with the changes given shall be performed using each bus as the primary bus and each as the alternate bus, including verification of the UUT response indicated. The pass criteria shall be that the UUT performs as defined in each step.

5.2.2.4.1.2.5 Broadcast Terminal Flag Bit Inhibit and Override: This test verifies that the UUT recognizes and responds properly to the broadcast mode commands of "Inhibit Terminal Flag Bit" and "Override Inhibit Terminal Flag Bit". Beginning in Step 2 of the test sequence below, the UUT shall be caused to set the terminal flag bit.

- Step 1. A valid legal receive command with at least one data word shall be transmitted to the UUT and a CS response verified.
- Step 2. Introduce a condition that will set the terminal flag in the UUT status response. Send a valid legal receive command with at least one data word to the UUT and verify that the TF bit is set in the returned status word.
- Step 3. A valid legal "Inhibit Terminal Flag" broadcast mode command shall be transmitted to the UUT and a NR verified.
- Step 4. A "Transmit Last Command" mode command shall be sent to the UUT. A BCR response shall be verified, followed by the data word from Step 3.
- Step 5. Repeat Step 1 and verify a CS response.
- Step 6. A valid legal "Override Inhibit Terminal Flag" broadcast mode command shall be transmitted to the UUT and a NR verified.
- Step 7. A "Transmit Last Command" mode command shall be sent to the UUT. A BCR shall be verified.
- Step 8. A valid legal receive command with at least one data word shall be transmitted and a TF verified in the returned status word.
- Step 9. Procedures, as defined for the UUT, shall be performed which reset the TF bit.
- Step 10. Repeat Step 1.

The pass criteria shall be that the UUT performs as defined in each step.

- 5.2.2.4.1.2.6 Broadcast Reset Remote Terminal: This test shall verify that the UUT has the capability to recognize the broadcast mode command to reset itself to a power-up initialized state. For this test, the sequence in 5.2.2.4.1 shall be used with a broadcast "Reset Remote Terminal" mode command in Step 2.

Note: Normal UUT operation may be affected during the Reset execution time. Detailed requirements shall be as defined by the UUT's design specification.

The pass criteria shall be as follows: Step 1 - CS; Step 2 - NR; Step 3 - action and response defined by UUT's design specifications.

- 5.2.2.4.1.3 RT to RT Broadcast Commands: The purpose of this test is to verify that the UUT responds properly to broadcast RT to RT commands with the UUT as the receiving RT. The following test sequence shall be used:

- Step 1. A valid legal receive message shall be sent to the UUT.
- Step 2. A valid legal broadcast RT to RT command pair shall be sent to the UUT.
- Step 3. A "Transmit Last Command" mode command shall be sent to the UUT.
- Step 4. Repeat Step 1.

The pass criteria shall be as follows: Step 1 - CS; Step 2 - NR from the UUT; Step 3 - BCR and the data word contains the receive command of the RT to RT command word pair of Step 2; Step 4 - CS.

- 5.2.2.5 RT to RT Transfers: This test is intended to verify proper UUT operation during RT to RT transfers. For this test, the bus tester shall act as the bus controller and receiving or transmitting remote terminal, as required.

- 5.2.2.5.1 RT to RT Transmit: A valid legal RT to RT command pair shall be sent to the UUT. The transmit command shall be addressed to the UUT. The pass criterion shall be CS.

- 5.2.2.5.2 RT to RT Receive: A valid legal RT to RT command pair followed in 4 to 12  $\mu$ s by a valid status word with the RT address of the transmit command and the proper number of data words shall be sent to the UUT. CS shall be verified.

**5.2.2.5.3 RT to RT Timeout:** The purpose of this test is to verify that the UUT functions properly when operating as the receiving RT in an RT to RT transfer. The UUT must not respond after receiving an RT to RT command pair if the data is not received within 54 to 60  $\mu$ s as shown in Fig. 6. This time is measured from the zero crossing of the parity bit of the receive command to the mid sync zero crossing of the first data word. The following test sequence shall be performed:

- Step 1. A valid legal RT-to-RT command pair followed in 4 to 12  $\mu$ s by a valid status word with the RT address of the transmit command and the proper number of data words shall be sent to the UUT. CS shall be verified.
- Step 2. The time between the command pair and status word of Step 1 shall be increased until the UUT (receiving RT) stops responding and the time "T" as specified in Fig. 6 shall be measured. This time shall be between 54 and 60  $\mu$ s.

The pass criterion for this test shall be the successful completion of Steps 1 and 2.

**5.2.2.6 Illegal Commands:** This test shall be performed if the UUT has the illegal command detection option implemented. If this test is performed, the Word Count (5.2.1.2) and Subaddress (5.2.1.3) tests shall not be performed. The requirements are as follows:

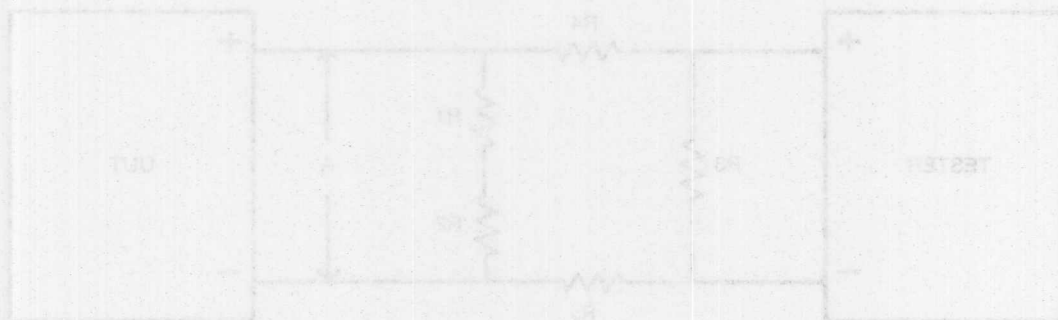
With the UUT terminal address set for a specific code and all commands issued containing that code, perform the following tests:

- Step 1. Send a valid command to the UUT with subaddress 00001, T/R bit 0, and word count 00000, and appropriate number of data words.
- Step 2. Send any valid legal receive command with appropriate data word(s) to the UUT.
- Step 3. Repeat Step 1 for all other combinations of subaddress (except 00000 and 11111), T/R and word counts with appropriate data words following for receive commands.
- Step 4. Repeat Step 2 following each of the commands of Step 3.
- Step 5. Send a valid illegal receive command to the UUT with a parity error in one of the data words.
- Step 6. Send a "Transmit Status" mode command to the UUT. If "Transmit Status" is not implemented, proceed to Step 7.
- Step 7. Repeat Step 2.
- Step 8. Send an illegal command to the UUT with a parity error in the command word.
- Step 9. Send a "Transmit Last Command" mode command to the UUT. If "Transmit Last Command" is not implemented, proceed to Step 10.
- Step 10. Repeat Step 2.
- Step 11. Repeat Step 1 for all combinations of T/R and mode code for subaddresses, 00000 and 11111 (mode commands) with a valid data word contiguously following each receive command.
- Step 12. Repeat Step 2 following each of the commands of Step 3.

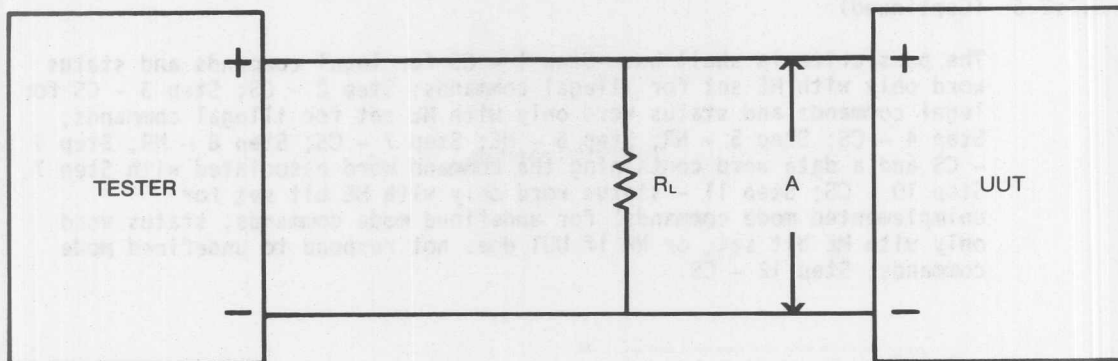


5.2.2.6 (Continued):

The pass criteria shall be: Step 1 - CS for legal commands and status word only with ME set for illegal commands; Step 2 - CS; Step 3 - CS for legal commands and status word only with ME set for illegal commands; Step 4 - CS; Step 5 - NR; Step 6 - ME; Step 7 - CS; Step 8 - NR; Step 9 - CS and a data word containing the command word associated with Step 7; Step 10 - CS; Step 11 - status word only with ME bit set for unimplemented mode commands; for undefined mode commands, status word only with ME bit set, or NR if UUT does not respond to undefined mode commands; Step 12 - CS.



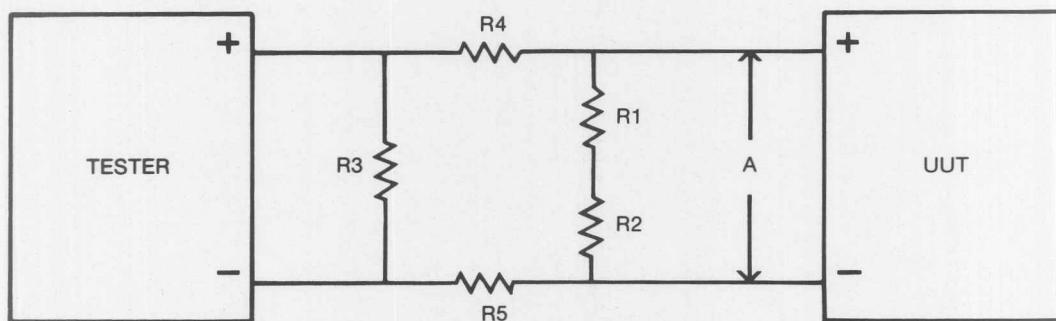
PREPARED BY SUBCOMMITTEE AS-1A, AVIONICS SYSTEMS,  
OF SAE COMMITTEE AS-1, AVIONICS/ARMAMENT INTEGRATION



	DIRECT COUPLED	TRANSFORMER COUPLED
$R_L$	35 ohms $\pm 2\%$	70 ohms $\pm 2\%$

### GENERAL TEST CONFIGURATION

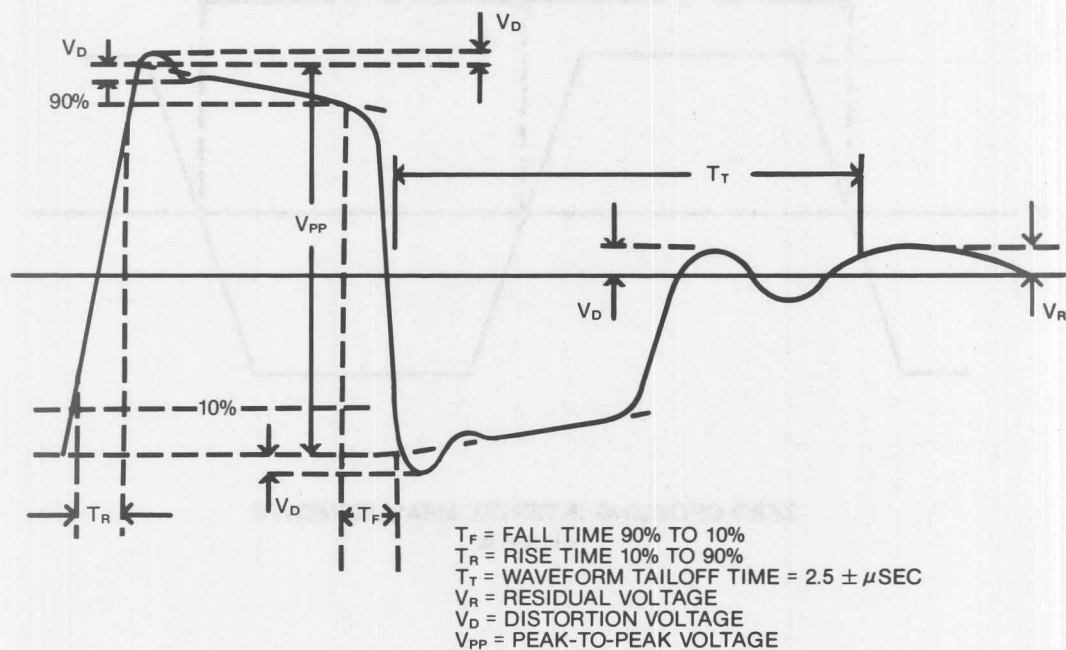
Figure 1.



	DIRECT COUPLED	TRANSFORMER COUPLED
$R_1, R_2$	35 ohms $\pm 2\%$	70 ohms $\pm 2\%$
$R_3, R_4, R_5$	20 100	46.5 93.1

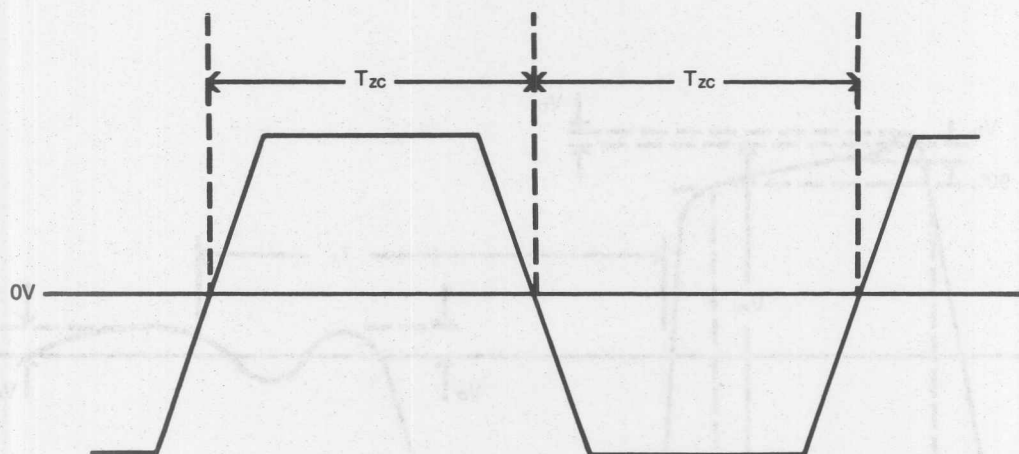
### OPTIONAL TEST CONFIGURATION

Figure 2.



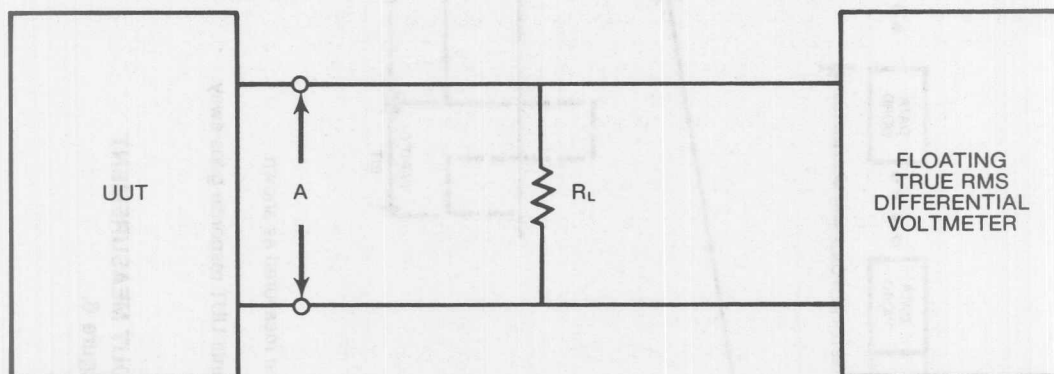
### WAVEFORM MEASUREMENTS

Figure 3.



### ZERO CROSSING INTERVAL MEASUREMENTS

Figure 4.



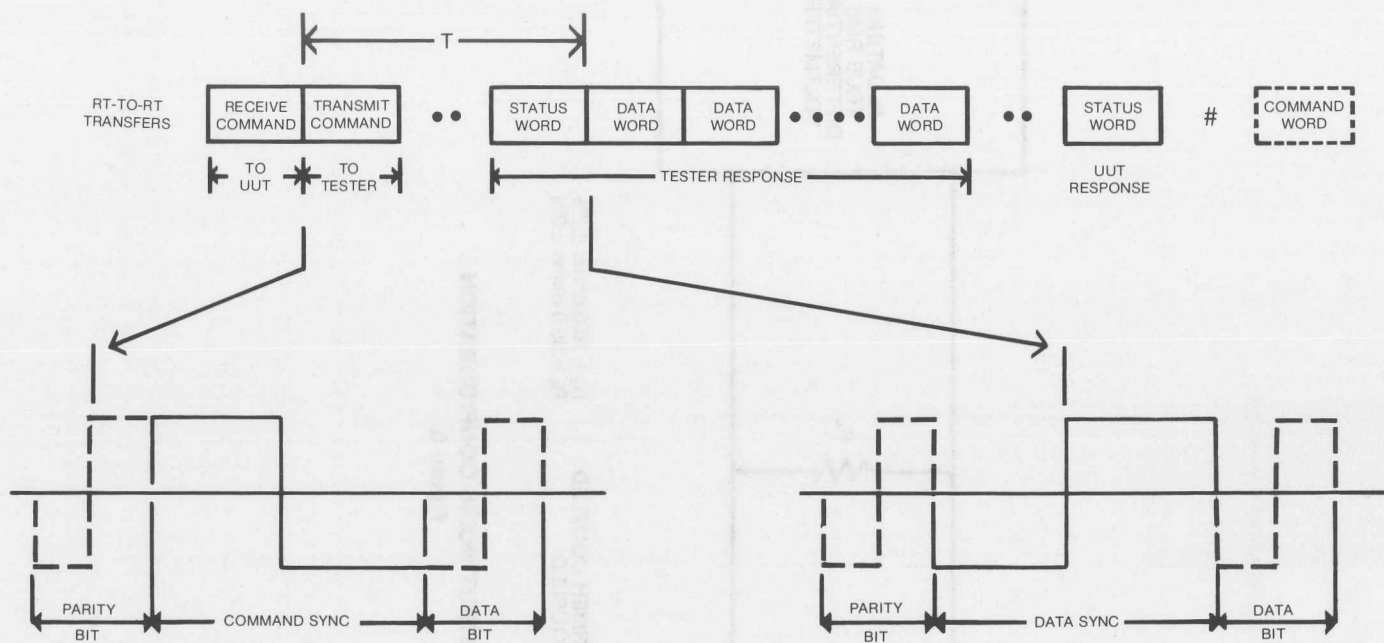
TRANSFORMER COUPLED  
DIRECT COUPLED

$R_L = 70.0 \text{ ohms} \pm 2\%$   
 $R_L = 35.0 \text{ ohms} \pm 2\%$

### OUTPUT NOISE CONFIGURATION

Figure 5.





$T = 54 \text{ to } 60 \mu\text{sec}$  measured as shown.

Delay tester response until UUT response goes away.

**RT — RT TIMEOUT MEASUREMENT**  
**Figure 6.**

APPENDIX A  
TEST PLAN CHANGES FOR MIL-STD-1553B, NOTICE 2 RTs

For remote terminals designed to comply with MIL-STD-1553B Notice 2, the following changes shall be made for tests or pass criteria, or both, in this document:

- A1. Unique Address: The purpose of this test is to verify that the UUT can be assigned a unique address from an external connector on the UUT. The following shall be performed for the UUT:

- Step 1. Send a valid legal command to the UUT.
- Step 2. After externally changing the RT address to simulate a single point address validation failure (for example, parity error on the address lines), repeat Step 1.

Note: Power cycling may be required after externally changing the RT address.

The pass criteria shall be: Step 1 - CS; Step 2 - NR.

- A2. Mode Codes: Compliance with the following paragraphs is no longer optional:

- 5.2.2.2.3 Transmit Status
- 5.2.2.2.6 Transmitter Shutdown and Override
- 5.2.2.2.8 Reset Remote Terminal

- A3. Reset Remote Terminal: The purpose of this test is to verify that the UUT has the ability to recognize the reset terminal mode command and the UUT to complete the reset function within its design time. The following sequence shall be performed once with time  $T \geq T_{dr}$  and again with time  $T < T_{dr}$  (see Step 2) where  $T_{dr}$  is the actual maximum design value for reset time. In no case shall  $T$  be greater than 5 ms.

- Step 1. A reset remote terminal mode command shall be sent to the UUT on one bus.
- Step 2. After time  $T$  from Step 1, as measured per Fig. A-1, a valid legal command shall be sent to the UUT on the same bus.
- Step 3. A valid legal transmitter shutdown mode command shall be sent to the UUT on the same bus.
- Step 4. A valid legal command shall be sent to UUT on the alternate bus.
- Step 5. A reset remote terminal mode command shall be sent to the UUT on the first bus.
- Step 6. After time  $T$ , repeat Step 4.

The pass criteria for each of the above steps shall be as follows: Step 1 - CS; Step 2 - CS (with BUSY bit reset) for time  $T \geq T_{dr}$ , and CS, CS with BUSY bit or NR (whichever is the design requirement) for  $T < T_{dr}$ ; Step 3 - CS; Step 4 - NR; Step 5 - CS; Step 6 - CS.

- A4. Initiate Self-Test: The purpose of this test is to verify that the UUT has the ability to recognize the initiate self-test mode command and complete self test within its design time. The following sequence shall be performed once with time  $T \geq T_{dt}$  and again with the time  $T < T_{dt}$  (see Step 2) where  $T_{dt}$  is the actual maximum design value for self test time. In no case shall  $T$  be greater than 100 ms.

- Step 1. An initiate self-test mode command shall be sent to the UUT on one bus.
- Step 2. After time  $T$  from Step 1, as measured per Fig. A-1, a valid legal command shall be sent to the UUT on the same bus. The test shall be performed with  $T$  set to a value determined by actual design requirement.

The pass criteria for each of the above steps shall be as follows: Step 1 - CS; Step 2 - CS (with BUSY bit reset) for all time  $T \geq$  the time used in Step 2, and CS, CS with BUSY bit set or NR (whichever is the design requirement) for  $T <$  the time used in Step 2.

- A5. Power On Response: The purpose of this test is to verify that the UUT responds correctly to commands after power is applied to the UUT. The following test sequence shall be performed for the UUT using the normal power on sequence for the UUT.

- Step 1. Power the UUT off.
- Step 2. Send valid legal non-broadcast, non-mode commands to the UUT with a maximum intermessage gap of 1 ms.
- Step 3. Power on the UUT and monitor all the UUT responses for 2 s starting from the first transmission of the UUT after power up.

The pass criteria shall be: Step 3 - NR until the first UUT transmission, and CS for the first transmission and all responses thereafter.

- A6. Data Wrap-Around: The purpose of this test is to verify that the UUT properly implements the data wrap-around capability. The following sequence shall be performed with random data patterns for each data word. The messages used shall contain the maximum number of data words that the RT is capable of transmitting or receiving; that is, the maximum word count from the set of all messages defined for that RT.

- Step 1. Send a receive command with the appropriate number of data words to the UUT at the design requirement receive wrap-around subaddress defined for the UUT.
- Step 2. Send a transmit command to the UUT with the design requirement wrap-around subaddress and with the same word count as Step 1.

The pass criteria shall be: Step 1 - CS; Step 2 - CS with each data word having the same bit pattern as the corresponding data word in Step 1.

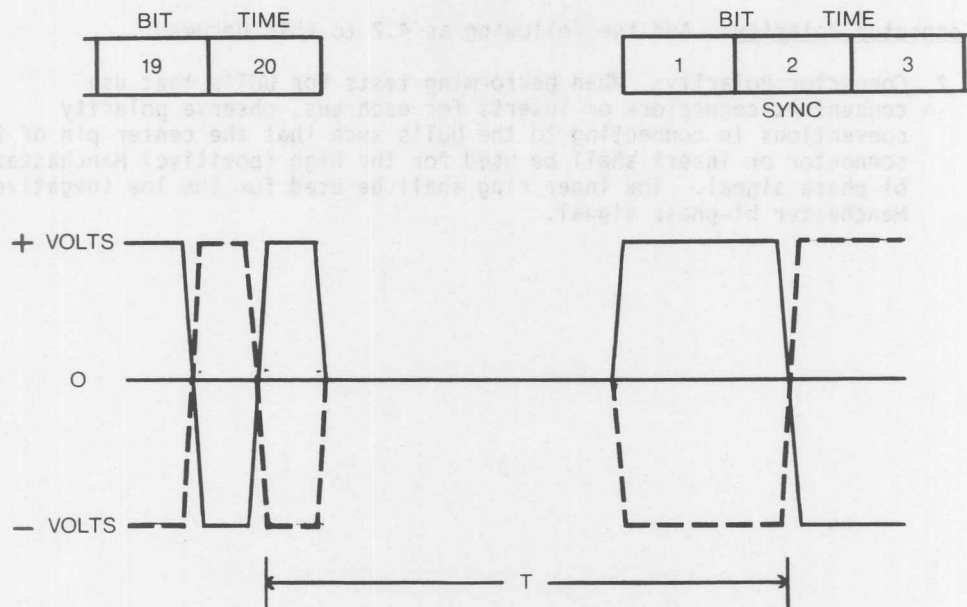
- A7. RT to RT Validation: The following step and pass criteria shall be added to 5.2.2.5.3:

Step 3. Following the completion of Step 2, a Transmit Status mode command shall be issued to the UUT.

The pass criterion for Step 3 is "ME."

- A8. Connector Polarity: Add the following as 4.2 to this document.

4.2 Connector Polarity: When performing tests for UUT's that use concentric connectors or inserts for each bus, observe polarity conventions in connecting to the UUT's such that the center pin of the connector or insert shall be used for the high (positive) Manchester bi-phase signal. The inner ring shall be used for the low (negative) Manchester bi-phase signal.



**GAP TIME MEASUREMENT**  
**Figure A-1**



## VI. RT VALIDATION TEST PLAN

MIL-HDBK-1553  
NOTICE 1  
24 September 1986

**MILITARY HANDBOOK**  
**MULTIPLEX APPLICATION**  
**HANDBOOK**

TO ALL HOLDERS OF MIL-HDBK-1553:

1. THE FOLLOWING PAGES OF MIL-HDBK-1553 ARE PUBLISHED AND SHOULD BE INSERTED IN THE DOCUMENT:

<u>NEW PAGE</u>	<u>DATE</u>	
Appendix A (ii thru viii) (1 thru 67)	24 September 1986	INITIAL PUBLICATION

2. RETAIN THIS NOTICE AND INSERT BEFORE TABLE OF CONTENTS.

3. Holders of MIL-HDBK-1553 will verify that additions indicated above have been entered. This notice page will be retained as a check sheet. This issuance, together with appended pages, is a separate publication. Each notice is to be retained by stocking points until the military standard is completely revised or canceled.

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# APPENDIX A RT VALIDATION TEST PLAN

#### FOREWORD

This section of the handbook provides a sample test plan for MIL-STD-1553B that may serve several different purposes. This section is intended to be noncontractual when the entire MIL-HDBK-1553 is referenced in an equipment specification or SOW. In this case the test plan, as well as the rest of the handbook, provides guidance to both the DOD procuring engineer and the contractor design engineer. This section is intended to be contractual when specifically called out in a specification, SOW, or when required by a DID. If the contractor is required to submit a test plan for his RT to the government, he may remove this section from the handbook and submit it as a portion of his test plan. A better approach would be to simply reference this section. In either case, any and all contractor changes, alterations, or testing deviations to this section shall be separately listed for easy review by government personnel.

MIL-HDBK-1553  
24 September 1986

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## 1.0 SCOPE

**1.1 General.** This validation test plan defines the test requirements for verifying that the design of remote terminals meet the requirements of MIL-STD-1553B, "Digital Time Division Command/Response Multiplex Data Bus." A remote terminal is considered to have failed to meet the above requirements if that remote terminal fails any test or a portion of any test performed according to this test plan. Passing this test plan does not automatically mean that the remote terminal is acceptable for use by the government. The remote terminal must also meet all the requirements of MIL-STD-1553B over all the environmental, EMI, vibration, and application requirements in the sub-system specification.

**1.2 Application.** This general test plan is intended for design verification of remote terminals designed to meet the requirements of MIL-STD-1553B, Notice 2. Appendix A and B provide cross references between this test plan and MIL-STD-1553B. For those remote terminals not required to meet Notice 2, Appendix C and D list the changes in this test plan for MIL-STD-1553B only and MIL-STD-1553B, Notice 1. These requirements shall apply to the terminal under test, when invoked in a specification or statement of work.

## 2.0 APPLICABLE DOCUMENTS

### 2.1 Standards

#### MILITARY

MIL-STD-1553	Digital Time Division Command/Response Multiplex Data Bus
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## 3.0 DEFINITIONS

**3.1 Responses.** The following are definitions of the responses of the RT as used in this test plan. In each case the status word must have the correct terminal address and unused status bits set to zero.

**3.1.1 Broadcast command received (BCR).** The broadcast command received bit (bit time fifteen) is set in status word (and no data words in response to a transmit status mode command or a single data word in response to a transmit last command mode command).

**3.1.2 Busy bit (BUSY).** CS with the busy bit (bit time sixteen) set in the status word, and no data words.

**3.1.3 Clear status (CS).** The status word may have the busy bit and/or service request bit set. All other status code bits in the status word must be zero and the associated message must have the proper word count.

**3.1.4 Dynamic bus acceptance bit (DBA).** CS with the dynamic bus control acceptance bit (bit time eighteen) set in the status word.

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**3.1.5 Service request bit (SRB).** CS with the service request bit (bit time eleven) set in the status word.

**3.1.6 Message error bit (ME).** The message error bit (bit time nine) is set in the status word and no data words (except in response to a transmit last command mode command which requires one data word).

**3.1.7 No response (NR).** The addressed terminal does not produce any response to the command.

**3.1.8 Respond in form.** A terminal is said to "respond in form" if its response to an illegal command as defined in the paragraph titled "Illegal command" of MIL-STD-1553 consists of a response formatted as though it were a legal command.

**3.1.9 Subsystem flag bit (SF).** CS with the subsystem flag bit (bit time seventeen) set in the status word.

**3.1.10 Terminal flag bit (TF).** CS with the terminal flag bit (bit time nineteen) set in the status word.

#### 4.0 GENERAL REQUIREMENTS

**4.1 General test requirements.** The following paragraphs define the configurations, pass/fail criteria, and general procedures for testing remote terminals (RT). Specifically, this document contains the test configurations and procedures for the Electrical Tests (5.1), the Protocol Tests (5.2), and the Noise Rejection Test (5.3) for MIL-STD-1553 remote terminals. The remote terminal under test is referred to as the unit under test (UUT). Proper terminal responses are defined in each test paragraph. If the hardware/software design of the UUT does not permit a test to be performed, then adequate analysis shall be provided in place of the test results to demonstrate that the design meets the requirements of MIL-STD-1553 as stated in the test.

Any condition which causes the UUT to respond other than as called out in MIL-STD-1553, to lock up, or require a power cycle in order to recover for any reason shall automatically cause that UUT to fail the test. All occurrences of responses with the busy bit set in the status word shall be recorded. If the UUT response does not match the pass criteria for a particular test, then the UUT has failed that test.

**4.2 Tests for optional requirements.** All tests for optional requirements defined in 5.2.2 shall be executed if that MIL-STD-1553 option is required by the subsystem specification or interface control document (ICD). Any optional capabilities implemented in the RT should also be tested, if possible. Within the constraints imposed by the hardware/software design, optional capabilities must be tested prior to use by system integrators.



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**4.3 General monitoring requirement.** In addition to the specific tests that follow, certain RT parameters must be continuously monitored throughout all tests. These parameters are:

- a. response time
- b. contiguous data
- c. proper Manchester encoding
- d. proper bit count
- e. odd parity
- f. proper word count
- g. proper terminal address in the status word
- h. reserved status and instrumentation bits in the status word are set to zero
- i. proper sync

The UUT shall have failed the test if at any time during the test any of these parameters fail to meet the requirements of MIL-STD-1553. Record the parameters for all failures.

## 5.0 DETAILED REQUIREMENTS

**5.1 Electrical tests.** Each test paragraph contains the requirements for both transformer and direct coupled stubs. A UUT which provides both transformer and direct coupled stubs must be tested on both stubs. Electrical tests shall be performed on all buses for UUTs with redundant bus configurations.

**5.1.1 Output characteristics.** The following tests are designed to verify that all UUT output characteristics comply with MIL-STD-1553. These tests shall be performed after establishing communications between the test equipment and the UUT. All output electrical tests shall use figure 1A, General Resistor Pad Configuration, with all measurements taken at point "A", unless otherwise noted.

**5.1.1.1 Amplitude.** A valid, legal transmit command shall be sent to the UUT, requesting the maximum number of words that it is capable of sending. The amplitude of the waveform transmitted by the UUT shall be measured, peak-to-peak, as shown on figure 2.

The pass criteria for  $V_{pp}$  for transformer coupled stubs shall be 18.0 V minimum, and 27.0 V maximum. The pass criteria for  $V_{pp}$  for direct coupled stubs shall be 6.0 V minimum and 9.0 V maximum. The maximum and minimum measured parameters,  $V_{pp}$ , shall be recorded.

**5.1.1.2 Risetime/falltime.** A valid, legal transmit command shall be sent to the UUT, requesting at least one data word. The rise and fall time of the UUT waveform shall be measured between the 10% and 90% points of the waveform as shown on figure 2. The measurements shall be taken at both the rising and falling edges of a sync waveform and a data bit waveform. The risetime ( $T_r$ ) and the falltime ( $T_f$ ) shall be recorded.

The pass criteria shall be  $100 \text{ ns} < T_r < 300 \text{ ns}$  and  $100 \text{ ns} < T_f < 300 \text{ ns}$ . The measured parameters,  $T_r$  and  $T_f$ , shall be recorded.

Note: The risetime of the sync waveform shall be measured at the mid-crossing of a data word sync, and the fall time of the sync waveform shall be measured at the mid-crossing of the status word sync.

**5.1.1.3 Zero crossing stability.** A valid legal transmit command shall be sent to the UUT, requesting the UUT to transmit words having zero crossing time intervals of 500 ns, 1000 ns, 1500 ns and 2000 ns. The zero crossing time shall be measured for both the positive ( $T_{zcp}$ ) and the negative ( $T_{zcn}$ ) waveforms as shown on figure 3.

The pass criteria for each case shall be that  $T_{zcp}$  and  $T_{zcn} = 500 + 25 \text{ ns}$ ,  $1000 + 25 \text{ ns}$ ,  $1500 + 25 \text{ ns}$  and  $2000 + 25 \text{ ns}$ . The measured parameters,  $T_{zcp}$  and  $T_{zcn}$  shall be recorded for each case.

**5.1.1.4 Distortion, overshoot and ringing.** A valid legal transmit command shall be sent to the UUT, requesting the UUT to transmit at least one data word. The distortion of the waveform, distortion voltage ( $VD$ ) shall be measured as indicated on figure 2.

Pass criteria shall be  $VD < + 900 \text{ mV}$  peak, line-to-line, for transformer coupled stubs or  $VD < + 300 \text{ mV}$  peak, line-to-line, for direct coupled stubs. The worst measured parameter,  $VD$ , shall be recorded.

**5.1.1.5 Output symmetry.** A valid legal transmit command shall be sent to the UUT requesting the maximum number of data words that the UUT is capable of transmitting. The output symmetry is determined by measuring the waveform tail-off at the end of each message. The maximum residual voltage ( $V_r$ ) shall be measured as shown on figure 2. This test shall be run six times with each data word in the message having the same bit pattern. The six data word bit patterns that shall be used are:

8000(HEX), 7FFF(HEX), 0000(HEX), FFFF(HEX),  
5555(HEX), and AAAA(HEX)

The pass criteria shall be  $V_r < + 250 \text{ mV}$  peak, line-to-line, for transformer coupled stubs and  $V_r < + 90 \text{ mV}$  peak, line-to-line, for direct coupled stubs after time  $T_t$  (the time beginning 2.5  $\mu\text{s}$  after the mid-bit zero crossing of the last parity bit). The measured parameter,  $V_r$ , shall be recorded for each bit pattern.

**5.1.1.6 Output noise.** The test configuration shown on figure 4 shall be used to test the UUT inactive bus output noise levels. The test shall be conducted while the UUT is in the power-on receive state and the power-off state. The output noise ( $V_{rms}$ ) shall be measured at point "A" as shown on figure 4 for both states. Measurements shall be made with an instrument that has a minimum frequency bandwidth of DC to 10 MHz.

The pass criteria shall be  $V_{rms} < 14.0 \text{ mV}$  for transformer coupled stubs and  $V_{rms} < 5.0 \text{ mV}$  for direct coupled stubs. The measured parameter,  $V_{rms}$ , shall be recorded for each case.

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**5.1.1.7 Output isolation.** This test shall be performed only if the UUT is configured with redundant buses. A valid legal transmit command shall be sent to the UUT requesting the maximum number of data words that it is capable of sending. The voltage of the output waveform transmitted by the UUT shall be measured on the active and redundant bus (or buses). Each data bus shall be alternately activated and measurements taken.

The pass criteria shall be that the ratio in dB between the output peak-to-peak voltage on the active bus and the output peak-to-peak voltage on all inactive buses shall be greater than or equal to 45dB (figure 5). The measured parameter, output isolation, expressed as a ratio in dB, shall be recorded for each bus combination.

**5.1.1.8 Power on/off.**

**5.1.1.8.1 Power on/off noise.** A UUT shall limit any spurious differential output during a power-up or power-down sequence. Power shall be applied to the UUT and any outputs from the UUT shall be measured. Power shall be removed from the UUT and any output from the UUT shall be measured. Repeat the test ten times.

The pass criteria shall be:

- a. For transformer coupled stubs any spurious noise pulses produced shall be less than or equal to  $\pm 250$  mV peak, line-to-line.
- b. For direct coupled stubs any spurious noise pulses produced shall be less than or equal to  $\pm 90$  mV peak, line-to-line.

All measured parameters, output noise amplitudes and pulse widths, shall be recorded.

Note: This test shall be performed using the normal on/off power sequence of the UUT.

**5.1.1.8.2 Power on response.** The purpose of this test is to verify that the UUT responds correctly to commands after power is applied to the UUT. Using the normal power on sequence for the UUT, repeat the following test sequence a minimum of ten times.

- Step 1. Power the UUT off.
- Step 2. Send valid, legal, non-broadcast, non-mode commands to the UUT with a maximum intermessage gap of 1 ms.
- Step 3. Power on the UUT and observe all the responses for a minimum of 2 s from the first transmission of the UUT after power on.

The pass criteria shall be: step 3 - NR until the first UUT transmission, and CS for the first transmission and all responses thereafter.

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**5.1.1.9 Terminal response time.** The purpose of this test is to verify that the UUT responds to messages within the proper response time. The test sequence shown below shall be performed.

- Step 1. A valid legal transmit command shall be sent to the UUT and the response time measured.
- Step 2. A valid legal receive command shall be sent to the UUT and the response time measured.
- Step 3. A valid legal RT-to-RT command, with the UUT as the receiving terminal, shall be sent to the UUT and the response time measured.
- Step 4. A valid legal mode command shall be sent to the UUT and the response time measured.

The pass criteria for step 1, step 2, step 3, and step 4 shall be a response time between 4.0 and 12.0 us at point A of figure 1A and measured as shown on figure 7. The command words used and the response times shall be recorded.

**5.1.1.10 Frequency stability.** The purpose of this test is to verify that the transmitter clock in the UUT has the proper accuracy and long term stability and proper short term stability. The transmitter clock measured shall be either the main oscillator output or an appropriate derivative of that clock (e.g., either the 16 MHz oscillator or the 1-2 MHz transmitter shift clock). The test sequence shown below shall be performed on the clock output whose ideal frequency is  $F_i$ .

- Step 1. The short term transmitter clock frequency shall be measured for a single period of the waveform.
- Step 2. Repeat step 1 for at least 10,000 samples and record the minimum ( $F_{smin}$ ) and the maximum ( $F_{smax}$ ) frequency from the samples taken.
- Step 3. The transmitter clock frequency shall be measured with a gate time of 0.1 s and the mean frequency for at least 1,000 samples ( $F_{av}$ ) shall be recorded.

The pass criteria shall be:

Step 1 and step 2 -  $Ss1 = 100(F_{smax} - F_{av})/F_{av} < 0.01$  and  
 $Ss2 = 100(F_{av} - F_{smin})/F_{av} < 0.01$ ;

Step 3 - the magnitude of  $S1 = 100(F_{av} - F_i)/F_i < 0.1$ . Record  $Ss1$ ,  $Ss2$  and  $S1$ .

**5.1.2 Input characteristics.** The input tests are designed to verify that multiplex devices can properly decode bi-phase data. All input electrical tests shall use figure 1A or figure 1B with all measurements taken at point "A," unless otherwise noted. For Air Force applications, all input electrical tests shall use figure 1B, with all measurements taken at point "A" unless otherwise noted.



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#### 5.1.2.1 Input waveform compatibility.

**5.1.2.1.1 Zero crossing distortion.** A legal valid receive message shall be sent to the UUT and the proper response verified. Positive and negative zero crossing distortions equal to  $N$  ns, with respect to the previous zero crossing shall be introduced individually to each zero crossing of each word transmitted to the UUT. The transmitted signal amplitude at point "A" shall be 2.1 Vpp for transformer coupled stubs and 3.0 Vpp for direct coupled stubs. The rise and fall time of the transmitted message (measured at a data bit zero crossing with the prior zero crossing and the next zero crossing at 500 ns intervals from the measured zero crossing) measured at point "A" shall be  $200 \text{ ns} + 20 \text{ ns}$ . Each zero crossing distortion shall be transmitted to the UUT a minimum of 1000 times.

The pass criteria is the transmission of a CS by the UUT for each zero crossing distortion sent with  $N \geq 150$  ns. Positive and negative zero crossing distortions shall then be applied in turn to a single zero crossing and adjusted to determine the values at which the first NR of the UUT occurs; these values shall be recorded.

The fail criteria is the transmission of a NR by the UUT for any zero crossing distortion sent with  $N < 150$  ns.

**5.1.2.1.2 Amplitude variations.** A legal valid receive message shall be sent to the UUT. The transmitter's voltage, as measured at point "A" of figure 1A or figure 1B, shall be decremented from 6.0 Vpp to 0.1 Vpp for transformer coupled stubs and from 9.0 Vpp to 0.1 Vpp for direct coupled stubs in steps no greater than 0.1 Vpp. The rise and fall time of the transmitted message (measured at a data bit zero crossing with the prior zero crossing and the next zero crossing at 500 ns intervals from the measured zero crossing) measured at point "A" shall be  $200 \text{ ns} + 20 \text{ ns}$ . The response of the UUT shall be observed at each step. A minimum of 1000 messages shall be transmitted for each setting.

The pass criteria shall be:

- a. A CS for  $0.86 < V_{pp} < 6.0$  for transformer coupled stubs and  $1.2 < V_{pp} < 9.0$  for direct coupled stubs
- b. A NR for  $V_{pp} < 0.20$  for transformer coupled stubs and  $V_{pp} < 0.28$  for direct coupled stubs

The measured parameter,  $V_{pp}$ , at which NR first occurs shall be recorded.

#### 5.1.2.1.3 Rise and fall time.

**5.1.2.1.3.1 Trapezoidal.** A minimum of 1000 valid receive messages shall be sent to the UUT with a signal amplitude of 2.1 Vpp for the transformer coupled stub and 3.0 Vpp for the direct coupled stub. The rise and fall times of the signal shall be less than or equal to 100 ns.

The pass criteria shall be CS by the UUT for each message.



**5.1.2.1.3.2 Sinusoidal.** A minimum of 1000 valid receive messages shall be sent to the UUT with a signal amplitude of 2.1 Vpp for the transformer coupled stub and 3.0 Vpp for the direct coupled stub. The rise and fall times of the signal shall approximate that of a 1 MHz sinusoidal signal.

The pass criteria shall be CS by the UUT for each message.

**5.1.2.2 Common mode rejection.** The common mode test configuration, figure 6A or figure 6B, shall be used for this test. Legal valid receive messages with the UUT's maximum word count shall be sent to the UUT at a repetition rate which generates a bus activity duty cycle of  $50\% \pm 10\%$  with a common mode voltage injected at point "C", and the UUT response observed. The voltage of the transmitted message measured at point "A" shall be 0.86 Vpp for transformer coupled stubs and 1.2 Vpp for direct coupled stubs. The rise and fall time of the transmitted message (measured at a data bit zero crossing with the prior zero crossing and the next zero crossing at 500 ns intervals from the measured zero crossing) measured at point "A" shall be  $200 \text{ ns} \pm 20 \text{ ns}$ . The following common mode voltage levels shall be applied in turn: +10.0 V.D.C. line-to-ground, -10.0 V.D.C. line-to-ground and  $\pm 10 \text{ Vp}$  line-to-ground sinusoidal signal that is swept through the range of 1 Hz to 2 MHz. Each test condition shall be present for a minimum time period of 90 seconds.

The pass criteria shall be a CS by the UUT for all messages at each setting. If a failure occurs, the measured parameter, common mode signal injected shall be recorded.

**5.1.2.3 Input impedance.** The input impedance of the UUT in a stand alone configuration (i.e., disconnected from figure 1A or 1B) shall be measured with the UUT power on and with the UUT power off. The input impedance,  $Z_{in}$ , shall be measured with a sinusoidal waveform having an amplitude 1.0 VRMS to 2.0 VRMS, at the following frequencies: 75.0 kHz, 100.0 kHz, 250.0 kHz, 500.0 kHz and 1.0 MHz.

The pass criteria shall be  $Z_{in} > 1000$  ohms for transformer coupled stubs and  $Z_{in} > 2000$  ohms for direct coupled stubs. The measured parameter,  $Z_{in}$ , shall be recorded at each frequency.

**5.2 Protocol tests.** All tests in this section shall use the test configuration as shown on figure 1A or figure 1B. The test signal amplitude shall be 3.0 Vpp  $\pm$  0.1 Vpp for direct coupled stubs and 2.1 Vpp  $\pm$  0.1 Vpp for transformer coupled stubs measured at point A. For UUTs having both direct and transformer coupled stubs, the protocol tests need only be performed on one stub type per bus. The protocol tests shall be performed on all buses for UUTs with redundant bus configurations.

**5.2.1 Required remote terminal operation.** The following tests verify required operations of a remote terminal.

**5.2.1.1 Response to command words.** The purpose of this test is to verify that the UUT responds properly to all commands.

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5.2.1.1.1 RT response to command words. All possible command words (65,536 combinations) meeting the criteria of the paragraph on "Word validation" of MIL-STD-1553 shall be sent to the UUT. Mode commands tested in 5.2.1.5, 5.2.2.1 or 5.2.2.4 may be omitted from this test since they are tested separately. Each command word shall be followed by the proper number of contiguous valid data words as defined in the paragraph on "Message formats" of MIL-STD-1553. Refer to table I for undefined mode commands. The associated data may be either random or controlled, depending on the UUT requirements. The following sequence shall be executed for all combinations of command words where the varying command word is sent as step 2.

Step 1. Send a valid legal non-broadcast non-mode command to the UUT

Step 2. Send the variable command word to the UUT.

Step 3. Send a transmit last command mode command to the UUT. (If this mode command is not implemented, then a transmit status mode command shall be used and the data word associated with transmit last command mode command shall be deleted from the pass criteria.)

The pass criteria given below is contingent on the type of command sent. All commands which cause the UUT to fail shall be recorded.

Non-Broadcast Commands (including mode commands):

a. Valid legal commands: step 1- CS; step 2- CS; step 3- CS and the data word contains the command word bit pattern from step 2 (except for transmit last command mode command where the data word contains the command word bit pattern from step 1).

b. Valid illegal commands:

(1) If illegal command detection option is implemented: step 1- CS; step 2- ME with no data words; step 3- ME and the data word contains the command word bit pattern from step 2.

(2) If the illegal command detection option is not implemented: step 1- CS; step 2- CS; step 3- CS and the data word contains the command word bit pattern from step 2.

c. Invalid command (wrong RT address): step 1- CS; step 2- NR; step 3- CS and the data word contains the command word bit pattern from step 1.

d. Undefined mode commands (see table I) (any single set (1), (2), (3), (4), is acceptable):

(1) step 1- CS; step 2- CS; step 3- CS and the data word contains the command word bit pattern addressed to the UUT from step 2.

(2) step 1- CS; step 2- ME; step 3- ME and the data word contains the word bit pattern addressed to the UUT from step 2.

(3) step 1- CS; step 2- NR; step 3- CS and the data word contains the command word bit pattern addressed to the UUT from step 1.

(4) step 1- CS; step 2- NR; step 3- ME and the data word contains the command word bit pattern addressed to the UUT from step 2.

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TABLE I. MIL-STD-1553B undefined mode codes.

T/R	MODE CODE	ASSOCIATED DATA WORD
0	00000	NO
↓	↓	↓
0	01111	NO
0	10000	YES
0	10010	YES
0	10011	YES
1	10001	YES
1	10100	YES
1	10101	YES

Broadcast Commands (including mode commands):

e. If there are any broadcast commands that are considered as valid commands:

(1) Legal commands: step 1- CS; step 2- NR; step 3- BCR and the data word contains the command word bit pattern from step 2.

(2) Illegal commands (if illegal command detection is implemented): step 1- CS; step 2- NR; step 3- BCR and ME and the data word contains the command word bit pattern from step 2.

(3) Illegal commands (if illegal command detection is not implemented): step 1- CS; step 2- NR; step 3- BCR and the data word contains the command word bit pattern from step 2.

f. If there are no broadcast commands that are considered as valid commands: step 1- CS; step 2- NR; step 3- CS and the data word contains the command word bit pattern from step 1.

g. Undefined broadcast mode commands (see table I) (any single set (1), (2), (3) is acceptable):

(1) step 1- CS; step 2- NR; step 3- BCR and the data word contains the command word bit pattern from step 2.

(2) step 1- CS; step 2- NR; step 3- ME and BCR and the data word contains the command word bit pattern from step 2.

(3) step 1- CS; step 2- NR; step 3- CS and the data word contains the command word bit pattern from step 1.

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**5.2.1.1.2 RT-RT response to command words.** All possible command words (65,536 combinations) meeting the criteria of the paragraph on "Word validation" of MIL-STD-1553 shall be sent to the UUT embedded in an RT-RT message format. The test equipment shall supply the required responses for the other RT in order to properly complete the message formats as defined in paragraph on "Message format" of MIL-STD-1553. Refer to table I for undefined mode commands. The associated data may be either random or controlled, depending on the UUT requirements. The intent of this test is for the UUT to be the receiving RT for half of the command combinations (i.e., T/R bit=0) and the transmitting RT for the rest of the command combinations (i.e., T/R bit=1). The following sequence shall be executed for all combinations of command words where the varying command word is sent as step 2.

Step 1. Send a valid legal non-broadcast non-mode command to the UUT.

Step 2. Send the variable command word to the UUT embedded in the RT-RT message format.

Step 3. Send a transmit last command mode command to the UUT. (If this mode command is not implemented, then a transmit status mode command shall be used and the data word associated with transmit last command mode command shall be deleted from the pass criteria.)

The pass criteria shall be as listed in 5.2.1.1.1, except the pass criteria for any RT-RT mode command is as specified in 5.2.1.1.1.d and the pass criteria for any broadcast RT-RT mode command shall be as specified in 5.2.1.1.1.g.

#### **5.2.1.2 Intermessage gap**

**5.2.1.2.1 Minimum time.** The purpose of this test is to verify that the UUT responds properly to messages with a minimum intermessage gap. The message pairs listed in table II shall be sent to the UUT with the minimum intermessage gaps as defined in the paragraph on "Intermessage gap" of MIL-STD-1553. Each message pair shall be sent to the UUT a minimum of 1,000 times. Message pairs which include commands not implemented by the UUT shall be deleted from the test. Each message pair shall have an intermessage gap time (T) of 4.0 us as shown on figure 7.

The pass criteria for this test is CS for each message. All message pairs used shall be recorded and message pairs which cause the UUT to fail the test shall be indicated.

**5.2.1.2.2 Transmission rate.** The purpose of this test is to verify that the UUT responds properly to messages sent for a sustained period with a minimum intermessage gap. The messages listed in each step shall be sent with an intermessage gap of 7 us + 3 us, i.e. a burst of messages with an intermessage gap of 7 us + 3 us between each message as shown on figure 7. Each step shall be performed for a minimum of 30 s.

Step 1. A valid legal transmit message followed by a valid legal transmit message.

Step 2. A valid legal receive message followed by a valid legal receive message.

TABLE II. Intermessage gap messages.

COMMAND TYPES

- A) BC to UUT Transfer (maximum word count)
- B) UUT to BC Transfer (maximum word count)
- C) UUT/RT (maximum word count)
- D) RT/UUT (maximum word count)
- E) Mode Command Without Data Word
- F) Mode Command With Data Word (Transmit)
- G) Mode Command With Data Word (Receive)
- H) BC to UUT Transfer (Broadcast)(maximum word count)
- I) UUT/RT (Broadcast)(maximum word count)
- J) RT/UUT (Broadcast)(maximum word count)
- K) Mode Command Without Data Word (Broadcast)
- L) Mode Command With Data Word (Broadcast)

MESSAGE PAIRS

- 1) A (GAP) A
- 2) B (GAP) A
- 3) C (GAP) A
- 4) D (GAP) A
- 5) E (GAP) A
- 6) F (GAP) A
- 7) G (GAP) A
- 8) H (GAP) A
- 9) I (GAP) A
- 10) J (GAP) A
- 11) K (GAP) A
- 12) L (GAP) A

Note: This table defines the types and combinations of messages to be used in test 5.2.1.2, e.g., pair number 2 specifies a transmit command with the maximum word count to be followed (after the minimum intermessage gap time specified in the paragraph on "Intermessage gap" of MIL-STD-1553) by a receive command with the maximum word count.

UUT/RT: denotes RT to RT transfer with UUT receiving  
RT/UUT: denotes RT to RT transfer with UUT transmitting



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Step 3. A valid legal transmit message followed by a valid legal receive message.

The pass criteria for this test is a CS for each message. All messages which cause the UUT to fail the test shall be recorded.

Note: If the busy bit gets set, then increase the intermessage gap until the busy bit is reset. At this time record the intermessage gap and repeat steps 1 thru 3 until the test is completed without the busy bit getting set.

**5.2.1.3 Error injection.** The purpose of these tests is to examine the UUT's response to specific errors in the message stream. Unless otherwise noted, the following test sequence shall be used for all error injection tests. The error to be encoded in step 2 for a given message is specified in each test paragraph.

Test sequence:

Step 1. A valid legal message shall be sent to the UUT. A mode command shall not be used.

Step 2. A legal message containing the specified error shall be sent to the UUT.

Step 3. A transmit status mode command shall be sent to the UUT.

The pass criteria is defined in each test paragraph. All commands and responses shall be recorded.

**5.2.1.3.1 Parity.** The purpose of these tests is to verify the UUT's capability of detecting parity errors embedded in different words within a message.

**5.2.1.3.1.1 Transmit command word.** This test verifies the ability of the UUT to detect a parity error occurring in a transmit command word. The test sequence as defined in 5.2.1.3 shall be performed with a parity error encoded into a transmit command word for test step 2.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- CS.

**5.2.1.3.1.2 Receive command word.** This test verifies the ability of the UUT to recognize a parity error occurring in a receive command word. The test sequence as defined in 5.2.1.3 shall be performed with a parity error encoded in a receive command word for test step 2.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- CS.

**5.2.1.3.1.3 Receive data words.** This test verifies the ability of the UUT to recognize a parity error occurring in a data word. The test sequence as defined in 5.2.1.3 shall be performed with a parity error encoded in a data word for test step 2. The message shall be a receive command with the maximum number of data words that the UUT is designed to receive. The test sequence must be sent N times, where N equals the number of data words sent.

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Individually each data word must have the parity bit inverted. Only one parity error is allowed per message.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- ME.

**5.2.1.3.2 Word length.** This test verifies the ability of the UUT to recognize an error in word length occurring within a message. The test plan excludes testing of high bit errors on a transmit command and on the last data word of a receive message.

**5.2.1.3.2.1 Transmit command word.** This test verifies the ability of the UUT to recognize transmit command word length errors. The test sequence as defined in 5.2.1.3 shall be performed with the command word shortened as defined below for test step 2.

- a. Transmit command shortened by one bit
- b. Transmit command shortened by two bits

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- CS.

**5.2.1.3.2.2 Receive command word.** This test verifies the ability of the UUT to recognize receive command word length errors. The test sequence as defined in 5.2.1.3 shall be performed with the command word as defined below for test step 2.

- a. Shorten the receive command word by one bit
- b. Shorten the receive command word by two bits
- c. Lengthen the receive command word by two bits
- d. Lengthen the receive command word by three bits

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- CS, or alternately for c and d only, the pass criteria may be: step 1- CS; step 2- NR; step 3- ME.

**5.2.1.3.2.3 Receive data words.** This test verifies the ability of the UUT to recognize data word length errors. The test sequence as defined in 5.2.1.3 shall be performed as defined below for test step 2. The message shall be a receive command with the maximum number of data words that the UUT is designed to receive.

- a. Shorten the data word by one bit
- b. Shorten the data word by two bits
- c. Lengthen the data word by two bits
- d. Lengthen the data word by three bits

The test sequence of 5.2.1.3 shall be performed N times for a and b and N-1 times for c and d, where N equals the number of data words sent. High bit errors shall not be tested in the last data word of a receive message. Only one data word shall be altered at a time. Steps a through d shall be performed for each data word in the message.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- ME.

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**5.2.1.3.3 Bi-phase encoding.** This test verifies the ability of the UUT to recognize bi-phase errors. A bi-phase encoding error is defined to be the lack of a zero crossing in the center of a bit time. A bi-phase error occurs as either a logic high or low for the duration of a bit time. Each bit location, except the sync period, of each word shall have a single bi-phase error encoded into it. Only a single bi-phase error shall be injected for each message.

**5.2.1.3.3.1 Transmit command word.** This test verifies the ability of the UUT to recognize bi-phase encoding errors in transmit command words. The test sequence as defined in 5.2.1.3 shall be performed with a bi-phase encoding error encoded into a transmit command word for test step 2. Each bit location shall have each of the bi-phase errors injected into it. Only one bi-phase error is allowed per command word. A test set involves performing the test sequence 17 times, once for each bit location. A complete test requires two test sets to be performed, one for injecting high bi-phase errors and another for injecting low bi-phase errors.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- CS.

**5.2.1.3.3.2 Receive command word.** This test verifies the ability of the UUT to recognize bi-phase encoding errors in receive command words. The test sequence as defined in 5.2.1.3 shall be performed with a bi-phase error encoded into a receive command word for test step 2. Each bit location must have each of the bi-phase errors injected into it. Only one bi-phase error is allowed per command word. A test set involves performing the test sequence 17 times, once for each bit location. A complete test requires two test sets to be performed one for injecting high bi-phase errors and another for injecting low bi-phase errors.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- CS.

**5.2.1.3.3.3 Receive data words.** This test verifies the ability of the UUT to recognize bi-phase encoding errors in data words. The test sequence as defined in 5.2.1.3 shall be performed with a bi-phase error encoded into each data word in the message for test step 2. The message shall be a receive command and the maximum number of data words that the UUT is designed to receive.

Individually each bit location of each data word shall have a bi-phase error encoded into it. Only one bi-phase error is allowed for each message. A test set involves performing the sequence 17 times. The test set shall be repeated N times, where N equals the number of data words sent. A complete test requires 2\*N test sets to be performed, once for high bi-phase errors and once for low bi-phase errors.

The pass criteria for this test shall be: step 1 CS; step 2- NR; step 3- ME.

**5.2.1.3.4 Sync encoding.** This test verifies the ability of the UUT to recognize sync errors. The sync pattern, as defined for this test, is a waveform with six 0.5 us divisions. The divisions are represented as a 1 or 0 to indicate the polarity of each division on the data bus. A proper command sync is represented as 111000 and a proper data sync is represented as 000111.

**5.2.1.3.4.1 Transmit command word.** This test shall verify that the UUT rejects transmit commands with invalid sync waveforms. The test sequence as defined in 5.2.1.3 shall be performed with a sync error encoded in a transmit command word for test step 2. The test sequence shall be performed for each of the following invalid sync patterns:

111100, 110000, 111001, 011000, 000111

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- CS.

**5.2.1.3.4.2 Receive command word.** This test shall verify that the UUT rejects receive commands with invalid sync waveforms. The test sequence as defined in 5.2.1.3 shall be performed with a sync error encoded in a receive command word for test step 2. The test sequence shall be performed for each of the following invalid sync patterns:

111100, 110000, 111001, 011000, 000111

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- CS.

**5.2.1.3.4.3 Data word.** This test shall verify that the UUT rejects invalid data sync waveforms. Perform the test sequence as defined in 5.2.1.3 with a sync error encoded into each data word for test step 2. The message is a valid receive command word and the maximum number of data words that the UUT is designed to receive. Only one data word per message shall have an invalid sync encoded into it. The test sequence shall be performed N times for each of the following invalid sync patterns: where N equals the maximum number of data words in the message.

000011, 001111, 000110, 100111, 111000

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- ME.

Note: Data words shall not be encoded such that bit times 4 thru 8 match the terminal address of the UUT or be 11111 when the invalid data sync pattern 111000 is being used.

**5.2.1.3.5 Message length.** These tests shall verify that the UUT properly detects an error when an incorrect number of data words are received.

**5.2.1.3.5.1 Transmit command.** This test verifies the ability of the UUT to respond properly if a data word is contiguous to a transmit command word. Perform the test sequence as defined in 5.2.1.3 with a data word contiguously following a transmit command word for test step 2.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- ME.



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**5.2.1.3.5.2 Receive command.** This test shall verify that the UUT recognizes an error in the number of data words that are received. Perform the test sequence as defined in 5.2.1.3 with a data word count error in a receive message for test step 2. This message is a valid legal receive command word with the word count field equal to the maximum number of data words that the UUT is designed to receive but with a different number of data words than specified in the command word. The test sequence shall be performed N+1 times, where N equals the maximum number of data words. The first sequence shall have N+1 data words. The second sequence shall have N-1 data words and each of the remaining sequences shall remove one additional data word until the number of data words equals zero.

The pass criteria shall be: step 1- CS; step 2- NR; step 3- ME.

**5.2.1.3.5.3 Mode command word count error.** This test verifies the ability of the UUT to respond properly when an incorrect number of words are sent with a mode command. Perform the test sequence defined in 5.2.1.3 using a valid receive mode command in step 2 which would normally have an associated data word transmitted with it, but send the number of data words equal to the mode code value used. Repeat the test sequence with the same mode command but with no data word in step 2. Repeat the test sequence using a valid transmit mode command except send a data word contiguously following the command word.

In all three cases the pass criteria shall be: step 1- CS; step 2- NR; step 3-ME.

**5.2.1.3.5.4 RT to RT word count error.** This test verifies the ability of the UUT to respond properly when an incorrect number of words are sent to it as a receiving RT during an RT to RT transfer. Perform the following test sequence.

- Step 1. Send a valid legal RT to RT command pair followed in 4 to 12 us by a valid status word and N data words to the UUT, where N is the number of data words requested in the transmit command.
- Step 2. Send the same RT to RT command pair followed in 4 to 12 us by a valid status word and N-1 data words.
- Step 3. A transmit status mode command shall be sent to the receiving RT.
- Step 4. Repeat steps 1 through 3 using a word count of N+1 in step 2.

The pass criteria in both cases shall be that the receiving RT's status is: step 1- CS; step 2- NR; step 3- ME.



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**5.2.1.3.6 Contiguous data.** This test verifies that the UUT recognizes discontinuous data in a message. Perform the test sequence as defined in 5.2.1.3 with a 4.0 us data word gap error in a receive message for test step 2. The gap is measured as on figure 7. The receive message shall be a receive command with the maximum number of data words that the UUT is designed to receive with a gap between the command word and the first data word or between a data word pair. The test sequence shall be performed N times, where N equals the maximum number of data words. Only one gap time insertion is allowed per message.

The pass criteria for this test shall be: step 1- CS; step 2- NR; step 3- ME.

**5.2.1.3.7 Terminal fail-safe.** The purpose of this test is to verify that the terminal fail-safe timer is properly implemented in the UUT. The UUT is required to contain a hardware implemented timer that will cause the transmitter to shutdown if the UUT transmits a message longer than 800 $\mu$ s. A fail-safe time-out occurring on one bus shall not affect the transmitter on any other bus. The reception of a valid command on the bus on which the time-out has occurred shall enable the transmitter. The test sequence below shall be performed for each bus:

- Step 1. Initiate a condition in the UUT which causes the fail-safe timer to timeout. Measure the duration of the transmission.
- Step 2. Remove the condition initiated in step 1.
- Step 3. Send the UUT a valid legal message over the bus on which the time-out has occurred.

The pass criteria shall be that the timeout in step 1 occurs and the transmitter is shut down allowing the total transmission time to be between 660 us and 800us. The response of the UUT in step 3 shall be CS. Record the measured parameter at which the fail-safe time-out occurs. For test failures, record the test parameters at which the failure occurred.

**5.2.1.4 Superseding commands.** This test verifies that the UUT will not malfunction and responds properly to possible occurrences of superseding commands. The following test sequence shall be used for this test:

- Step 1. A valid legal receive message shall be sent to the UUT with the maximum number of words that the UUT is designed to receive encoded in the word count field.
- Step 2. Before step 1 is completed, a superseding message shall be sent to the UUT.
- Step 3. A transmit status mode command shall be sent to the UUT.

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Record the UUT's response to each step when the test is performed with the following superseding command formats (step 2):

- a. After at least one data word is transmitted in step 1, but before the last data word is transmitted, follow the selected data word with a gap of 4 us (reference figure 7), then a valid legal transmit command requesting the maximum number of data words that the UUT is designed to transmit.
- b. Proceed as in "a" above, except transmit a valid legal transmit status mode command as the superseding command.
- c. After at least one data word is transmitted in step 1, but before the last data word is transmitted, follow the selected data word contiguously with a valid legal transmit command requesting the maximum number of data words that the UUT is designed to transmit.
- d. After the last data word is transmitted in step 1 follow it contiguously with a valid legal transmit command requesting the maximum number of data words that the UUT is designed to transmit.

The pass criteria shall be:

- for a, step 1 - NR, step 2 - CS, step 3 - CS
- for b, step 1 - NR, step 2 - ME, step 3 - ME
- for c, step 1 - NR, step 2 - NR, step 3 - ME
  - or, step 1 - NR, step 2 - CS, step 3 - CS
- for d, step 1 - NR, step 2 - CS, step 3 - CS
  - or, step 1 - NR, step 2 - NR, step 3 - ME

For test failures, record the test parameters for which the failure occurred.

**5.2.1.5 Required mode commands.** The purpose of these tests is to verify that the UUT responds properly to the required mode commands. The tests are not intended to verify the mission aspects stated in the equipment specification. The UUT shall be tested for each required mode code with a subaddress field mode code indicator of all zeros and repeated with a subaddress field of all ones.

The pass criteria is defined in each test paragraph. If any test fails, record the UUT response to that test.

**5.2.1.5.1 Transmit status.** The purpose of this test is to verify that the UUT has the ability to recognize the transmit status mode command and to transmit its last status word. The following sequence shall be performed:

- Step 1. A valid legal message shall be sent to the UUT on the primary bus.
- Step 2. A transmit status mode command shall be sent to the UUT on the primary bus.

- Step 3. A valid legal message shall be sent to the UUT on the alternate bus.
- Step 4. A transmit status mode command shall be sent to the UUT on the alternate bus.
- Step 5. A valid legal receive command with a parity error in a data word shall be sent on the primary bus.
- Step 6. A transmit status mode command shall be sent to the UUT on the alternate bus.
- Step 7. Repeat step 6.
- Step 8. Repeat step 4.
- Step 9. Repeat step 1.
- Step 10. Repeat step 2.
- Step 11. Repeat step 4.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS; step 3- CS; step 4- CS; step 5- NR; step 6- ME; step 7- ME; step 8- ME; step 9- CS; step 10- CS; step 11- CS.

**5.2.1.5.2 Transmitter shutdown and override.** This test shall verify that the UUT recognizes the dual redundant mode code commands to shutdown the alternate bus transmitter and to override the shutdown. In a dual redundant system each bus must be tested as the alternate bus and as the primary bus. A valid legal transmitter shutdown mode command shall be sent to the UUT to cause an alternate bus transmitter shutdown. A valid legal override transmitter shutdown mode command shall be sent to the UUT to cause an override of the transmitter shut-down. The following test sequence shall be used for each case including verification of the UUT response indicated.

- Step 1. A valid legal command shall be sent on the primary bus to the UUT.
- Step 2. A valid legal command shall be sent on the alternate bus to the UUT.
- Step 3. A valid legal transmitter shutdown mode command shall be sent to the UUT on the primary bus.
- Step 4. A valid legal command shall be sent on the alternate bus to the UUT.
- Step 5. A valid legal command shall be sent on the primary bus to the UUT.
- Step 6. A valid legal override transmitter shutdown mode command shall be sent to the UUT on the alternate bus.

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- Step 7. A valid legal command shall be sent to the UUT on the alternate bus.
- Step 8. A valid legal override transmitter shutdown mode command shall be sent to the UUT on the primary bus.
- Step 9. A valid legal command shall be sent on the alternate bus to the UUT.
- Step 10. A valid legal command shall be sent on the primary bus to the UUT.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS; step 3- CS; step 4- NR; step 5- CS; step 6- NR; step 7- NR; step 8- CS; step 9- CS; step 10- CS.

**5.2.1.5.3 Reset remote terminal.** The purpose of this test is to verify that the UUT has the ability to recognize the reset remote terminal mode command. The following sequence shall be performed:

- Step 1. A reset remote terminal mode command shall be sent to the UUT on one bus.
- Step 2. After time T from step 1, as measured per figure 7, a valid legal command shall be sent to the UUT on the same bus.

The time T shall be obtained by repeating step 1 and step 2 while varying the intermessage gap from 100 ms down to 4 us in the following steps: from 100 ms to 6 ms in no greater than 1 ms steps, and from 6 ms to 4 us in no greater than 10 us steps. When the time T is between 5 ms and 100 ms, then in addition to each command sent in step 2, a minimum of one valid legal command shall be sent to the UUT positioned within 4 ms after step 1.

- Step 3. A valid legal transmitter shutdown mode command shall be sent to the UUT on the same bus.
- Step 4. A valid legal command shall be sent to the UUT on the alternate bus.
- Step 5. A reset remote terminal mode command shall be sent to the UUT on the first bus.
- Step 6. After 5 ms repeat step 5.

The minimum time between step 1 and step 2 as measured per figure 7 in which the UUT's response to step 2 is CS (with BUSY bit reset), shall be recorded.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS (with BUSY bit reset) for all time  $T > 5$  ms, and CS or NR for  $T < 5$  ms; step 3- CS; step 4- NR; step 5- CS; step 6- CS.

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**5.2.1.6 Data wrap-around.** The purpose of this test is to verify that the UUT properly implements the data wrap-around capability. The following sequence shall be performed 10,000 times, with random data patterns for each data word in each sequence. The messages used shall contain the maximum number of data words that the RT is capable of transmitting or receiving, i.e., the maximum word count from the set of all messages defined for that RT. Record the number of correct responses and the number of incorrect responses.

- Step 1. Send a receive message to the UUT at subaddress 30 (11110) or the appropriate receive wrap-around subaddress defined for the UUT.
- Step 2. Send a transmit command to the UUT with the appropriate transmit wrap-around subaddress and with the same word count as step 1.

The pass criteria shall be: step 1- CS; step 2- CS with each data word having the same bit pattern as the corresponding data word in step 1.

**5.2.1.7 RT to RT timeout.** The purpose of this test is to verify that the UUT functions properly when operating as the receiving RT in a RT to RT transfer. The UUT must not respond after receiving a RT to RT command pair if the data is not received within 54 us to 60 us as shown on figure 8. This time is measured from the zero crossing of the parity bit of the receive command to the mid sync zero crossing of the first data word. The following test sequence shall be performed:

- Step 1. A valid legal RT to RT command pair followed in 4 us to 12 us by a valid status word with the RT address of the transmit command and the proper number of data words shall be sent to the UUT.
- Step 2. The transmitting RT's status word shall be delayed until the UUT (receiving RT) stops responding and the time "T" as specified in figure 8 shall be measured.
- Step 3. A transmit status mode command shall be sent to the UUT when the time "T" is greater than 60 us.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- "T" shall be between 54 us and 60 us; step 3- ME. All commands, UUT responses and time "T" shall be recorded.



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**5.2.1.8 Bus switching.** This test shall be performed only if the UUT is configured with dual redundant buses. This test verifies that the dual redundant remote terminal properly performs the bus switching requirements of MIL-STD-1553 (para on "Data bus activity"). The requirements are as follows:

- a. If the UUT is receiving or operating on a message on one bus, and another valid, legal command to the UUT occurs on the opposite bus later in time, then the UUT is required to reset and respond appropriately to the later command on the opposite bus.
- b. An invalid command on the alternate bus shall not affect the response of the UUT to commands on the original bus.

Unless otherwise specified, legal messages are used in this test. The interrupting message on the alternate bus shall be swept through the command word, the response time gap, the UUT's status word, and the UUT's data transmission on the first bus. For all tests, record the command words used. The following test sequences shall be performed twice for each interrupting command, once for each redundant bus.

RT transmitting:

- Step 1. Send a valid transmit command to the UUT requesting the maximum number of data words that the UUT is designed to transmit.
- Step 2. Send the interrupting command on the alternate bus beginning 4.0 us after the beginning of the first command.
- Step 3. Send a valid transmit status mode command after the messages on both buses have been completed.
- Step 4. Repeat step 1 through step 3 increasing the time between step 1 and step 2 in no greater than 0.25 us increments until the messages no longer overlap.

Perform the test with the following interrupting messages for step 2.

- a. A valid legal message.
- b. A message with a parity error in the command word.
- c. A valid message with a terminal address different than that of the UUT.

The pass criteria shall be: for a, step 1- truncated message or CS, step 2- CS and step 3- CS; and for b and c, step 1- CS, step 2- NR and step 3- CS. For test failures, record the test parameters at which the failure occurred.

RT receiving:

- Step 1. Send a valid RT to RT message command to the UUT and a second RT with the UUT the receiving terminal with the maximum number of data words that the UUT is designed to receive.
- Step 2. Send the interrupting command on the alternate bus beginning 4.0 us after the beginning of the first command.
- Step 3. Send a valid transmit status mode command after the messages on both buses have been completed.
- Step 4. Repeat step 1 through step 3 varying the time between step 1 and step 2 in no greater than 0.25 us increments until the messages no longer overlap.

Perform the test with the following interrupting messages for step 2.

- a. A valid legal message.
- b. A message with a parity error in the command word.
- c. A valid message with a terminal address different than that of the UUT.

The pass criteria shall be: for a, step 1- NR or CS, step 2 CS and step 3- CS; and for b and c, step 1- CS, step 2- NR and step 3- CS. For test failures, record the test parameters at which the failure occurred.

**5.2.1.9 Unique address.** The purpose of this test is to verify that the UUT can be assigned any unique address from an external connector on the UUT. The following sequence shall be performed for the UUT:

- Step 1. Send a valid, legal command to the UUT.
- Step 2. Repeat step 1 thirty-one times with the same command word except use all other possible bit combinations in the RT address field of the command word.
- Step 3. Repeat step 1 and step 2 after externally changing the RT address for all possible combinations from 00000 thru 11110.
- Step 4. After externally changing the RT address to simulate a single point address validation failure (e.g., parity error on the address lines), repeat step 1 and step 2.

The pass criteria shall be: step 1- CS; step 2- NR for each combination; step 3- same as step 1 and step 2; step 4- NR for each combination.

Note: Power cycling may be required after externally changing the RT address.

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**5.2.2 Optional operation.** This section provides for testing the optional requirements of MIL-STD-1553. If a remote terminal implements any of the options, it shall be tested in accordance with the test herein identified for the option. If the transmit last command mode command is not implemented in the UUT, then the transmit status mode command shall be used.

**5.2.2.1 Optional mode commands.** The purpose of these tests is to verify that the UUT responds properly to implemented mode commands. The tests are not intended to verify the mission aspects stated in the equipment specification. The UUT shall be tested for each mode code implemented with a subaddress field mode code indicator of all zeros and repeated with a subaddress field of all ones.

The pass criteria is defined in each test paragraph. If any test fails, record the UUT response to that test.

**5.2.2.1.1 Dynamic bus control.** The purpose of this test is to verify that the UUT has the ability to recognize the dynamic bus control mode command and to take control of the data bus. A valid legal dynamic bus control mode command shall be sent to the UUT. The UUT shall take control of the data bus when its response is DBA as required in the UUT's design specification.

The pass criteria shall be that the UUT respond with a DBA upon acceptance of bus control or a CS upon rejection of bus control.

**5.2.2.1.2 Synchronize.** The following paragraphs provide the test criteria for the synchronize mode commands.

**5.2.2.1.2.1 Synchronize (without data word).** The purpose of this test is to verify that the UUT has the ability to recognize a synchronization mode command

without using a data word. A valid legal synchronize (without data word) mode command shall be sent to the UUT.

The pass criteria shall be that the UUT respond with CS.

**5.2.2.1.2.2 Synchronize (with data word).** The purpose of this test is to verify that the UUT has the ability to recognize a synchronization mode command which uses a data word. A valid legal synchronize (with data word) mode command shall be sent to the UUT.

The pass criteria shall be that the UUT respond with CS.

**5.2.2.1.3 Initiate self-test.** The purpose of this test is to verify that the UUT has the ability to recognize the initiate self-test mode command. The following sequence shall be performed:

- Step 1. An initiate self-test mode command shall be sent to the UUT on one bus.
- Step 2. After time T from step 1, as measured per figure 7, a valid legal command shall be sent to the UUT on the same bus.

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Step 3. The time T shall be obtained by repeating step 1 and step 2 while varying the intermessage gap from 200 ms down to 4 us in no greater than 1 ms steps. When the time T is between 200 ms and 100 ms then in addition to each command sent in step 2, a minimum of one valid legal command shall be sent to the UUT positioned within 50 ms after step 1.

The minimum time between step 1 and step 2 as measured per figure 7 in which the UUT's response to step 2 is CS (with BUSY bit reset) shall be recorded.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS (with BUSY bit reset) for all time  $T \geq 100$  ms, and CS or NR for  $T < 100$  ms.

**5.2.2.1.4 Transmit BIT word.** The purpose of this test is to verify that the UUT has the ability to recognize this mode command. A valid legal transmit BIT mode command shall be sent to the UUT.

The pass criteria shall be that the UUT respond with CS.

**5.2.2.1.5 Selective transmitter shutdown and override.** This test shall verify that the UUT recognizes the multi-redundant mode code commands to shut down a selected bus transmitter and to override the shutdown. In a multi-redundant system, each bus must be tested as the primary bus with the remaining busses as alternate busses. A valid legal selected transmitter shutdown mode command shall be sent to the UUT accompanied by the appropriate data word to cause a selective bus transmitter shutdown. A valid legal override selected transmitter shutdown mode command shall be sent to the UUT accompanied by the appropriate data word to cause an override of the selected bus transmitter shutdown. The following test sequence shall be performed using each bus as the primary bus and each of the remaining busses in turn as the alternate bus, including verification of the UUT response indicated.

- Step 1. A valid legal command shall be sent on the first bus to the UUT.
- Step 2. A valid legal command shall be sent on the alternate bus to the UUT.
- Step 3. A valid legal selected transmitter shutdown mode command shall be sent to the UUT on the first bus with the data word encoded to shutdown the alternate bus.
- Step 4. A valid legal command shall be sent on the alternate bus to the UUT.
- Step 5. A valid legal command shall be sent on the first bus to the UUT.
- Step 6. A valid legal override selected transmitter shutdown mode command shall be sent to the UUT on the alternate bus with the same data word as sent in step 3.

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- Step 7. A valid legal command shall be sent to the UUT on the alternate bus.
- Step 8. A valid legal override selected transmitter shutdown mode command shall be sent to the UUT on the first bus with the same data word as sent in step 3.
- Step 9. A valid legal command shall be sent on the alternate bus to the UUT.
- Step 10. A valid legal command shall be sent on the first bus to the UUT.
- Step 11. Repeat step 3 except that the data word shall be encoded with a bit pattern that would normally shutdown the first bus if it was sent on the alternate bus.
- Step 12. Repeat step 4.
- Step 13. Repeat step 5.

The data words associated with step 3 and step 11 for each bus shall be recorded.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS; step 3- CS; step 4- NR; step 5- CS; step 6- NR; step 7- NR; step 8- CS; step 9- CS; step 10- CS; step 11- CS; step 12- CS; step 13- CS.

**5.2.2.1.6 Terminal flag bit inhibit and override.** This test verifies that the UUT recognizes and responds properly to the mode code commands of inhibit terminal flag bit and override inhibit terminal flag bit. Beginning in step 2 of the test sequence below, the UUT shall be caused to set the terminal flag bit.

- Step 1. A valid legal receive command with at least one data word shall be sent to the UUT.
- Step 2. Procedures as defined for the UUT, shall be performed that will set the terminal flag in the UUT status response. Send a valid legal receive command with at least one data word to the UUT.
- Step 3. A valid legal inhibit terminal flag mode code command shall be sent to the UUT.
- Step 4. Repeat step 1.
- Step 5. A valid legal override inhibit terminal flag mode code command shall be sent to the UUT.
- Step 6. A valid legal receive command with at least one data word shall be sent to the UUT.



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Step 7. Procedures, as defined for the UUT, shall be performed which resets the TF bit.

Step 8. Repeat step 1.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- TF; step 3- CS or TF; step 4- CS; step 5- CS or TF; step 6- TF; step 8- CS.

**5.2.2.1.7 Transmit vector word.** This test verifies the capability of the UUT to recognize and respond properly to a transmit vector word mode code command.

A valid legal transmit vector word mode code command shall be sent to the UUT.

The pass criteria shall be that the UUT respond with CS.

**5.2.2.1.8 Transmit last command.** This test verifies that the UUT recognizes and responds properly to a transmit last command mode code. The following test sequence shall be used:

- Step 1. A valid legal receive command with at least one data word shall be sent to the UUT.
- Step 2. A valid legal receive command different from that used in step 1 above with at least one data word shall be sent to the UUT and a parity error shall be encoded into the first data word.
- Step 3. A valid transmit last command mode command shall be sent to the UUT.
- Step 4. A valid transmit status mode command shall be sent to the UUT.
- Step 5. A valid legal transmit last command mode command shall be sent to the UUT.
- Step 6. A valid legal transmit last command mode command shall be sent to the UUT.
- Step 7. A valid legal receive command with at least one data word shall be sent to the UUT.
- Step 8. A valid legal transmit last command mode command shall be sent to the UUT.
- Step 9. A valid legal transmit command shall be sent to the UUT.
- Step 10. A valid legal transmit last command mode command shall be sent to the UUT.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- NR; step 3- ME, followed by a data word containing the command word from step 2; step 4- ME; step 5- ME, followed by a data word containing the command word from step 4; step 6- ME, followed by a data word containing the

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command word from step 4; step 7- CS; step 8- CS, followed by a data word containing the command word from step 7; step 9- CS; step 10- CS, followed by a data word containing the command word from step 9.

**5.2.2.2 Status word bits.** The following tests verify that all implemented status code bits are properly used and cleared. Implementation of all status code bits in the status word except the ME bit is optional. In addition to the separate tests, for each of the following status bits: service request, busy, subsystem flag, and terminal flag, provide the analysis as listed below.

- a. What conditions set the status bit in the status word transmitted on the data bus.
- b. What conditions reset the status bit in the status word transmitted on the data bus.
- c. If the condition specified in item a. occurred and disappeared without intervening commands to the UUT, list the cases where the status bit is set and reset in response to a valid, non-mode command to the UUT.
- d. Given that the status bit was set, and the condition which set the bit has gone away, list the cases where the status bit is still set in response to the second valid, non-mode command to the UUT.

The UUT has failed a test sequence if it does not respond as indicated in each of the separate tests below.

**5.2.2.2.1 Service request.** This test verifies that the UUT sets the service request bit as necessary and clears it when appropriate. The UUT shall set bit time eleven of the status word when a condition in the UUT warrants the RT to be serviced. A reset of the bit shall occur as defined by each RT. The following steps shall be performed and the appropriate responses verified:

- Step 1. A valid legal receive command with at least one data word shall be sent to the UUT.
- Step 2. A condition which causes the service request bit to be set shall be introduced into the UUT. A valid legal command that does not service the request shall be sent to the UUT.
- Step 3. A valid legal command that does not service the request shall be sent to the UUT.
- Step 4. Procedures, as defined for the UUT, shall be performed which resets the service request bit.
- Step 5. A valid legal receive command with at least one data word shall be sent to the UUT.

The pass criteria for each of the above steps shall be as follows: step 1- CS, with the service request bit reset; step 2- SRB; step 3- SRB; step 5- CS, with the service request bit reset. All commands and UUT responses shall be recorded.

**5.2.2.2.2 Broadcast command received.** This test verifies that the UUT sets the broadcast command received bit of the status word after receiving a broadcast command. The UUT shall set status bit fifteen to a logic one after receiving the broadcast command. The following test sequence shall be performed using either the transmit last command or transmit status mode code command to verify the bit condition.

Step 1. A valid legal broadcast receive message shall be sent to the UUT.

Step 2. A valid legal transmit last command shall be sent to the UUT.

Step 3. A valid, legal, non-broadcast command shall be sent to the UUT.

Step 4. Repeat step 1.

Step 5. Repeat step 3.

Step 6. A broadcast receive message with a parity error in one of the data words shall be sent to the UUT.

Step 7. A valid legal transmit last command shall be sent to the UUT.

The pass criteria for each of the above step shall be as follows: step 1- NR; step 2- BCR, and the data word contains the bit pattern of the command word in step 1; step 3- CS; step 4- NR; step 5- CS; step 6- NR; step 7- ME and BCR, and the data word contains the bit pattern of the command word in step 6. All commands and UUT responses shall be recorded.

**5.2.2.2.3 Busy.** This test verifies the capability of the UUT to set the busy bit of the status word. Bit time sixteen of the status word shall be set when the UUT is busy. Prior to performing the test sequence below, a condition which sets the busy bit must be activated.

Step 1. A valid legal transmit command shall be sent to the UUT.

Step 2. Procedures, as defined for the UUT, shall be performed which resets the busy bit.

Step 3. A valid legal transmit command shall be sent to the UUT.

The pass criteria for each of the above steps shall be as follows: step 1- BUSY; step 3- CS. All commands and UUT responses shall be recorded.

**5.2.2.2.4 Subsystem flag.** This test verifies the capability of the UUT to set the subsystem flag of the status word. Bit time seventeen of the status word shall be set to a logic one when a subsystem fault has been determined. Prior to performing the test sequence below, a condition which sets the subsystem flag bit must be activated.

Step 1. A valid legal transmit command shall be sent to the UUT.

Step 2. Remove the condition which sets the subsystem flag bit. Cycling power to the UUT shall not be part of these procedures to reset the SF bit.

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Step 3. A valid legal transmit command shall be sent to the UUT.

Step 4. Repeat step 3.

The pass criteria for each of the above steps shall be as follows: step 1- SF; step 3- SF or CS; step 4- CS. All commands and UUT responses shall be recorded.

**5.2.2.2.5 Terminal flag.** This test verifies that the UUT sets the terminal flag bit as necessary and clears it when appropriate. The UUT shall set bit time nineteen of the status word when an occurrence in the UUT causes a terminal fault condition. Prior to performing the test sequence below, a condition which sets the terminal flag bit must be activated.

Step 1. A valid legal receive command with at least one data word shall be sent to the UUT.

Step 2. Remove the condition which sets the terminal flag bit. Cycling power to the UUT shall not be part of this procedure.

Step 3. A valid legal transmit command shall be sent to the UUT.

Step 4. Repeat step 3.

The pass criteria for each of the above steps shall be as follows: step 1 - TF; step 3 - CS or TF; step 4 - CS. All commands and UUT responses shall be recorded.

**5.2.2.3 Illegal command.** This test verifies that the UUT recognizes and responds properly to illegal commands when the illegal command detection option is implemented. The following sequence shall be performed:

Step 1. Send an illegal receive command to the UUT.

Step 2. Send a valid legal transmit command to the UUT.

Step 3. Send an illegal receive command to the UUT with a parity error in one of the data words.

Step 4. Send a transmit status mode command to the UUT.

Step 5. Repeat step 2.

Step 6. Send an illegal command to the UUT with a parity error in the command word.

Step 7. Send a transmit last command mode command to the UUT.

Step 8. Repeat step 1 thru step 7, except step 1 shall be an illegal

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The pass criteria shall be: step 1- status word only with ME bit set; step 2- CS; step 3- NR; step 4- ME; step 5- CS; step 6- NR; step 7- CS and the data word shall represent the command word associated with step 5; step 8 - same as step 1 thru step 7.

**5.2.2.4 Broadcast mode commands.** The purpose of this test is to verify that the UUT responds properly to implemented broadcast mode commands. This test is not intended to verify the mission aspects stated in the equipment specification. The UUT shall be tested for each mode code implemented with a subaddress field mode code indicator of all zeros and repeated with a subaddress field of all ones. Use the following test sequence unless otherwise noted.

Step 1. A valid receive message shall be sent to the UUT.

Step 2. A valid legal broadcast message shall be sent to the UUT.

Step 3. A transmit last command mode command shall be sent to the UUT.

The pass criteria is defined in each test paragraph. If any test fails, record the UUT response to that test.

**5.2.2.4.1 Broadcast synchronize (without data word).** The purpose of this test

is to verify that the UUT has the ability to recognize a broadcast synchronize (without data word) mode command. The test sequence defined in 5.2.2.4 shall be used with a broadcast synchronize (without data word) mode command in step 2.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- NR; step 3- BCR and the data word contains the broadcast command sent in step 2.

**5.2.2.4.2 Broadcast synchronize (with data word).** The purpose of this test is to verify that the UUT has the ability to recognize a broadcast synchronize (with data word) mode command. The test sequence defined in 5.2.2.4 shall be used with a broadcast synchronize (with data word) mode command in step 2.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- NR; step 3- BCR and the data word contains the broadcast command sent in step 2.

**5.2.2.4.3 Broadcast initiate self-test.** The purpose of this test is to verify that the UUT has the ability to recognize the broadcast initiate self-test mode command. The following sequence shall be performed:

Step 1. A broadcast initiate self-test mode command shall be sent to the UUT on one bus.

Step 2. After time "T" from step 1, as measured per figure 7, a valid, legal, non-broadcast, non-mode command shall be sent to the UUT on the same bus.



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Step 3. The time T shall be obtained by repeating step 1 and step 2 while varying the intermessage gap from 200 ms down to 4 us in no greater than 1 ms steps. When the time, T, is between 200 ms and 100 ms then in addition to each command sent in step 2, a minimum of one valid legal command shall be sent to the UUT positioned within 50 ms after step 1.

The minimum time between step 1 and step 2 as measured per figure 7 in which the UUT's response to step 2 is CS (with BUSY bit reset), shall be recorded.

The pass criteria for each of the above steps shall be as follows: step 1- NR; step 2- CS (with BUSY bit reset) for all time  $T \geq 100$  ms, and CS or NR for  $T < 100$  ms.

**5.2.2.4.4 Broadcast transmitter shutdown and override.** The purpose of this test is to verify that the UUT has the ability to recognize and properly execute these broadcast mode commands. The pass criteria for each individual test is contained in the paragraph below. The following sequence shall be performed for each test:

- Step 1. A valid legal command shall be sent on the first bus to the UUT.
- Step 2. A valid legal command shall be sent on the alternate bus to the UUT.
- Step 3. A valid legal broadcast transmitter shutdown mode command shall be sent to the UUT on the first bus.
- Step 4. A transmit last command mode command shall be sent on the first bus to the UUT.
- Step 5. A valid legal command shall be sent on the alternate bus to the UUT.
- Step 6. A valid legal command shall be sent on the first bus to the UUT.
- Step 7. A valid legal broadcast override transmitter shutdown mode command shall be sent to the UUT on the alternate bus.
- Step 8. A valid legal command shall be sent to the UUT on the alternate bus.
- Step 9. A valid legal broadcast override transmitter shutdown mode command shall be sent to the UUT on the first bus.
- Step 10. A transmit last command mode command shall be sent on the first bus to the UUT.
- Step 11. A valid legal command shall be sent on the alternate bus to the UUT.
- Step 12. A valid legal command shall be sent on the first bus to the UUT.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS; step 3- NR; step 4- BCR (and the data word contains the command word of step 3); step 5- NR; step 6- CS; step 7- NR; step 8- NR; step 9- NR; step 10- BCR (and the data word contains the command word of step 9); step 11- CS; step 12- CS.

**5.2.2.4.5 Broadcast selective transmitter shutdown and override.** This test shall verify that the UUT recognizes the multi-redundant broadcast mode code commands to shutdown a selected bus transmitter and to override the shutdown. In a multi-redundant system each bus must be tested as the primary bus with the remaining busses as alternate busses. A valid legal broadcast selected transmitter shutdown mode command shall be sent accompanied by the appropriate data word to cause a selective bus transmitter shutdown. A valid legal broadcast override selected transmitter shutdown mode command shall be sent accompanied by the appropriate data word to cause an override of the selected bus transmitter shutdown. The following test sequence shall be performed using each bus as the primary bus and each of the remaining busses in turn as the alternate bus, including verification of the UUT response indicated.

- Step 1. A valid legal command shall be sent on the first bus to the UUT.
- Step 2. A valid legal command shall be sent on the alternate bus to the UUT.
- Step 3. A valid legal broadcast selected transmitter shutdown mode command shall be sent to the UUT on the first bus with the data word encoded to shutdown the alternate bus.
- Step 4. A transmit last command mode shall be sent on the first bus to the UUT.
- Step 5. A valid legal command shall be sent on the alternate bus to the UUT.
- Step 6. A valid legal command shall be sent on the first bus to the UUT.
- Step 7. A valid legal broadcast override selected transmitter shutdown mode command shall be sent to the UUT on the alternate bus with same data word as sent in step 3.
- Step 8. A valid legal command shall be sent to the UUT on the alternate bus.
- Step 9. A valid legal broadcast override selected transmitter shutdown mode command shall be sent to the UUT on the first bus with the same data word as sent in step 3.
- Step 10. Repeat step 4.
- Step 11. A valid legal command shall be sent on the alternate bus to the UUT.

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Step 12. A valid legal command shall be sent on the first bus to the UUT.

Step 13. Repeat step 3 except that the data word shall be encoded with a bit pattern that would normally shutdown the first bus if it was sent on the alternate bus.

Step 14. Repeat step 4.

Step 15. Repeat step 5.

Step 16. Repeat step 6.

The data words associated with step 3 and step 13 for each bus shall be recorded.

The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- CS; step 3- NR; step 4- BCR (and the data word contains the command word of step 3); step 5- NR; step 6- CS; step 7- NR; step 8- NR; step 9- NR; step 10- BCR (and the data word contains the command word of step 9); step 11- CS; step 12- CS; step 13- NR; step 14- BCR (and the data word contains the command word of step 13); step 15- CS; step 16- CS.

**5.2.2.4.6 Broadcast terminal flag bit inhibit and override.** This test verifies that the UUT recognizes and responds properly to the broadcast mode code commands of inhibit terminal flag bit and override inhibit terminal flag bit. Beginning in step 2 of the test sequence below, the UUT shall be caused to set the terminal flag bit.

Step 1. A valid legal receive command with at least one data word shall be sent to the UUT.

Step 2. Procedures, as defined for the UUT, shall be performed that will set the terminal flag in the UUT status response. Send a valid legal receive command with at least one data word to the UUT.

Step 3. A valid legal inhibit terminal flag broadcast mode code command shall be sent to the UUT.

Step 4. A transmit last command mode command shall be sent to the UUT.

Step 5. Repeat step 1.

Step 6. A valid legal override inhibit terminal flag broadcast mode code command shall be sent to the UUT.

Step 7. A transmit last command mode command shall be sent to the UUT.

Step 8. A valid legal receive command with at least one data word shall be sent to the UUT.

Step 9. Procedures, as defined for the UUT, shall be performed which resets the TF bit.

Step 10. Repeat step 1.

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The pass criteria for each of the above steps shall be as follows: step 1- CS; step 2- TF; step 3- NR; step 4- BCR or (BCR and TF) and in either case the data word contains the command word of step 3; step 5- CS; step 6- NR; step 7- BCR or (BCR and TF) and in either case the data word contains the command word of step 6; step 8- TF; step 10- CS.

**5.2.2.4.7 Broadcast reset remote terminal.** The purpose of this test is to verify that the UUT has the ability to recognize the broadcast mode code command to reset itself to a power up initialized state. The following sequence shall be performed:

- Step 1. A broadcast reset remote terminal mode command shall be sent to the UUT on one bus.
- Step 2. After time T from step 1, as measured per figure 7, a valid legal transmit command shall be sent to the UUT on the same bus.
- Step 3. The time T shall be obtained by repeating step 1 and step 2 while varying the intermessage gap from 100 ms down to 4 us in the following steps: from 100 ms to 6 ms in no greater than 1 ms steps, and from 6 ms to 4 us in no greater than 10 us steps. When the time T is between 5 ms and 100 ms then in addition to each command sent in step 2, a minimum of one valid legal command shall be sent to the UUT positioned within 4 ms after step 1.
- Step 4. A valid legal transmitter shutdown mode command shall be sent to the UUT on the same bus.
- Step 5. A valid legal command shall be sent to the UUT on the alternate bus.
- Step 6. A broadcast reset remote terminal mode command shall be sent to the UUT on the first bus.
- Step 7. After 5 ms repeat step 5.

The minimum time between step 1 and step 2 as measured per figure 7 in which the UUT's response to step 2 is CS (with BUSY bit reset), shall be recorded.

The pass criteria for each of the above steps shall be as follows: step 1- NR; step 2- CS (with BUSY bit reset) for all time T  $\geq$  5 ms and CS or NR for T < 5 ms; step 4- CS; step 5- NR; step 6- NR; step 7- CS.

**5.2.2.4.8 Broadcast dynamic bus control.** The purpose of this test is to insure that the UUT does not take over bus control function in response to a broadcast mode command. The following sequence shall be performed:

- Step 1. A broadcast dynamic bus control mode command shall be sent to the UUT.
- Step 2. A transmit status mode command shall be sent to the UUT.

The pass criteria shall be: step 1- NR; step 2- CS (the BCR bit shall be set, ME bit may be set, but the DBA bit shall not be set).

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**5.2.2.5 Error injection - broadcast messages.** The purpose of this test is to verify the UUT's response to data specific errors in broadcast messages. Unless otherwise noted, the following test sequence shall be used for all error injection tests. The error to be encoded in step 4 for a given message is specified in each test paragraph. The pass criteria is defined in each test paragraph. All responses shall be recorded.

Test sequence:

- Step 1. A valid legal broadcast message shall be sent to the UUT.
- Step 2. A transmit last command mode command shall be sent to the UUT.
- Step 3. A valid legal receive message shall be sent to the UUT.
- Step 4. A broadcast message containing the specified error shall be sent to the UUT.
- Step 5. A transmit last command mode command shall be sent to the UUT.
- Step 6. Repeat Step 3.

**5.2.2.5.1 Parity: bus controller (BC)-RT broadcast.** The purpose of this test is to verify the UUT's capability to detect parity errors embedded in different words within a message.

**5.2.2.5.1.1 Command word error.** This test verifies the ability of the UUT to recognize a parity error in the broadcast command. The test sequence as defined in 5.2.2.5 shall be performed with a parity error encoded in a broadcast command for test step 4.

The pass criteria for this test shall be: step 1- NR; step 2- BCR and the data word contains the command word of step 1; step 3- CS; step 4- NR; step 5- CS and the data word contains the command word of step 3; step 6- CS.

**5.2.2.5.1.2 Data word error.** This test verifies the ability of the UUT to recognize a parity error occurring in a data word. The test sequence as defined in 5.2.2.5 shall be performed with a parity error encoded in a data word for step 4. The message shall be a BC-RT (broadcast) command with the maximum number of data words that the UUT is designed to receive. The test sequence must be executed N times, where N equals the number of data words in the message. Each data word in the message will be transmitted with a parity error. Only one parity error is allowed per message.

The pass criteria for this test shall be: step 1- NR; step 2- BCR and the data word contains the command word of step 01; step 3- CS; step 4- NR; step 5- ME (BCR may be set) and the data word contains the command word of step 4; step 6- CS.



5.2.2.5.2 Message length, BC to RT broadcast. This test shall verify that the UUT recognizes an error in the number of data words that are received. Perform the test sequence as defined in 5.2.2.5 with the data word count error in a BC - RT (broadcast) message for test step 4. The message is a valid legal broadcast command word with the word count field equal to the maximum number of data words that the UUT is designed to receive and a different number of data words than specified in the command word. The test sequence shall be performed N+1 times, where N equals the maximum number of data words.

The first sequence shall have N+1 data words. The second sequence shall have N-1 data words. Other sequences shall remove one additional data word until the number of data words equals zero.

The pass criteria for this test shall be: step 1- NR; step 2- BCR and the data word contains the command word of step 1; step 3- CS; step 4- NR; step 5- ME (BCR may be set) and the data word contains the command word of step 4; step 6- CS.

5.3 Noise rejection test. This test verifies the RT's ability to operate in the presence of noise. The maximum word error rate for a RT is one part in 107. While performing this test, all words received by the UUT shall be in the presence of an additive white Gaussian noise distributed over a bandwidth of 1.0kHz to 4.0 MHz at an RMS amplitude of 140mV for transformer coupled stubs or 200 mV for direct coupled stubs measured at point A of figure 9A or figure 10A. This test shall be conducted with a signal level of 2.1 V peak-to-peak, line-to-line, for transformer coupled stubs or 3.0 V peak-to-peak, line-to-line, for direct coupled stubs measured at point A of figure 9A or figure 10A. The rise and fall time of the transmitted message (measured at a data bit zero crossing with the prior zero crossing and the next zero crossing at 500ns intervals from the measured zero crossing) measured at point "A" shall be 200ns +20ns. Figure 9A and figure 10A depict the configurations for conducting the noise rejection test. Air Force applications shall only use the configuration in figure 10A. Figure 9B and figure 10B depict suggested configurations for the noise rejection test. The noise test shall run continuously with intermessage gaps of > 100us until the total number of all words received by the UUT exceeds the required number for acceptance of the UUT or is less than the required number for rejection of the terminal, as specified in table III. All data words used in the tests shall contain random bit patterns. These bit patterns shall be unique for each data word in a message and shall change randomly from message to message.

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TABLE III. Criteria for acceptance or rejection of  
a terminal for the noise rejection tests.

Total number of words received by the terminal (in multiples of 107)		
<u>NO. OF</u> <u>ERRORS</u>	<u>REJECT</u> <u>(EQUAL OR LESS)</u>	<u>ACCEPT</u> <u>(EQUAL OR MORE)</u>
0	N/A	4.40
1	N/A	5.21
2	N/A	6.02
3	N/A	6.83
4	N/A	7.64
5	N/A	8.45
6	.45	9.27
7	1.26	10.08
8	2.07	10.89
9	2.88	11.70
10	3.69	12.51
11	4.50	13.32
12	5.31	14.13
13	6.12	14.94
14	6.93	15.75
15	7.74	16.56
16	8.55	17.37
17	9.37	18.19
18	10.18	19.00
19	10.99	19.81
20	11.80	20.62
21	12.61	21.43
22	13.42	22.24
23	14.23	23.05
24	15.04	23.86
25	15.85	24.67
26	16.66	25.48
27	17.47	26.29
28	18.29	27.11
29	19.10	27.92
30	19.90	28.73
31	20.72	29.54
32	21.53	30.35
33	22.34	31.16
34	23.15	31.97
35	23.96	32.78
36	24.77	33.00
37	25.58	33.00
38	26.39	33.00
39	27.21	33.00
40	28.02	33.00
41	33.00	N/A

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Do not include information on this page. This page is reserved for the user's information.

Table 1. Summary of the data in the previous table.

ITEM NO.	ITEM NAME	ITEM VALUE
01.01	01.01	01.01
02.01	02.01	02.01
03.01	03.01	03.01
04.01	04.01	04.01
05.01	05.01	05.01
06.01	06.01	06.01
07.01	07.01	07.01
08.01	08.01	08.01
09.01	09.01	09.01
10.01	10.01	10.01
11.01	11.01	11.01
12.01	12.01	12.01
13.01	13.01	13.01
14.01	14.01	14.01
15.01	15.01	15.01
16.01	16.01	16.01
17.01	17.01	17.01
18.01	18.01	18.01
19.01	19.01	19.01
20.01	20.01	20.01
21.01	21.01	21.01
22.01	22.01	22.01
23.01	23.01	23.01
24.01	24.01	24.01
25.01	25.01	25.01
26.01	26.01	26.01
27.01	27.01	27.01
28.01	28.01	28.01
29.01	29.01	29.01
30.01	30.01	30.01
31.01	31.01	31.01
32.01	32.01	32.01
33.01	33.01	33.01
34.01	34.01	34.01
35.01	35.01	35.01
36.01	36.01	36.01
37.01	37.01	37.01
38.01	38.01	38.01
39.01	39.01	39.01
40.01	40.01	40.01
41.01	41.01	41.01
42.01	42.01	42.01
43.01	43.01	43.01
44.01	44.01	44.01
45.01	45.01	45.01
46.01	46.01	46.01
47.01	47.01	47.01
48.01	48.01	48.01
49.01	49.01	49.01
50.01	50.01	50.01
51.01	51.01	51.01
52.01	52.01	52.01
53.01	53.01	53.01
54.01	54.01	54.01
55.01	55.01	55.01
56.01	56.01	56.01
57.01	57.01	57.01
58.01	58.01	58.01
59.01	59.01	59.01
60.01	60.01	60.01
61.01	61.01	61.01
62.01	62.01	62.01
63.01	63.01	63.01
64.01	64.01	64.01
65.01	65.01	65.01
66.01	66.01	66.01
67.01	67.01	67.01
68.01	68.01	68.01
69.01	69.01	69.01
70.01	70.01	70.01
71.01	71.01	71.01
72.01	72.01	72.01
73.01	73.01	73.01
74.01	74.01	74.01
75.01	75.01	75.01
76.01	76.01	76.01
77.01	77.01	77.01
78.01	78.01	78.01
79.01	79.01	79.01
80.01	80.01	80.01
81.01	81.01	81.01
82.01	82.01	82.01
83.01	83.01	83.01
84.01	84.01	84.01
85.01	85.01	85.01
86.01	86.01	86.01
87.01	87.01	87.01
88.01	88.01	88.01
89.01	89.01	89.01
90.01	90.01	90.01
91.01	91.01	91.01
92.01	92.01	92.01
93.01	93.01	93.01
94.01	94.01	94.01
95.01	95.01	95.01
96.01	96.01	96.01
97.01	97.01	97.01
98.01	98.01	98.01
99.01	99.01	99.01
100.01	100.01	100.01

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APPENDIX A

TEST PLAN TO MIL-STD-1553B

CROSS REFERENCE

P = Primary Reference  
R = Related Reference

Test Plan		MIL-STD-1553B
5.0	Detailed requirements	
5.1	Electrical tests	
5.1.1	Output characteristics	
5.1.1.1	Amplitude (Transformer coupled)	4.5.2.1.1.1-P
	(Direct coupled)	4.5.2.2.1.1-P
5.1.1.2	Rise time/fall time (Transformer coupled)	4.5.2.1.1.2-P
	(Direct coupled)	4.5.2.2.1.2-P
5.1.1.3	Zero crossing stability	
	(Transformer coupled)	4.5.2.1.1.2-P
	(Direct coupled)	4.5.2.2.1.2-P
5.1.1.4	Distortion, overshoot & ringing	
	(Transformer coupled)	4.5.2.1.1.2-P
	(Direct coupled)	4.5.2.2.1.2-P
5.1.1.5	Output symmetry (Transformer coupled)	4.5.2.1.1.4-P
	(Direct coupled)	4.5.2.2.1.4-P
5.1.1.6	Output noise (Transformer coupled)	4.5.2.1.1.3-P
	(Direct coupled)	4.5.2.2.1.3-P
5.1.1.7	Output isolation	4.6.1-P
		30.10.6-P
5.1.1.8	Power on/off	
5.1.1.8.1	Power on/off noise (Transformer coupled)	30.10.6-P
	(Direct coupled)	30.10.6-P
5.1.1.8.2	Power on response	30.5.1-P
		3.16-R
5.1.1.9	Terminal response time	4.3.3.8-P
5.1.1.10	Frequency stability	4.3.3.3-P
5.1.2	Input characteristics	
	(Transformer coupled)	4.5.2.1.2-P
	(Direct coupled)	4.5.2.2.2-P
5.1.2.1	Input waveform compatibility	
	(Transformer coupled)	4.5.2.1.2.1-P
	(Direct coupled)	4.5.2.2.2.1-P
5.1.2.1.1	Zero crossing distortion	
	(Transformer coupled)	4.5.2.1.2.1-P
	(Direct coupled)	4.5.2.2.2.1-P
5.1.2.1.2	Amplitude variations	
	(Transformer coupled)	4.5.2.1.2.1-P
	(Direct coupled)	4.5.2.2.2.1-P
5.1.2.1.3	Rise and fall time	4.5.2.1.2.1-P
5.1.2.1.3.1	Trapezoidal	4.5.2.1.2.1-P
5.1.2.1.3.2	Sinusoidal	4.5.2.1.2.1-P

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P = Primary Reference  
R = Related Reference

<u>Test Plan</u>		<u>MIL-STD-1553B</u>
5.1.2.2	Common mode rejection (Transformer coupled)	4.5.2.1.2.2-P
	(Direct coupled)	4.5.2.2.2.2-P
5.1.2.3	Input impedance (Transformer coupled)	4.5.2.1.2.3-P
	(Direct coupled)	4.5.2.2.2.3-P
5.2	Protocol tests	4.4.1.3-P
		4.2.3-R
5.2.1	Required remote terminal operation	4.4.3-P
5.2.1.1	Response to command words	
5.2.1.1.1	RT response to command words	4.3.3.6-P
		4.4.3-P
5.2.1.1.2	RT-RT response to command words	4.3.3.6-P
		4.4.3-P
5.2.1.2	Intermessage gap	
5.2.1.2.1	Minimum time	4.3.3.7-P
5.2.1.2.2	Transmission rate	4.3.3.7-P
		4.3.3.8-R
5.2.1.3	Error injection	4.3.3.5.1.6-R
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.1-R
		4.4.3.3-R
		4.4.3.5-R
		4.4.3.6-R
5.2.1.3.1	Parity	4.3.3.5.1.6-R
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.1-R
		4.4.3.3-P
5.2.1.3.1.1	Transmit command word	4.3.3.5.1.6-R
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.3-P
		4.4.3.5-R
		4.4.3.6-R
5.2.1.3.1.2	Receive command word	4.3.3.5.1.6-R
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.3-P
		4.4.3.5-R
		4.4.3.6-R
5.2.1.3.1.3	Receive data word	4.3.3.5.1.6-R
		4.3.3.5.3.3-P
		4.4.1.1-R
		4.4.3.1-R
		4.4.3.3-P
		4.4.3.5-R
		4.4.3.6-R



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P = Primary Reference  
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Test Plan

MIL-STD-1553B

5.2.1.3.2 Word length

4.3.3.4-R  
4.3.3.5.3.3-P  
4.4.1.1-R  
4.4.3.1-R

5.2.1.3.2.1 Transmit command word

4.4.3.3-P  
4.3.3.4-P

5.2.1.3.2.2 Receive command word

4.3.3.5.3.3-P  
4.4.1.1-R  
4.4.3.3-P  
4.4.3.5-R  
4.3.3.4-P  
4.3.3.5.3.3-P  
4.4.1.1-R  
4.4.3.3-P

5.2.1.3.2.3 Receive data words

4.4.3.6-R  
4.3.3.4-P  
4.3.3.5.3.3-P  
4.4.1.1-R  
4.4.3.6-R

5.2.1.3.3 Bi-phase encoding

4.3.3.2-P  
4.3.3.5.3.3-R  
4.4.1.1-R  
4.4.3.5-R  
4.4.3.6-R

5.2.1.3.3.1 Transmit command word

4.3.3.2-P  
4.3.3.5.3.3-R  
4.4.1.1-R  
4.4.3.3-R

5.2.1.3.3.2 Receive command word

4.3.3.2-P  
4.3.3.5.3.3-R  
4.4.1.1-R

5.2.1.3.3.3 Receive data word

4.4.3.3-R  
4.3.3.2-P  
4.3.3.5.3.3-R  
4.4.1.1-R  
4.4.3.5-R

5.2.1.3.4 Sync encoding

4.4.3.6-R  
4.3.3.5.1.1-P  
4.3.3.5.2.1-P  
4.3.3.5.3.1-P  
4.4.1.1-R  
4.4.3.3-R  
4.4.3.5-R  
4.4.3.6-R

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P = Primary Reference  
R = Related Reference

Test Plan	MIL-STD-1553B
5.2.1.3.4.1 Transmit command word	4.3.3.5.1.1-P 4.4.1.1-R 4.4.3.3-R
5.2.1.3.4.2 Receive command word	4.3.3.5.1.1-P 4.4.1.1-R 4.4.3.3-R
5.2.1.3.4.3 Data word	4.3.3.5.2.1-P 4.4.1.1-R 4.4.3.6-R
5.2.1.3.5 Message length	4.3.3.5.1.5-P
5.2.1.3.5.1 Transmit command	4.3.3.5.1.5-P 4.3.3.6-R 4.3.3.6.2-R
5.2.1.3.5.2 Receive command	4.3.3.5.1.5-P 4.3.3.6-R 4.3.3.6.1-R
5.2.1.3.5.3 Mode command word count error	4.3.3.6-R
5.2.1.3.5.4 RT to RT word count error	4.3.3.5.1.5-P 4.3.3.6-R
5.2.1.3.6 Contiguous data	4.3.3.6.1-P 4.4.1.2-R 4.4.3.5-R
5.2.1.3.7 Terminal fail-safe	4.4.1.3-P
5.2.1.4 Superseding commands	4.4.3.2-P
5.2.1.5 Required mode commands	30.4.2.1-P 4.3.3.5.1.7-P
5.2.1.5.1 Transmit status	4.3.3.5.1.7.3-P
5.2.1.5.2 Transmitter shutdown & override	4.3.3.5.1.7.5-P 4.3.3.5.1.7.6-P
5.2.1.5.3 Reset remote terminal	4.3.3.5.1.7.9-P 30.4.3-P
5.2.1.6 Data wrap-around	30.7-P
5.2.1.7 RT to RT timeout	30.9-P 4.3.3.9-P
5.2.1.8 Bus switching	4.6.3-P 30.2-R
5.2.1.9 Unique address	30.3-P 4.3.3.5.1.2-R
5.2.2 Optional operation	
5.2.2.1 Optional mode commands	4.3.3.5.1.7-P
5.2.2.1.1 Dynamic bus control	4.3.3.5.1.7.1-P 4.3.3.5.3.10-R
5.2.2.1.2 Synchronize	
5.2.2.1.2.1 Synchronize without data word	4.3.3.5.1.7.2-P
5.2.2.1.2.2 Synchronize with data word	4.3.3.5.1.7.12-P
5.2.2.1.3 Initiate self-test	4.3.3.5.1.7.4-P 30.4.4-P

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P = Primary Reference  
R = Related Reference

<u>Test Plan</u>		<u>MIL-STD-1553B</u>
5.2.2.1.4	Transmit bit word	4.3.3.5.1.7.14-P
5.2.2.1.5	Selective transmitter shutdown & override	4.3.3.5.1.7.15-P
		4.3.3.5.1.7.16-P
5.2.2.1.6	Terminal flag bit inhibit and override	4.3.3.5.1.7.7-P
		4.3.3.5.1.7.8-P
5.2.2.1.7	Transmit vector word	4.3.3.5.1.7.11-P
5.2.2.1.8	Transmit last command	4.3.3.5.1.7.13-P
5.2.2.2	Status word bits	4.3.3.5.3-P
		30.5.2-P
5.2.2.2.1	Service request	4.3.3.5.3.5-P
5.2.2.2.2	Broadcast command received	4.3.3.5.3.7-P
5.2.2.2.3	Busy	4.3.3.5.3.8-P
		30.5.3-P
5.2.2.2.4	Subsystem flag	4.3.3.5.3.9-P
5.2.2.2.5	Terminal flag	4.3.3.5.3.11-P
5.2.2.3	Illegal command	4.4.3.4-P
5.2.2.4	Broadcast mode commands	4.3.3.6.7.3-P
		4.3.3.6.7.4-P
5.2.2.4.1	Broadcast synchronize (without data word)	4.3.3.5.1.7.2-P
		4.3.3.6.7.3-P
5.2.2.4.2	Broadcast synchronize (with data word)	4.3.3.5.1.7.12-P
		4.3.3.6.7.4-P
5.2.2.4.3	Broadcast initiate self-test	4.3.3.5.1.7.4-P
		4.3.3.6.7.3-P
5.2.2.4.4	Broadcast transmitter shutdown and override	4.3.3.5.1.7.5-P
		4.3.3.5.1.7.6-P
		4.3.3.6.7.3-P
5.2.2.4.5	Broadcast selective transmitter shutdown and override	4.3.3.5.1.7.15-P
		4.3.3.5.1.7.16-P
		4.3.3.6.7.4-P
5.2.2.4.6	Broadcast terminal flag bit inhibit and override	4.3.3.5.1.7.7-P
		4.3.3.5.1.7.8-P
		4.3.3.6.7.3-P
5.2.2.4.7	Broadcast reset remote terminal	4.3.3.5.1.7.9-P
		4.3.3.6.7.3-P
5.2.2.4.8	Broadcast dynamic bus control	4.3.3.5.1.7.1-P

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P = Primary Reference  
R = Related Reference

<u>Test Plan</u>		<u>MIL-STD-1553B</u>
5.2.2.5	Error injection - broadcast messages	4.3.3.5.3.3-P 4.3.3.5.3.7-R 4.4.1.1-R 4.4.3.1-R 4.4.3.3-R 4.4.3.5-R 4.4.3.6-R
5.2.2.5.1	Parity: BC-RT broadcast	4.3.3.5.1.6-P 4.3.3.6.7.1-R
5.2.2.5.2	Command word error	4.3.3.5.1.6-P 4.3.3.5.1-R
5.2.2.5.3	Data word error	4.3.3.5.1.6-P 4.3.3.5.2-R
5.2.2.5.4	Message length, BC to RT broadcast	4.3.3.6.7.1-P 4.4.3.6-P
5.3	Noise rejection (Transformer coupled) (Direct coupled)	4.3.3.5.3.7-R 4.5.2.1.2.4-P 4.5.2.2.2.4-P

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APPENDIX B  
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APPENDIX B

MIL-STD-1553B TO TEST PLAN

CROSS REFERENCE

<u>MIL-STD-1553B</u>		<u>Test Plan</u>
4.	General requirements	
4.1	Test & operating requirements	none
4.2	Data bus operation	5.2
4.3	Characteristics	
4.3.1	Data form	none
4.3.2	Bit priority	none
4.3.3	Transmission method	
4.3.3.1	Modulation	none
4.3.3.2	Data code	5.2.1.3.3
4.3.3.3	Transmission bit rate	5.1.1.10
4.3.3.4	Word size	5.2.1.3.2
4.3.3.5	Word formats - command	5.2.1.1
	- data	none
	- status	5.2.2.2
4.3.3.5.1	Command word	5.2.1.1
4.3.3.5.1.1	Sync	5.2.1.3.4.1
4.3.3.5.1.2	Remote terminal address (not 11111)	5.2.1.1
	( 11111)	5.2.1.1
4.3.3.5.1.3	Transmit/receive	5.2
4.3.3.5.1.4	Subaddress/mode - subaddress	5.2.1.1
	- mode	5.2.2.1
4.3.3.5.1.5	Data word count/mode code - word count	5.2.1.3.5
	- mode code	5.2.2.1
4.3.3.5.1.6	Parity	5.2.1.3.1
4.3.3.5.1.7	Optional mode control	5.2.2.1
4.3.3.5.1.7.1	Dynamic bus control	5.2.2.1.1
4.3.3.5.1.7.2	Synchronize (without data word)	5.2.2.1.2.1
4.3.3.5.1.7.3	Transmit status word	5.2.1.5.1
4.3.3.5.1.7.4	Initiate self test	5.2.2.1.3
4.3.3.5.1.7.5	Transmitter shutdown	5.2.1.5.2
4.3.3.5.1.7.6	Override transmitter shutdown	5.2.1.5.2
4.3.3.5.1.7.7	Inhibit T/F bit	5.2.2.1.6
4.3.3.5.1.7.8	Override inhibit T/F flag	5.2.2.1.6
4.3.3.5.1.7.9	Reset remote terminal	5.2.1.5.3
4.3.3.5.1.7.10	Reserved mode codes (01001-01111)	5.2.1.1
4.3.3.5.1.7.11	Transmit vector word	5.2.2.1.7
4.3.3.5.1.7.12	Synchronize (with data word)	5.2.2.1.2.2
4.3.3.5.1.7.13	Transmit last command word	5.2.2.1.8
4.3.3.5.1.7.14	Transmit built-in-test (BIT) word	5.2.2.1.4
4.3.3.5.1.7.15	Selected transmitter shutdown	5.2.2.1.5
4.3.3.5.1.7.16	Override selected transmitter shutdown	5.2.2.1.5
4.3.3.5.1.7.17	Reserved mode codes (10110 to 11111)	5.2.1.1



<u>MIL-STD-1553B</u>		<u>Test Plan</u>
4.3.3.5.2	Data word	
4.3.3.5.2.1	Sync	5.2.1.3.4.2
4.3.3.5.2.2	Data	none
4.3.3.5.2.3	Parity	4.1
4.3.3.5.3	Status word	5.2.2.2
4.3.3.5.3.1	Sync	4.2
4.3.3.5.3.2	RT address	4.2
4.3.3.5.3.3	Message error bit	5.2.1.3
4.3.3.5.3.4	Instrumentation bit	4.2
4.3.3.5.3.5	Service request bit	5.2.2.2.1
4.3.3.5.3.6	Reserved status bits	4.2
4.3.3.5.3.7	Broadcast command received bit	5.2.2.2.2
4.3.3.5.3.8	Busy bit	5.2.2.2.3
4.3.3.5.3.9	Subsystem flag bit	5.2.2.2.4
4.3.3.5.3.10	Dynamic bus control acceptance bit	5.2.2.1.1
4.3.3.5.3.11	Terminal flag bit	5.2.2.2.5
4.3.3.5.3.12	Parity bit	4.2
4.3.3.5.4	Status word reset	5.2.2.2
4.3.3.6	Message formats	n/a
4.3.3.6.1	BC to RT transfers	5.2.1.1.1
4.3.3.6.2	RT to BC transfers	5.2.1.1.1
4.3.3.6.3	RT to RT transfers	5.2.1.1.2
4.3.3.6.4	Mode command w/o data word	5.2.2.1
4.3.3.6.5	Mode command with data word (transmit)	5.2.2.1
4.3.3.6.6	Mode command data word (receive)	5.2.2.1
4.3.3.6.7	Optional broadcast command	5.2.1.1
4.3.3.6.7.1	BC to RT transfer (broadcast)	5.2.1.1
4.3.3.6.7.2	RT to RT transfer (broadcast)	5.2.1.1
4.3.3.6.7.3	Mode commands w/o data word (broadcast)	5.2.2.4
4.3.3.6.7.4	Mode commands with data word (broadcast)	5.2.2.4
4.3.3.7	Intermessage gap	5.2.1.2
4.3.3.8	Response time	4.2
		5.1.1.9
4.3.3.9	Minimum no-response time-out	5.2.1.7
4.4	Terminal operation	
4.4.1	Common operation	
4.4.1.1	Word validation	5.2.1.3
4.4.1.2	Transmission continuity	5.2.1.3.6
4.4.1.3	Terminal fail-safe	5.2.1.3.7
4.4.2	Bus controller operation	n/a
4.4.3	Remote terminal	5.2
4.4.3.1	Operation	5.2.1.1
4.4.3.2	Superseding valid commands	5.2.1.4
4.4.3.3	Invalid commands	5.2.1.3
4.4.3.4	Illegal commands	5.2.2.3
4.4.3.5	Valid data reception	5.2.1.3
4.4.3.6	Invalid data reception	5.2.1.3
4.4.4	Bus monitor operation	n/a

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APPENDIX B  
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MIL-STD-1553B		Test Plan
4.5	Hardware characteristics	
4.5.1	Data bus characteristics	
4.5.1.1	Cable	n/a
4.5.1.2	Characteristics impedance	n/a
4.5.1.3	Cable attenuation	n/a
4.5.1.4	Cable termination	n/a
4.5.1.5	Cable stub requirements	n/a
4.5.1.5.1	Transformer coupled stubs	n/a
4.5.1.5.1.1	Coupling transformer	n/a
4.5.1.5.1.1.1	Transformer input impedance	n/a
4.5.1.5.1.1.2	Transformer waveform integrity	n/a
4.5.1.5.1.1.3	Transformer common mode rejection	n/a
4.5.1.5.1.2	Fault isolation	n/a
4.5.1.5.1.3	Cable coupling	n/a
4.5.1.5.1.4	Stub voltage requirements	n/a
4.5.1.5.2	Direct coupled stubs	n/a
4.5.1.5.2.1	Fault isolation	n/a
4.5.1.5.2.2	Cable coupling	n/a
4.5.1.5.2.3	Stub voltage requirements	n/a
4.5.1.5.3	Wiring & cabling for EMC	n/a
4.5.2	Terminal characteristics	5.1
4.5.2.1	Terminals with transformer coupled stubs	5.1
4.5.2.1.1	Terminal output characteristics	5.1.1
4.5.2.1.1.1	Output levels	5.1.1.1
4.5.2.1.1.2	Output waveform	5.1.1.2
		5.1.1.3
		5.1.1.4
4.5.2.1.1.3	Output noise	5.1.1.6
		5.1.1.8
4.5.2.1.1.4	Output symmetry	5.1.1.5
4.5.2.1.2	Terminal input characteristics	5.1.2
4.5.2.1.2.1	Input waveform compatibility	5.1.2.1
4.5.2.1.2.2	Common mode rejection	5.1.2.2
4.5.2.1.2.3	Input impedance	5.1.2.3
4.5.2.1.2.4	Noise rejection	5.3
4.5.2.2	Terminals with direct coupled stubs	5.1
4.5.2.2.1	Terminal output characteristics	5.1.1
4.5.2.2.1.1	Output levels	5.1.1.1
4.5.2.2.1.2	Output waveform	5.1.1.2
		5.1.1.3
		5.1.1.4
4.5.2.2.1.3	Output noise	5.1.1.6
		5.1.1.8
4.5.2.2.1.4	Output symmetry	5.1.1.5
4.5.2.2.2	Terminal input characteristics	5.1.2
4.5.2.2.2.1	Input waveform compatibility	5.1.2.1
4.5.2.2.2.2	Common mode rejection	5.1.2.2
4.5.2.2.2.3	Input impedance	5.1.2.3
4.5.2.2.2.4	Noise rejection	5.3

MIL-HDBK-1553  
APPENDIX B  
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<u>MIL-STD-1553B</u>		<u>Test Plan</u>
4.6	Redundant data bus requirements	5.2.1.8
4.6.1	Electrical isolation	5.1.1.7
4.6.2	Single event failures	n/a
4.6.3	Dual standby redundant data bus	5.2.1.8
4.6.3.1	Data bus activity	5.2.1.8
4.6.3.2	Superseding valid commands	5.2.1.8
30.	GENERAL REQUIREMENTS	n/a
30.1	Option selection	n/a
30.2	Application	n/a
30.3	Unique address	5.2.1.9
30.4	Mode codes	n/a
30.4.1	Subaddress/mode	5.2.1.5
30.4.2	Required mode codes	n/a
30.4.2.1	Remote terminal required mode codes	5.2.1.5
30.4.2.2	Bus controller required mode codes	n/a
30.4.3	Reset remote terminal	5.2.1.5.3
30.4.4	Initiate RT self-test	5.2.2.1.3
30.5	Status word bits	n/a
30.5.1	Information content	5.1.1.8.2
30.5.2	Status bit requirements	5.2.2.2
30.5.3	Busy bit	5.2.2.2.3
30.6	Broadcast	5.2.1.1
30.7	Data wrap-around	5.2.1.6
30.8	Message formats	n/a
30.9	RT to RT validation	5.2.1.7
30.10	Electrical characteristics	n/a
30.10.1	Cable shielding	n/a
30.10.2	Shielding	n/a
30.10.3	Connector polarity	n/a
30.10.4	Characteristic impedance	n/a
30.10.5	Stub coupling	n/a
30.10.6	Power on/off noise	5.1.1.8

MIL-HDBK-1553  
APPENDIX C  
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## APPENDIX C

### TEST PLAN CHANGES FOR MIL-STD-1553B ONLY RT's

For remote terminals designed to only comply with MIL-STD-1553B, the following changes shall be made for the pass criteria in this document.

1. The following paragraphs are optional and are subject to the same requirements as 5.2.2.

5.2.1.5	Required mode commands
5.2.1.5.1	Transmit status
5.2.1.5.2	Transmitter shutdown and override
5.2.1.5.3	Reset remote terminal
5.2.1.6	Data wrap-around
5.2.1.7	RT to RT timeout
5.2.1.8	Bus switching
5.2.1.9	Unique address

2. For the following paragraphs, the pass criteria for step 2 shall be changed to delete the words "(with BUSY bit reset)."

5.2.2.1.3	Initiate self-test
5.2.1.5.3	Reset remote terminal
5.2.2.4.3	Broadcast initiate self-test
5.2.2.4.7	Broadcast reset remote terminal

3. For 5.1.1.8.1 Power on/off noise, the pass criteria shall not be defined in this document.

4. For the following paragraphs, the requirement to implement both mode code indicators of all zeros and all ones is optional and subject to the same requirements as 5.2.2. The RT must meet the pass criteria for either all zeros or all ones, but is not required to meet both.

5.2.1.5	Required mode commands
5.2.2.1	Optional mode commands
5.2.2.4	Broadcast mode commands

5. The following note shall be added to the end of 5.2.1.3.

Note: If transmit status mode command is not implemented, then transmit last command mode command shall be used. If neither mode command is implemented, then step 3 shall be deleted.

APPENDIX C

THE MAIN C

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For certain functions described in only one of the two documents, the following changes shall be made to the code in the document:

1. The following paragraphs are deleted and are subject to the same changes as 2.1.1:

2.1.1.1	General code changes
2.1.1.2	General code changes
2.1.1.3	General code changes
2.1.1.4	General code changes
2.1.1.5	General code changes
2.1.1.6	General code changes
2.1.1.7	General code changes
2.1.1.8	General code changes
2.1.1.9	General code changes

2. For the following paragraphs, the code shall be changed to delete the code in the following paragraphs:

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2.1.1.10	General code changes
2.1.1.11	General code changes
2.1.1.12	General code changes
2.1.1.13	General code changes
2.1.1.14	General code changes

3. For 2.1.1.15, the code shall be changed to delete the code in the following paragraphs:

4. For the following paragraphs, the code shall be changed to delete the code in the following paragraphs:

2.1.1.15	General code changes
2.1.1.16	General code changes
2.1.1.17	General code changes

5. The following code shall be added to the end of 2.1.1.1:

When it is determined that the code is not required, the code shall be deleted. If the code is required, the code shall be added. The code shall be added to the code in the following paragraphs:



MIL-HDBK-1553  
APPENDIX D  
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## APPENDIX D

### TEST PLAN CHANGES FOR MIL-STD-1553B, NOTICE 1 RTs

For remote terminals designed to comply with MIL-STD-1553B, Notice 1, the following changes shall be made for the pass criteria in this document.

1. The following paragraphs are optional, and are subject to the same requirements as 5.2.2.

5.2.1.5	Required mode commands
5.2.1.5.1	Transmit status
5.2.1.5.2	Transmitter shutdown and override
5.2.1.5.3	Reset remote terminal
5.2.1.6	Data wrap-around
5.2.1.7	RT to RT timeout
5.2.1.9	Unique address

2. For the following paragraphs, the pass criteria for step 2 shall be changed to delete the words "(with BUSY bit reset)."

5.2.2.1.3	Initiate self-test
5.2.1.5.3	Reset remote terminal
5.2.2.4.3	Broadcast initiate self-test
5.2.2.4.7	Broadcast reset remote terminal

3. For 5.1.1.8, the pass criteria shall not be defined in this document.

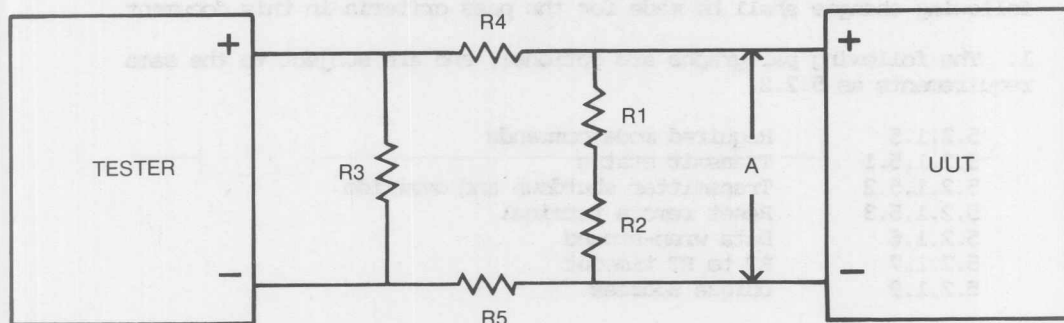
4. For the following paragraphs the requirement to implement mode code indicator of all ones is optional and subject to the same requirements as 5.2.2.

5.2.1.5	Required mode commands
5.2.2.1	Optional mode commands
5.2.2.4	Broadcast mode commands

5. The following note shall be added to the end of 5.2.1.3.

Note: If transmit status mode command is not implemented, then transmit last command mode command shall be used. If neither mode command is implemented, then step 3 shall be deleted.

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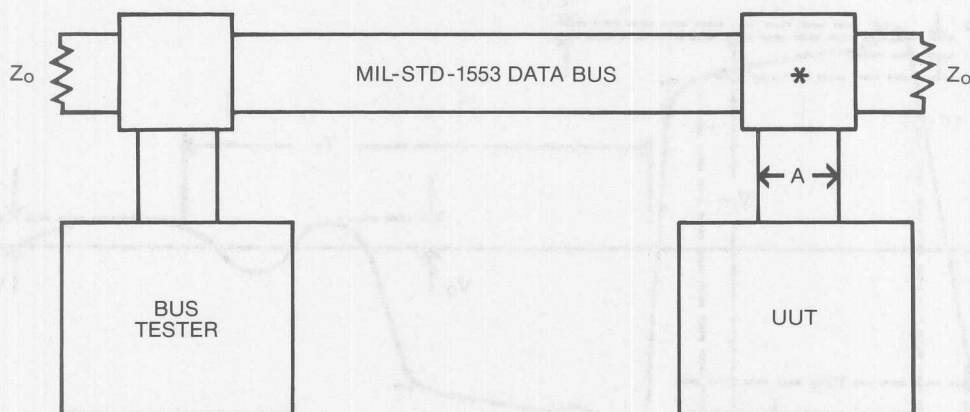


	DIRECT COUPLED	TRANSFORMER COUPLED
R1, R2	35 ohms $\pm 2\%$	70 ohms $\pm 2\%$
R3, R4, R5	20 100	46.5 93.1

### GENERAL RESISTOR PAD CONFIGURATION

Figure 1A.

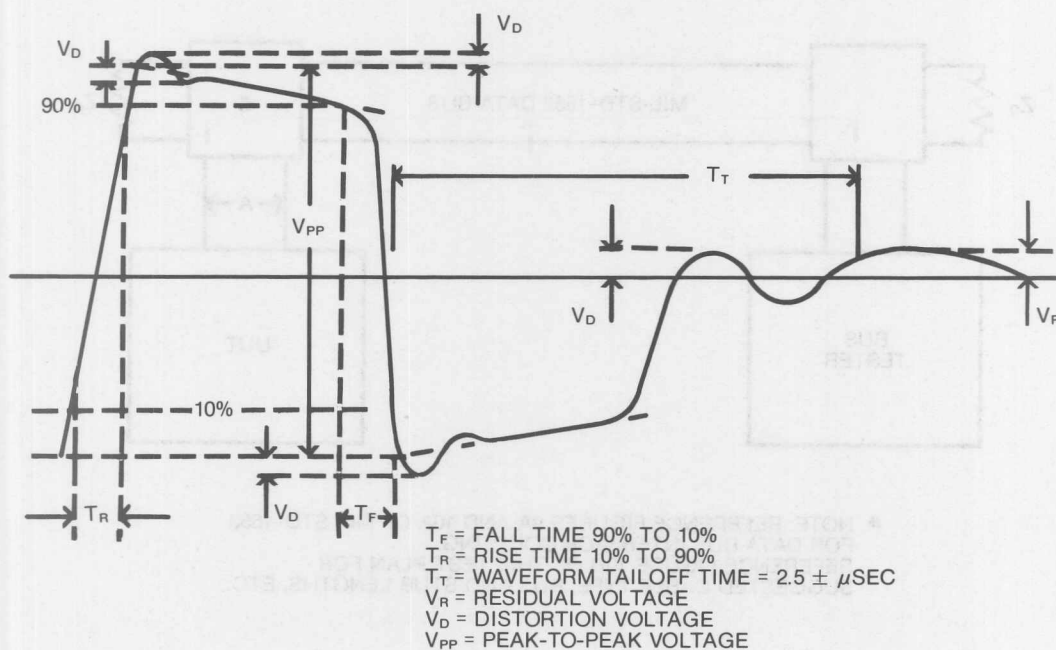
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\* NOTE: REFERENCE FIGURES 9A AND 10A OF MIL-STD-1553 FOR DATA BUS INTERFACE COUPLING. REFERENCE FIGURE 10B OF THIS TEST PLAN FOR SUGGESTED CABLE TYPE, BUS AND STUB LENGTHS, ETC.

**GENERAL BUS CONFIGURATION**  
**Figure 1B.**

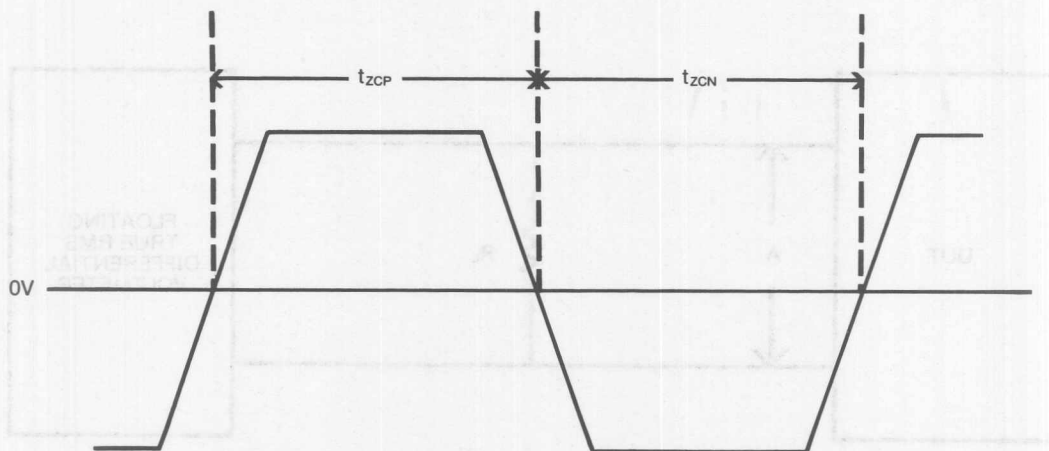
MIL-HDBK-1553  
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### WAVEFORM MEASUREMENTS

Figure 2.

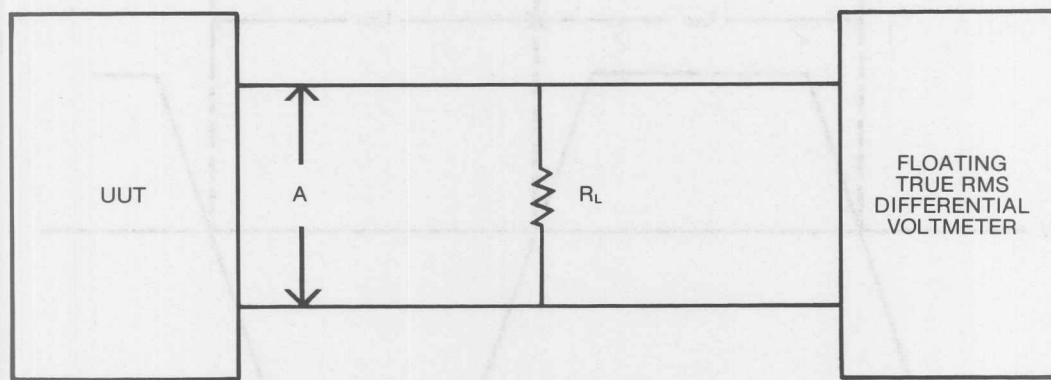
MIL-HDBK-1553  
24 September 1986



### ZERO CROSSING INTERVAL MEASUREMENTS

Figure 3.





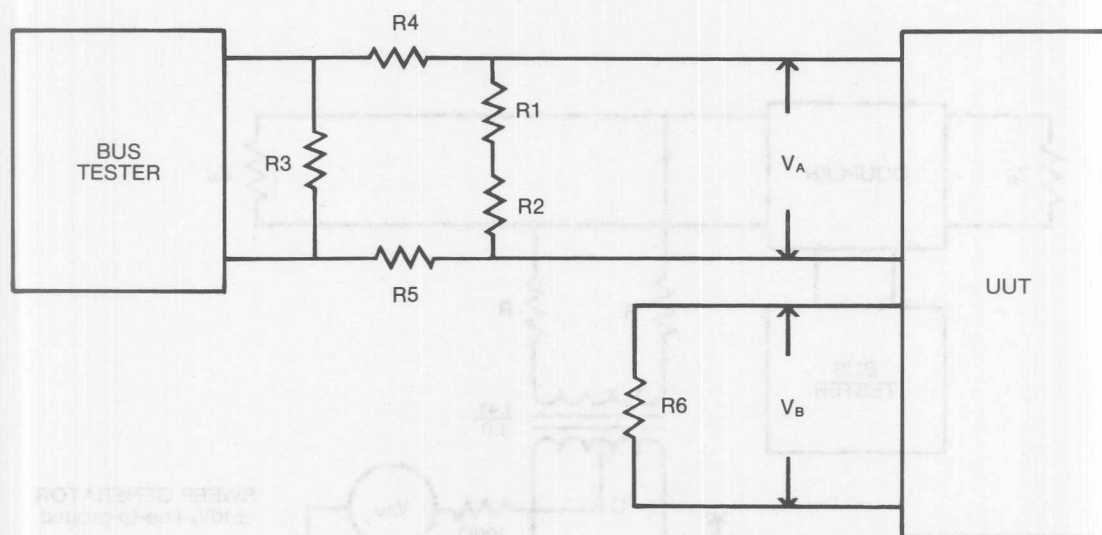
TRANSFORMER COUPLED  
DIRECT COUPLED

$R_L = 70.0 \text{ ohms} \pm 2\%$   
 $R_L = 35.0 \text{ ohms} \pm 2\%$

#### OUTPUT NOISE CONFIGURATION

Figure 4.

MIL-HDBK-1553  
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R1, R2  
R3, R4, R5  
R6

**DIRECT COUPLED**

35 ohms  $\pm 2\%$   
20  
100  
35

**TRANSFORMER COUPLED**

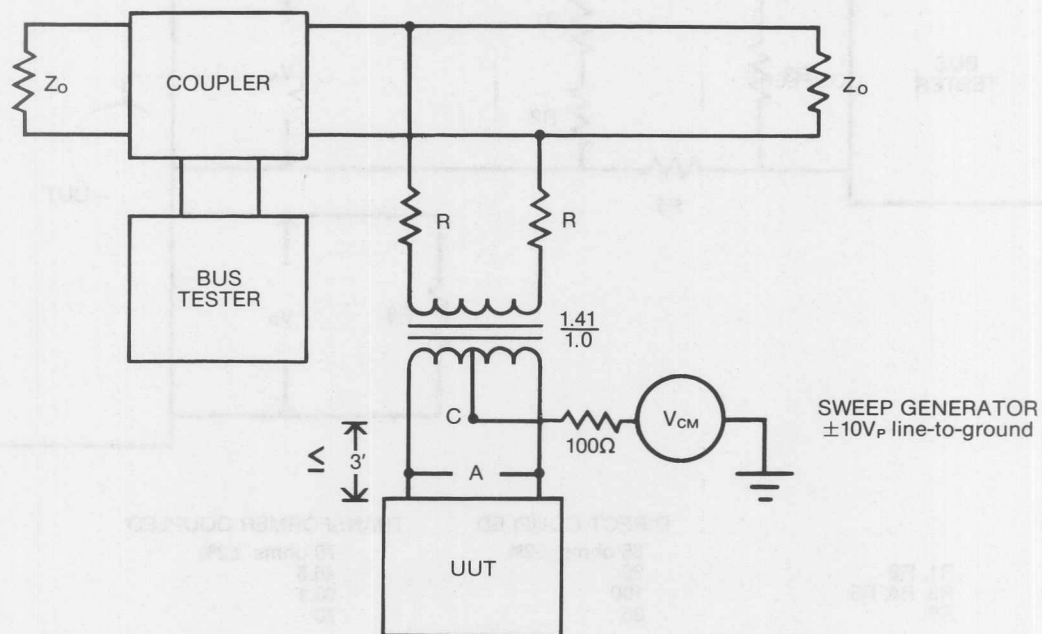
70 ohms  $\pm 2\%$   
46.5  
93.1  
70

$$\text{dB} = 20 \text{ LOG } \frac{V_A}{V_B}$$

**OUTPUT ISOLATION**

Figure 5.

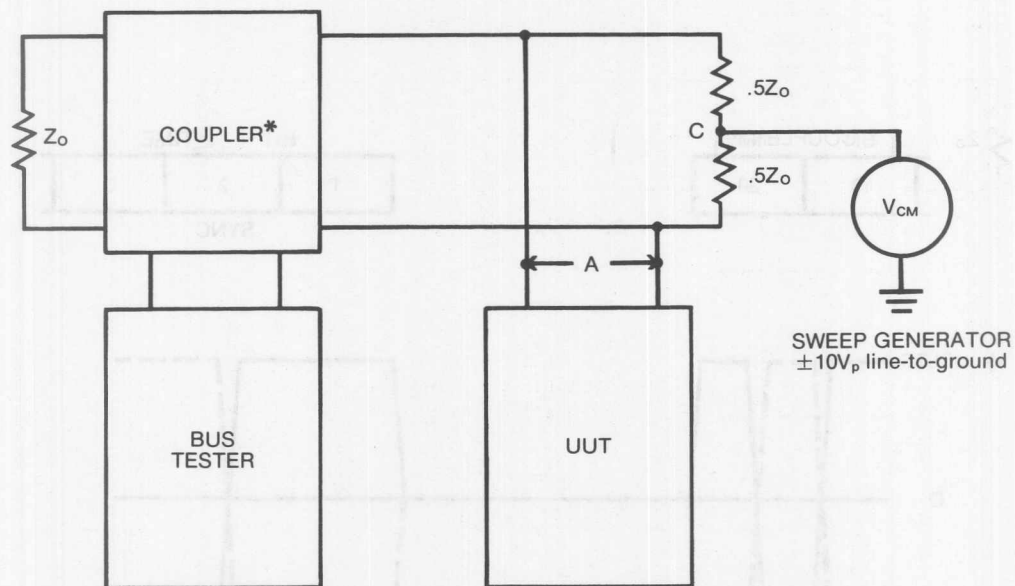
MIL-HDBK-1553  
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$R = 0.75 Z_o \pm 2\%$   
 $Z_o$  — Selected Cable Nominal Characteristic Impedance

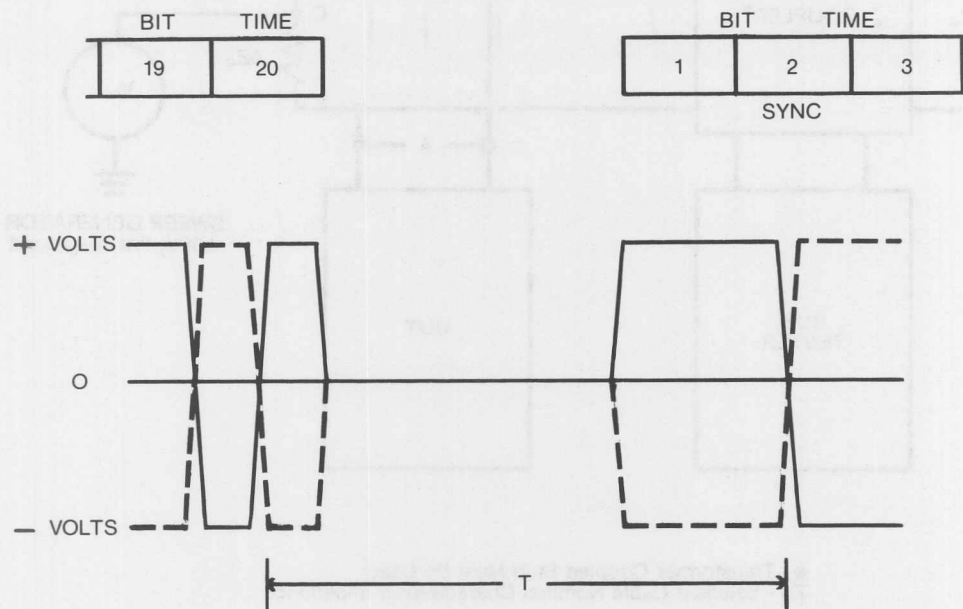
**TRANSFORMER COUPLED  
COMMON MODE CONFIGURATION**  
Figure 6A.

MIL-HDBK-1553  
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\*- Transformer Coupled Stub Must Be Used  
 $Z_o$  - Selected Cable Nominal Characteristic Impedance

**DIRECT COUPLED  
COMMON MODE CONFIGURATION**  
Figure 6B.

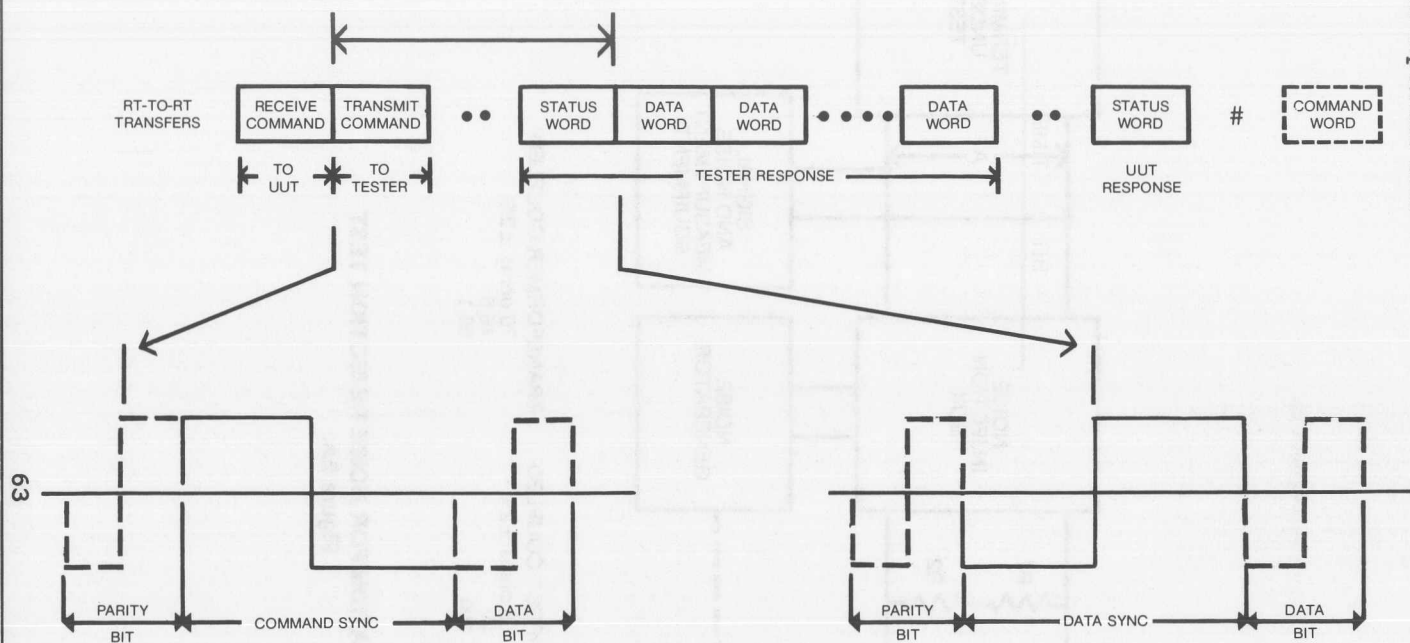


# GAP TIME MEASUREMENT

Figure 7.



MIL-HDBK-1553  
24 September 1986

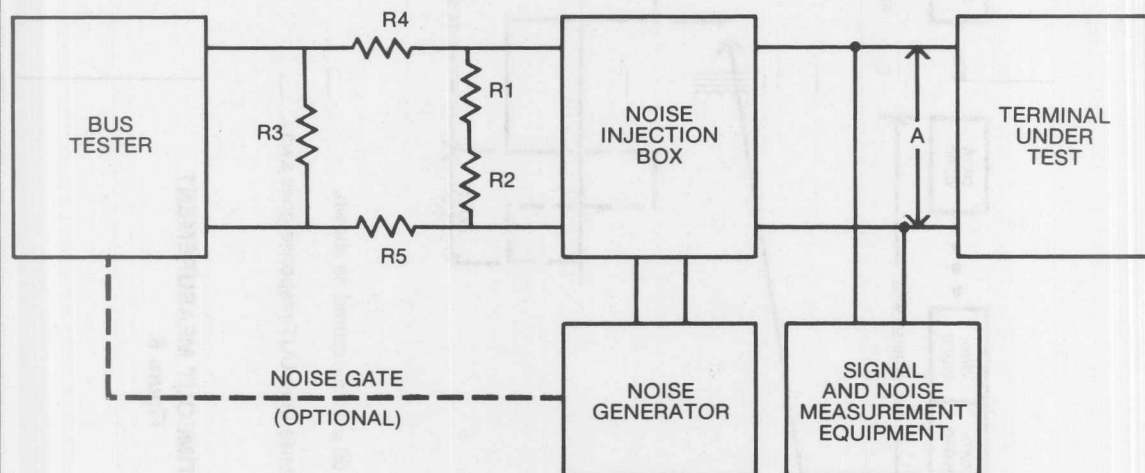


$T = 54 \text{ to } 60 \mu\text{sec}$  measured as shown.

Delay tester response until UUT response goes away.

**RT — RT TIMEOUT MEASUREMENT**  
**Figure 8.**

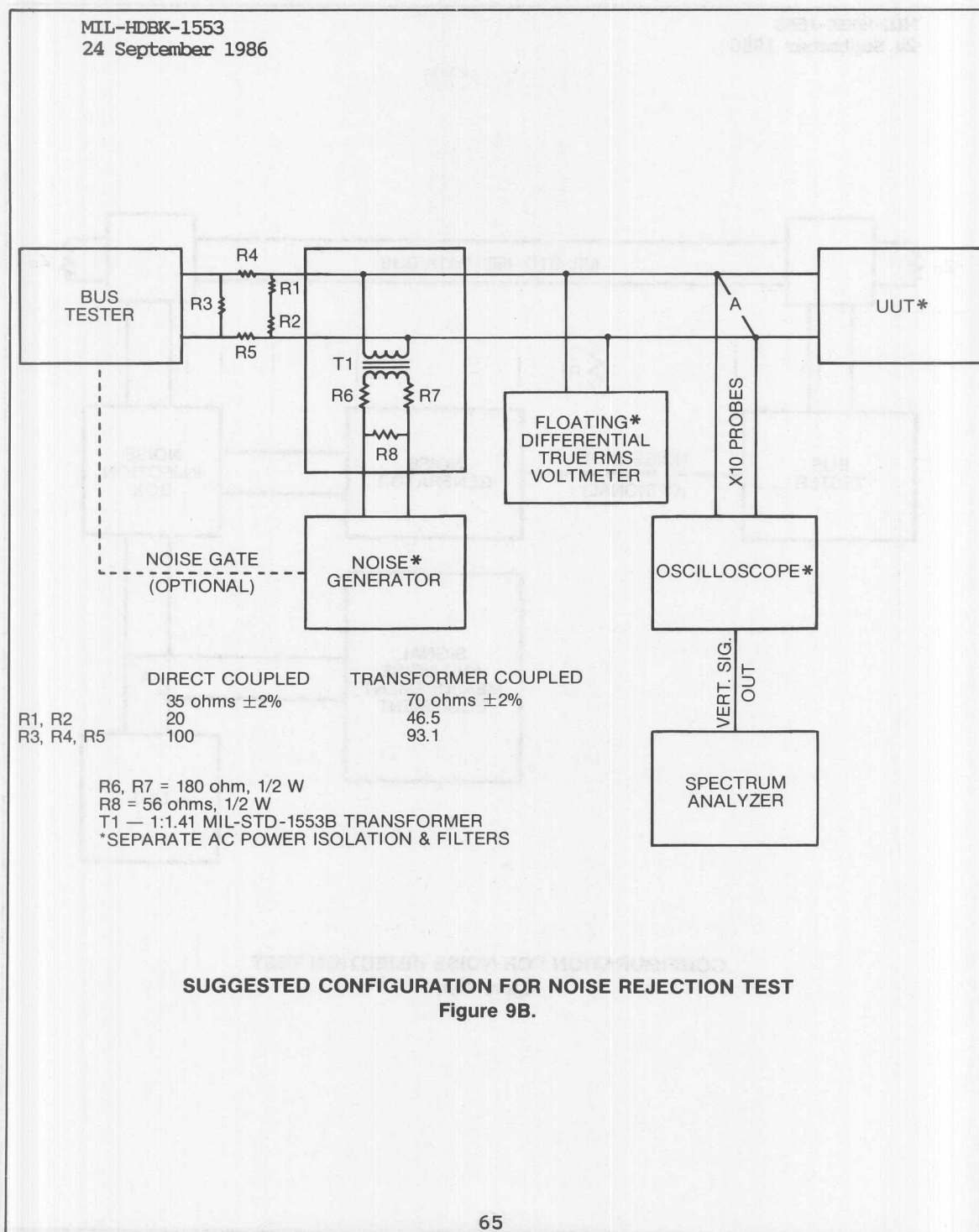
MIL-HDBK-1553  
24 September 1986



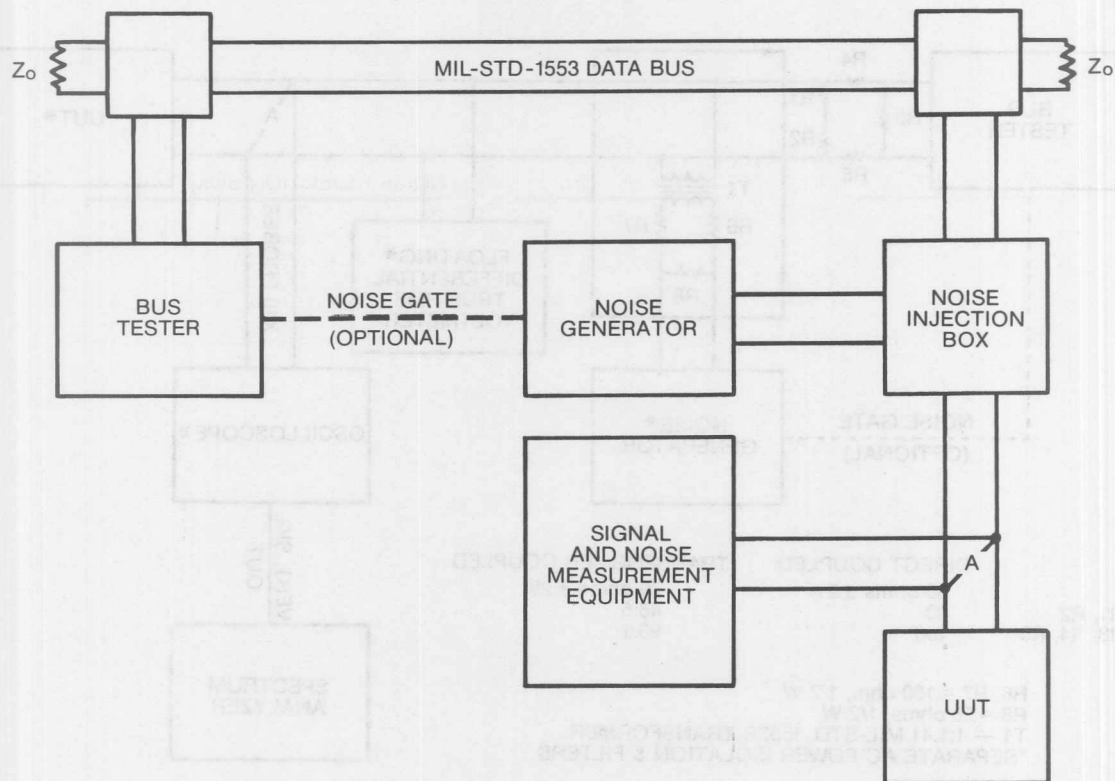
	DIRECT COUPLED	TRANSFORMER COUPLED
R1, R2	35 ohms $\pm 2\%$	70 ohms $\pm 2\%$
R3, R4, R5	20	46.5
	100	93.1

**CONFIGURATION FOR NOISE REJECTION TEST**  
**Figure 9A.**

MIL-HDBK-1553  
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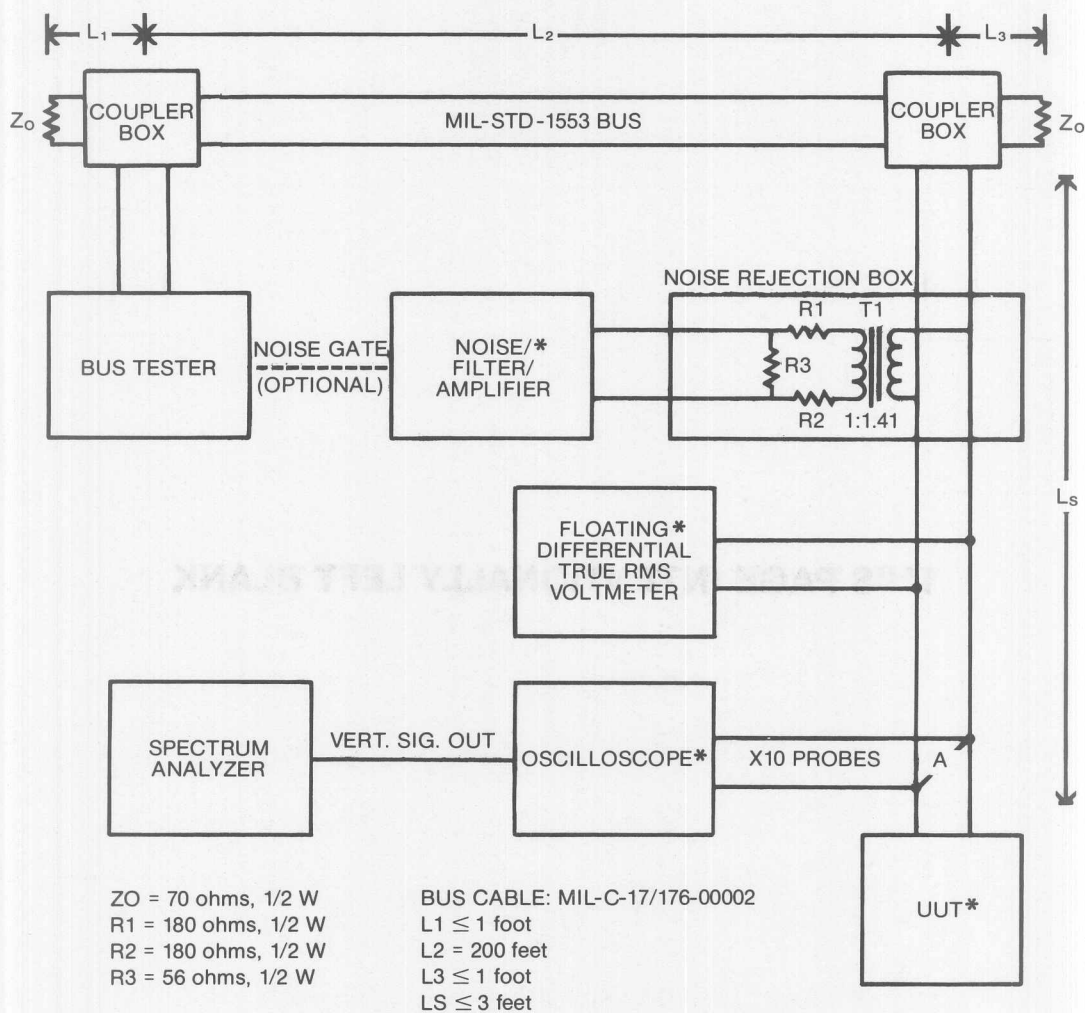


**SUGGESTED CONFIGURATION FOR NOISE REJECTION TEST**  
Figure 9B.



**CONFIGURATION FOR NOISE REJECTION TEST**  
**Figure 10A.**

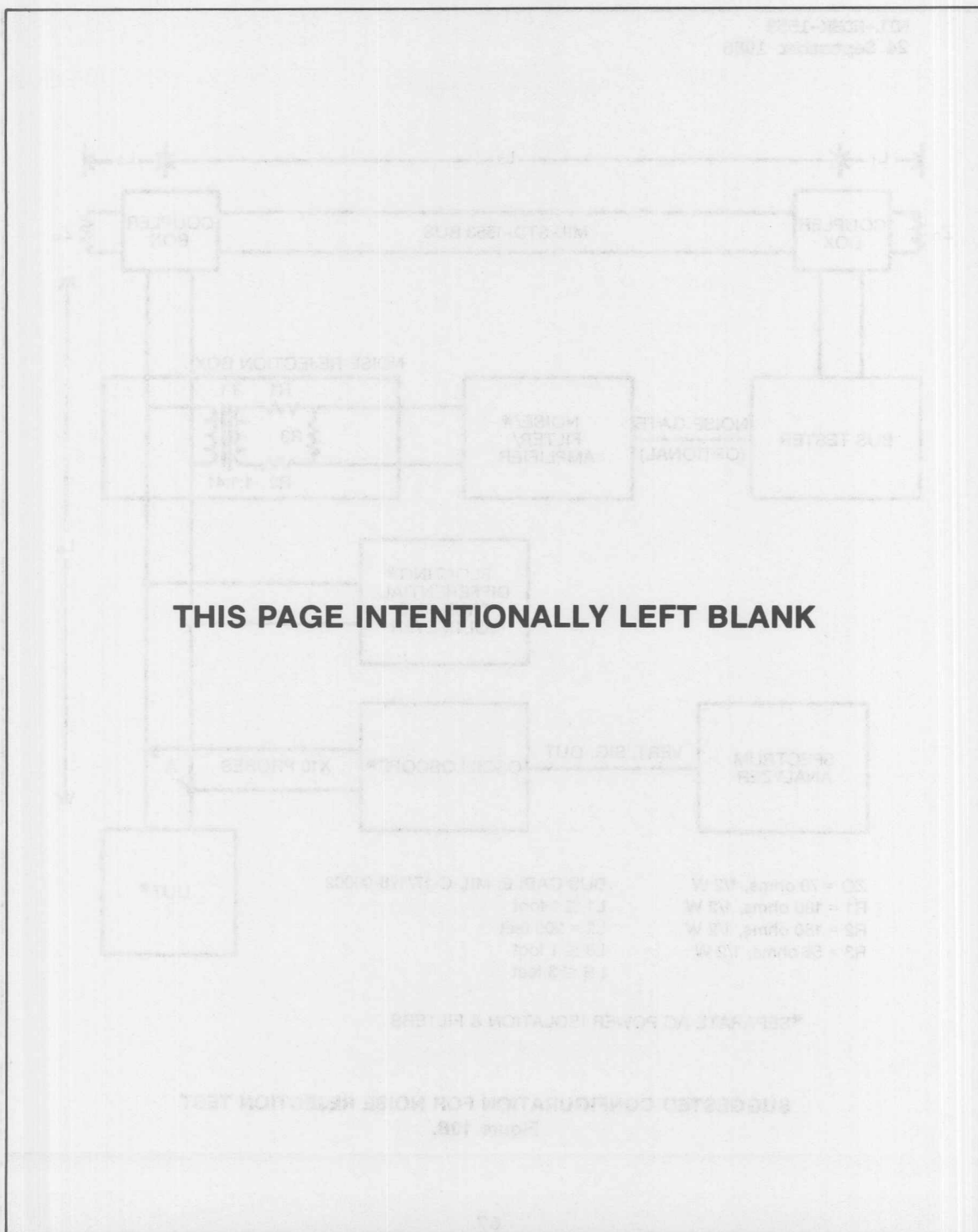
MIL-HDBK-1553  
24 September 1986



\*SEPARATE AC POWER ISOLATION & FILTERS

**SUGGESTED CONFIGURATION FOR NOISE REJECTION TEST**  
Figure 10B.





## VII. DATA BUS PRODUCT INFORMATION

PRODUCTS	MONOLITHIC CHIP	MIL-STD-1538	MIL-STD-1533A	McA86	± 10V	± 12V	± 5V	INVERTED OUTPUT	BUS CONTROLLER	REMOTE TERMINAL	BUS MONITOR	SINGLE CHANNEL	DUAL REDUNDANT	ENCODER/DECODER	8 BIT I/O	16 BIT I/O	SHARED RAM	MEMORY MGMT.	TIME - 1V <sup>1</sup>	UNIBUS <sup>®</sup>	MULTIBUS <sup>®</sup>	IBM PC <sup>®</sup> BUS	GRiD <sup>®</sup>	PLUG-IN	FLATPACK	PIN GRID ARRAY	MODULE	IEEE-488	RS-232	SEAFAC TESTED	NOTES	
<b>TRANSCEIVERS</b> <b>Single:</b>																																
BUS-8553	•	•			•		•																	•						•	A.K. A. BUS-63100	
BUS-8555 (Receiver)	•	•	•	•	•	•	•	•																•	•						A.K. A. BUS-63100	
BUS-63102 II	•	•	•	•	•	•	•																	•	•						Universal T/R.	
BUS-63104 II	•	•	•	•	•	•	•																	•	•							
BUS-63105 II	•	•	•		•		•																	•	•						•	MIL-DWG (DESC) No. 5962-86049-01ZC **
BUS-63107 II	•	•	•		•		•																	•							**	
BUS-63115 II	•	•	•		•		•	•																•							**	
BUS-63117 II	•	•	•		•		•	•																•							**	
<b>Dual:</b>																																
BUS-63125 II	•	•	•		•		•																	•	•						•	MIL-DWG (DESC) No. 5962-87579-02XC **
BUS-63125 II - 641																															- 641 is BUS-65612 compatible.	
BUS-63127 II	•	•	•		•		•																	•							**	
BUS-63135 II	•	•	•		•		•	•																•							**	
BUS-63137 II	•	•	•		•		•	•																•							**	
BUS-63147 & BUS-63148	•	•				•																	•								Low power, +5V only MIL-DWG (DESC) No. 5962-89522-01XC BUS-63148 is BUS-65612 compatible.	
<b>COMPLETE TERMINALS</b>																																
BUS-61553 AIM-HY	•	•		•		•			•	•	•	•					•	•	•					•	•						•	MIL-DWG (DESC) No. 5962-88692-01XC No. 5962-88692-01YC Contains MK II Contains 8K x 16 RAM **
BUS-61554 AIM-HY	•	•		•		•			•	•	•	•					•	•	•					•	•							Contains low power transceivers
BUS-61555 AIM-HY	•	•		•		•			•	•	•	•					•	•	•					•	•							MIL-DWG (DESC) No. 5962-88692-02XC ** No. 5962-88692-02YC
BUS-61565	•	•		•		•			•	•	•	•					•	•	•					•								Contains +5V transceivers
BUS-61556	•	•		•		•			•	•	•	•					•	•	•					•								Transceiverless-use with BUS-63102 II
BUS-61559 & BUS-61569	•	•		•		•			•	•	•	•					•	•	•					•	•						•	Enhanced AIM-HY-Contains data buffers, RT MEM MGMT, & additional interrupt capability. 78pin package, contains low, power transceivers.
BUS-65111	•	•		•		•			•		•						•							•	•							MIL-DWG (DESC) No. 5962-87632-01XC, replaces BUS-65113, with low power MK II transceivers. **
BUS-65112	•	•		•		•			•		•						•							•								MIL-DWG (DESC) No. 5962-87535-01XC, 12 MHz clock, with transceiver.
BUS-65142	•	•		•		•			•		•						•							•	•							Low cost 2 chip RTU, 16 MHz clock, with transceiver. **
BUS-65149	•	•	•	•	•	•	•		•		•						•															Multi protocol RT, 1553A/B/ McA86, 12 or 16 MHz clock. Ceramic package 90pin, contains universal transceivers.
BUS-65153	•	•		•		•			•		•						•							•								Low cost 1553B RT 8/16 bit I/O, 12/16 MHz clock, ceramic 70pin package contains low power transceivers.
BUS-65600	•			•		•			•	•	•	•					•							•	•							MIL-DWG (DESC) No. 5962-88585-01XC, 12 MHz clock, without transceiver.
BUS-65610 & BUS-65611	•	•		•		•			•	•	•	•					•							•	•							16 MHz clock, single chip, without transceiver
BUS-65612	•	•		•		•			•	•	•	•					•														•	16 MHz clock, single chip, without transceiver
BUS-66300 II	•			•		•			•		•						•							•	•							MIL-DWG (DESC) No. 5962-88586-01XC, Universal RAM Controller (1K-64K)
BUS-66312	•			•		•			•		•						•															Universal Ram Controller (1K-64K)

\* Inverted output means RX DATA OUT and RX DATA OUT of receiver are HIGH when data is not on the bus.

\*\* Roman numeral II versions are low power and do not require + Vcc.

® IBM PC is a registered trademark of International Business Machines Corporation.

Continued on reverse side

® Unibus is a registered trademark of Digital Equipment Corporation.

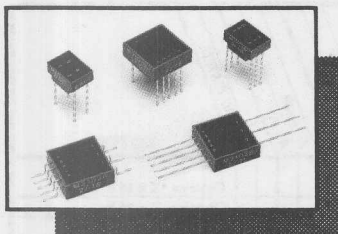
® Multibus is a registered trademark of Intel Corporation.

® GRiD is a registered trademark of GRiD Systems Corporation.

# PRODUCTS FOR MIL-STD-1553 DATA BUS

PRODUCTS	MONOLITHIC CHIP	MIL-STD-1553B	MeAIR	± 15V	± 12V	± 5V	INVERTED OUTPUT*	BUS CONTROLLER	REMOTE TERMINAL	SINGLE MONITOR	DUAL CHANNEL	DUAL REDUNDANT	ENCODER/DECODER	DUMB RTU	8 BIT I/O	16 BIT I/O	SHARED RAM	MEMORY MGMT.	VME - VXI	UNIBUS®	MILIBUS®	IBM PC® BUS	GRID®	PLUG-IN	FLATPACK	PIN GRID ARRAY	MODULE	IEEE-488	RS-232	SEMIAC TESTED	NOTES
<b>CARD ASSEMBLIES</b>																															
BUS-65505	•				•	•		•	•	•					•		•	•		•											Contains 4K x 16 RAM.
BUS-65506	•			•				•	•	•							•	•													Contains 4K x 16 RAM.
BUS-65508	•			•				•	•	•							•	•													Contains 4K x 16 RAM.
BUS-65509	•							•	•	•							•	•			•										Contains 4K x 16 RAM.
BUS-65515	•				•	•		•	•	•					•		•	•				•									Contains 4K x 16 RAM.
BUS-65517 II & DISK	•							•	•	•					•		•	•				•									Software and 32K x 16 RAM, Error injection capability. Simultaneous Emulation of BC, up to 31 RTs, and MT.
BUS-65519	•				•	•		•	•	•					•		•	•				•									RT Production Test Plan (PTP) protocol tester card with menu & run time libraries - software.
BUS-65522	•				•	•		•	•	•							•	•													Replaces BUS-65502. Contains 8K x 16 RAM VMEbus and VXIbus.
BUS-65523	•		•	•	•	•		•	•	•					•		•	•													Replaces BUS-65503. Contains 8K x 16 RAM VMEbus and VXIbus.
BUS-65555	•					•		•	•	•					•		•	•					•								1553B RT/BC/MT, 8K RAM module for GRID® ruggedized laptop.
<b>TESTERS</b>																															
BUS-68005	•	•						•	•	•					•													•	•		Error injection and detection.
BUS-68010	•							•	•	•																					Low cost
BUS-68011	•							•	•	•																					230 VAC
BUS-68015	•	•	•					•	•	•																			•	•	Noise generator, BER tester.
BUS-69005/6 (DISKS)	•																					•						•			Software-RTU Production Test Plan. With BUS-68005
<b>SPECIAL TEST EQUIPMENT</b>																															
BUS-8559	•	•				•																	•								Variable output transceiver. A. K. A. BUS-63109
BUS-1555	•	•	•			•				•		•			•											•					Error detection capability.
BUS-1556	•	•	•			•				•		•			•											•					Error generation capability.
<b>SEMS</b>																															
BUS-9253	•	•			•	•				•	•			•	•											•					Key code MAN.
BUS-67001	•	•	•		•	•				•		•		•	•																M28787/348 Key code UKT.
BUS-67002	•	•						•				•		•	•											•					M28787/349 Key code UKU.
BUS-67003	•	•						•				•		•	•											•					M28787/367 Key code UKS.
BUS-67007	•					•		•	•	•		•		•	•		•	•													SEM E module. 1750A micro & 1553B RT/BC/MT & RS 422 port. 5V power. MIL-M-28787/TBD key code = ESAP.

STANDARD MIL-DWIGS (DESC)																																PRODUCT
5962-86049-01XC	•	•	•																													BUS-63105
5962-87535-01XC	•	•	•																													BUS-65112
5962-87579-02XC	•	•	•																													BUS-63125 II
5962-87632-01XC	•	•	•																													BUS-65111
5962-88585-01XC	•	•	•																													BUS-65600
5962-88586-01XC	•	•	•																													BUS-66300 II
5962-88692-01XC	•	•	•																													BUS-61553
5962-89522-01XC	•	•	•																													BUS-61554
																																BUS-63147



## MIL-STD-1553 TRANSFORMERS TO DESC SPECIFICATION NO. 21038/27

### FEATURES

- FULLY QUALIFIED TO DESC SPECIFICATION NO. 21038/27
- FOR USE WITH MIL-STD-1553A AND B, MACAIR A-3818, A-5690, A-5232, AND A-4905
- LOW PROFILE
- -55°C TO +130°C OPERATING TEMPERATURE RANGE
- BUILT AND TESTED TO MIL-T-21038 AND MIL-STD-202
- LISTED ON QPL-21038-31
- QUALIFICATION VALIDATED ANNUALLY

### DESCRIPTION AND APPLICATIONS

The military data bus specification, MIL-STD-1553, has brought about the need for versatile pulse transformers that meet all the electrical requirements of Manchester II serial bi-phase data transmission. The B-2200/2300 series of transformers provide the turns ratio configurations, component isolation, and common mode rejection ratio characteristics necessary for MIL-STD-1553A and B compliance.

The step up and down ratios that are available with the B-2200/2300 series complement DDC's entire MIL-STD-1553 product line and are compatible with competitor's drivers, receivers, and transceivers. These transformers are low profile, modular units that are multi-tapped to accommodate existing system configurations. Encapsulated in accordance with MIL-T-21038, their tin coated steel leads conveniently accommodate printed circuit board mounting. Sinusoidal or trapezoidal waveforms are accurately processed, making the B-2200/2300 series of transformers an excellent choice for any MIL-STD-1553A or B application.

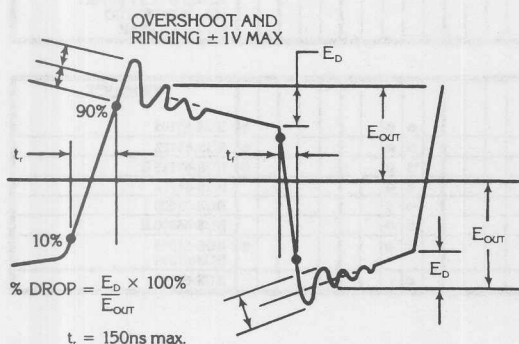


FIGURE 1. WAVEFORM INTEGRITY

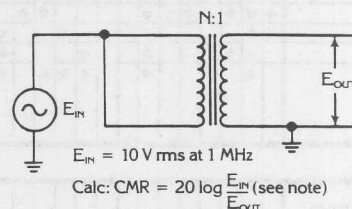


FIGURE 2. CIRCUIT FOR COMMON MODE REJECTION

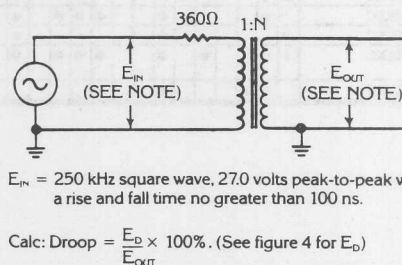


FIGURE 3. CIRCUIT FOR WAVEFORM INTEGRITY

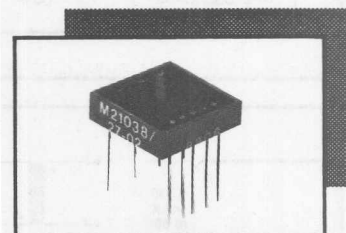
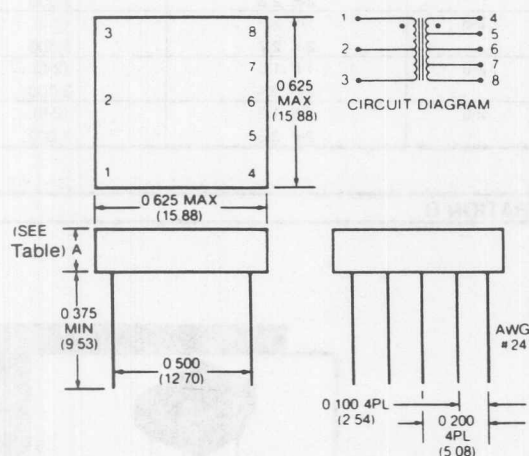
Note: Input to be applied and output to be measured for all dash numbers as shown. N represents highest turn winding in each test.



TABLE 1. B-2200/2300 SERIES SPECIFICATIONS

PARAMETER	UNIT	VALUE	REMARK
Case			Flame Resistant, DIALLYL PHTHALATE
Terminals			Copper Clad Steel (soft tinned)
Weight	Oz (gm)	0.175(5) max	
Terminal Strength	lbs	2	2 pounds applied force, Method 211, MIL-STD-202, Test condition A
Dielectric Withstanding Voltage	Vrms	100	Method 301, MIL-STD-202
Life (expectancy "X")	Hrs	10,000 min	In accordance with MIL-T-21038
Insulation Resistance	M Ohm	1,000 min	At 250Vdc using method 302, test condition B, MIL-STD-202
Pulse Width (of Output Pulse)	μs	2	Tested using figure 3 with resulting figure 1 waveform.
Overshoot	V	< 1	Tested using figure 3 with resulting figure 1 waveform.
Rise Time (of Output Pulse)	ns	< 150	Tested using figure 3 with resulting figure 1 waveform.
Common Mode Rejection	db	45 min	Tested using figure 2
Operating Temperature Range	°C	-55 to +130	
Droop	%	20 max	Tested using figure 3 with resulting figure 1 waveform.
DC Resistance	Ohm		See respective Electrical Characteristics Table
Input Impedance	Ohm		See respective Electrical Characteristics Table

## CONFIGURATION A

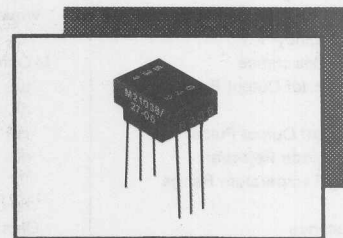
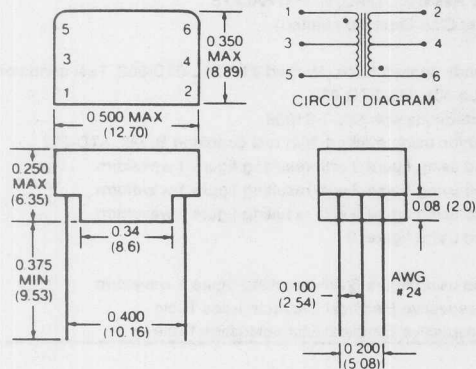


Notes  
(1) Dimensions are in inches (mm)  
(2) Unless otherwise specified, tolerance is  $\pm 0.010$  inches (0.25 mm)

TABLE 2. ELECTRICAL CHARACTERISTICS - CONFIGURATION A

BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	"A" (max)	DC RESISTANCE $\Omega$ (max)	IMPEDANCE $\Omega$ (min)
B-2202	M-21038/27-01	1:1 $\pm 3\%$	1-3	4-8		1-3 3.0	(1-3)
		1:0.707 $\pm 3\%$	1-3	5-7	0.300	4-8 3.0	4,000
B-2203	M-21038/27-02	1.4:1 $\pm 3\%$	1-3	4-8		1-3 3.5	(1-3)
		2:1 $\pm 3\%$	1-3	5-7	0.250	4-8 3.0	7,200
B-2204	M-21038/27-03	1.25:1 $\pm 3\%$	1-3	4-8		1-3 3.2	(1-3)
		1.66:1 $\pm 3\%$	1-3	5-7	0.250	4-8 3.0	4,000
B-2205	M-21038/27-04	2.3:1 $\pm 3\%$	1-3	4-8		1-3 1.2	(5-7)
		3.2:1 $\pm 3\%$	1-3	5-7	0.300	4-8 3.0	3,000
B-2385	M-21038/27-10	2.12:1 $\pm 3\%$	4-8	1-3		1-3 1.0	(4-8)
		1.5:1 $\pm 3\%$	5-7	1-3	0.250	4-8 3.0	4,000

## CONFIGURATION B



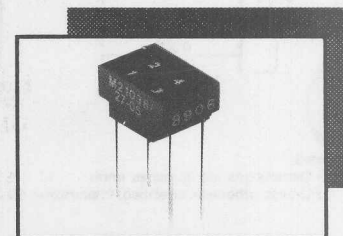
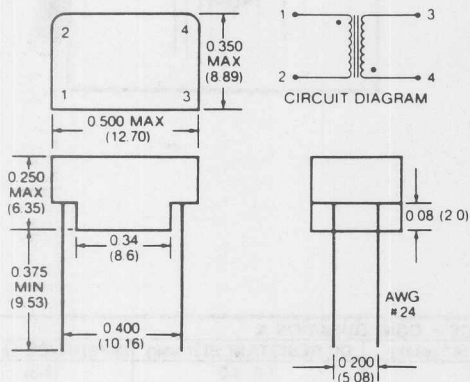
### Notes

- (1) Dimensions are in inches (mm)  
 (2) Unless otherwise specified, tolerance is  $\pm 0.010$  inches (0.25 mm)

TABLE 3. ELECTRICAL CHARACTERISTICS - CONFIGURATION B

BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE $\Omega$ (max)	IMPEDANCE $\Omega$ (min)
B-2207	M-21038/27-06	1:1 $\pm 3\%$	1-5	2-6	1-5 2.5 2-6 2.8	(1-5) 3,000
B-2208	M-21038/27-07	1:1.41 $\pm 3\%$	1-5	2-6	1-5 2.2 2-6 2.7	(2-6) 3,000
B-2209	M-21038/27-08	1:1.66 $\pm 3\%$	1-5	2-6	1-5 1.5 2-6 2.4	(2-6) 3,000
B-2210	M-21038/27-09	1:2 $\pm 3\%$	1-5	2-6	1-5 1.3 2-6 2.6	(2-6) 3,000

## CONFIGURATION C



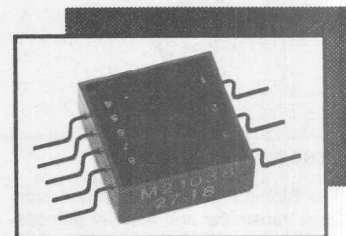
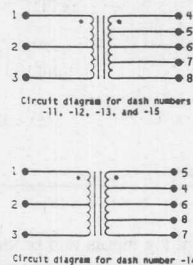
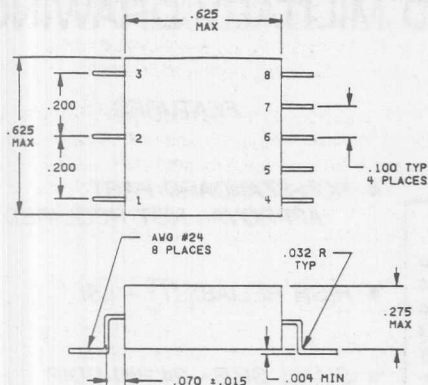
### Notes

- (1) Dimensions are in inches (mm)  
 (2) Unless otherwise specified, tolerance is  $\pm 0.010$  inches (0.25 mm)

TABLE 4. ELECTRICAL CHARACTERISTICS - CONFIGURATION C

BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE $\Omega$ (max)	IMPEDANCE $\Omega$ (min)
B-2206	M-21038/27-05	1:1.41 $\pm 3\%$	1-2	3-4	1-2 2.2 3-4 2.7	(3-4) 3,000

## CONFIGURATION D

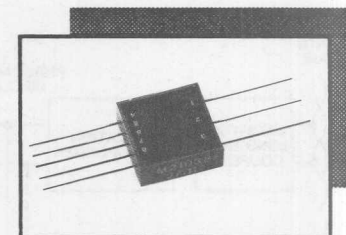
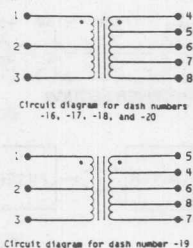
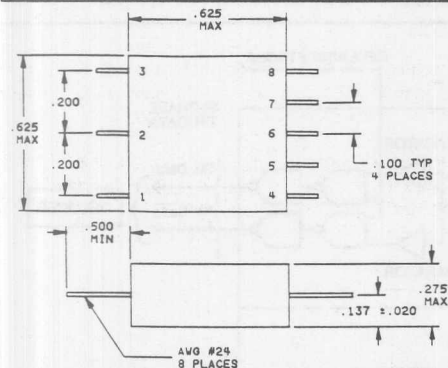


- Notes  
(1) Dimensions are in inches  
(2) Unless otherwise specified, tolerance is  $\pm 0.010$  inches

TABLE 5. ELECTRICAL CHARACTERISTICS - CONFIGURATION D

BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE $\Omega$ (max)	IMPEDANCE $\Omega$ (min)
B-2386	M-21038/27-11	1:1 $\pm 3\%$	1-3	4-8	1-3 3.0	(1-3)
		1:0.707 $\pm 3\%$	1-3	5-7	4-8 3.0	4,000
B-2387	M-21038/27-12	1.4:1 $\pm 3\%$	1-3	4-8	1-3 3.5	(1-3)
		2:1 $\pm 3\%$	1-3	5-7	4-8 3.0	7,200
B-2388	M-21038/27-13	1.25:1 $\pm 3\%$	1-3	4-8	1-3 3.2	(1-3)
		1.66:1 $\pm 3\%$	1-3	5-7	4-8 3.0	4,000
B-2389	M-21038/27-14	2.3:1 $\pm 3\%$	4-8	1-3	1-3 1.2	(5-7)
		3.2:1 $\pm 3\%$	5-7	1-3	4-8 3.0	3,000
B-2390	M-21038/27-15	2.12:1 $\pm 3\%$	4-8	1-3	1-3 1.0	(4-8)
		1.5:1 $\pm 3\%$	5-7	1-3	4-8 3.0	4,000

## CONFIGURATION E

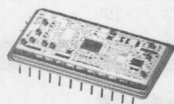


- Notes  
(1) Dimensions are in inches  
(2) Unless otherwise specified, tolerance is  $\pm 0.010$  inches

TABLE 6. ELECTRICAL CHARACTERISTICS - CONFIGURATION E

BETA P/N	DESC P/N	TURNS RATIO	PRIMARY	SECONDARY	DC RESISTANCE $\Omega$ (max)	IMPEDANCE $\Omega$ (min)
B-2342	M-21038/27-16	1:1 $\pm 3\%$	1-3	4-8	1-3 3.0	(1-3)
		1:0.707 $\pm 3\%$	1-3	5-7	4-8 3.0	4,000
B-2343	M-21038/27-17	1.4:1 $\pm 3\%$	1-3	4-8	1-3 3.5	(1-3)
		2:1 $\pm 3\%$	1-3	5-7	4-8 3.0	7,200
B-2344	M-21038/27-18	1.25:1 $\pm 3\%$	1-3	4-8	1-3 3.2	(1-3)
		1.66:1 $\pm 3\%$	1-3	5-7	4-8 3.0	4,000
B-2345	M-21038/27-19	2.3:1 $\pm 3\%$	4-8	1-3	1-3 1.2	(5-7)
		3.2:1 $\pm 3\%$	5-7	1-3	4-8 3.0	3,000
B-2391	M-21038/27-20	2.12:1 $\pm 3\%$	4-8	1-3	1-3 1.0	(4-8)
		1.5:1 $\pm 3\%$	5-7	1-3	4-8 3.0	4,000

## BUS-63105 MIL-STD-1553 TRANSCEIVER TO MILITARY DRAWING



### FEATURES

- NON-STANDARD PART  
APPROVAL NOT REQUIRED
- HIGH RELIABILITY – LSI
- SMALL SIZE – 24 PIN DDIP
- LOW POWER
- SHORT CIRCUIT PROTECTED
- INPUT TRANSMITTER PROTECTION TIME OUT CIRCUIT
- SUPERIOR FILTERING

### DESCRIPTION

The BUS-63105 transceiver is a complete transmitter and receiver pair conforming fully to MIL-STD-1553A and B, packaged in a small 24 pin DDIP. It is available to Military Drawing No. 5962-86049 and does not require non-standard part approval.

The receiver section accepts a phase-modulated bipolar data at the inputs and produces bi-phase TTL signals at the outputs. These outputs, DATA and  $\overline{\text{DATA}}$ , represent positive and negative variations of the inputs beyond an internally fixed threshold. The thresholds are factory set for a nominal 1Vpp signal. An external STROBE input is provided to take the receiver off-line. A logic "0" applied to the STROBE input will disable the receiver output.

The transmitter section accepts bipolar

TTL data at the inputs and produces a 27Vpp nominal differential signal across a 145 $\Omega$  load. When coupled to the data bus with the specified transformers, 55 $\Omega$  fault isolation resistors, and loaded by 70 $\Omega$  terminators, a 6.5Vpp signal is produced. When the DATA and  $\overline{\text{DATA}}$  inputs are both kept at the same logic level, the transmitter presents a high impedance. An external TX INHIBIT input is provided to take the transmitter output off-line. A logic "1" applied to the TX INHIBIT input takes priority over the condition of the data inputs and disables the transmitter.

Additional features of the BUS-63105 include low power dissipation, superior filtering, and high reliability, making it an excellent choice for MIL-STD-1553 transceiver applications.

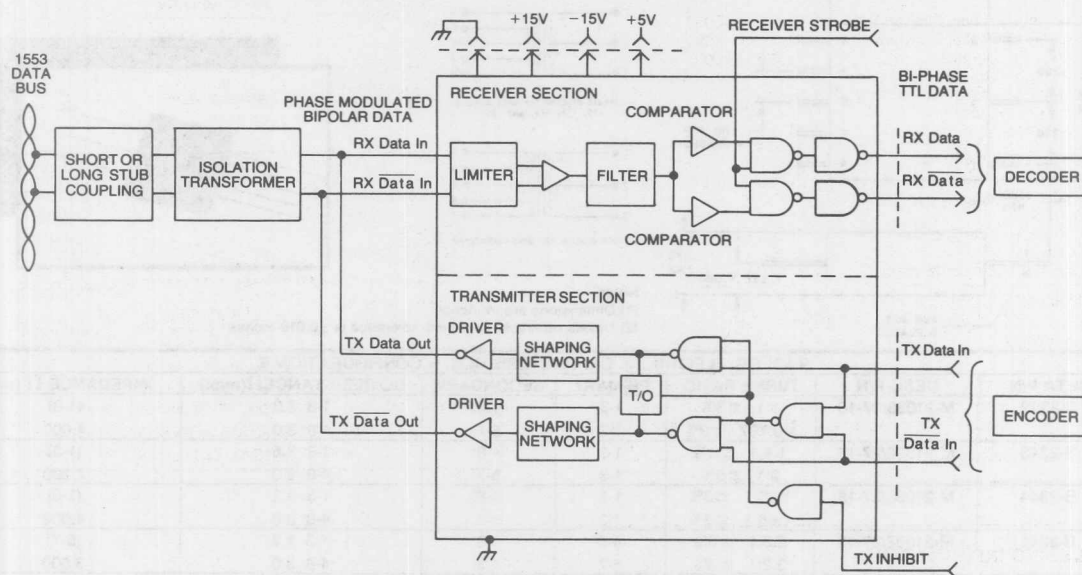


FIGURE 1. BUS-63105 AND 5962-86049 BLOCK DIAGRAM

**TABLE 1. BUS-63105 AND 5962-86049 SPECIFICATIONS\***

\* The information and specifications in this data sheet are for reference only. Complete specifications are on DESC drawing no. 5962-86049 available from the factory or:

DESC-E  
1507 Wilmington Pike  
Dayton, OH. 45444  
(573) 296-6511

**RECEIVER**

Strobe  
Input Level  
Threshold Level (Internal)\*\*  
CMRR  
Input Resistance – Diff  
Input Capacitance – Diff  
Output Fan Out

1 TTL Load  
40Vpp, Diff, max  
0.56Vpp min, 1.0Vpp max  
40 db, min  
7K $\Omega$ , min  
5pf, max  
10 TTL Loads

**TRANSMITTER**

TX Inhibit  
Input Level  
Output Level (Direct Coupled)  
Rise/Fall Time  
Output Noise  
Output Offset Voltage  
Output Impedance  
– Non-Transmitting  
Output Resistance – Diff  
Output Capacitance – Diff

1 TTL Load  
1 TTL Load  
28Vpp, nom across 140 $\Omega$  load  
125ns, typ  
10mVpp, Diff, max  
90mVpp, max across 35 $\Omega$  load  
10K $\Omega$ , min  
5pf, max

**LOGIC**

TTL/CMOS Compatible  
All Logic Inputs  
(Loading Requirements)  
All Logic Outputs (Fan Out)

1 TTL Load, max  
10 TTL Loads, min

**POWER SUPPLY REQUIREMENTS**

+5V $\pm$ 5% +15V $\pm$ 5% –15V $\pm$ 5%  
Non-Transmitting – (typ/max)  
Transmitting –  
50% duty cycle (typ/max)  
Transmitting –  
100% duty cycle (typ/max)

25/35mA 35/50mA 35/50mA  
25/35mA 35/50mA 125/140mA  
25/35mA 35/50mA 200/220mA

**THERMAL**

Operating Junction Temperature  
Operating Case Temperature  
Storage Temperature  
Thermal Impedance –  
Junction (Hottest Die) to Case  
Thermal Impedance –  
Case to Air (typ)

–55°C to +160°C  
–55°C to +125°C  
–65°C to +150°C  
8.8°C/W  
30°C/W

**POWER DISSIPATION**

Single Channel (Hottest Die)  
Non-Transmitting – (typ/max)  
Transmitting –  
50% duty cycle (typ/max)  
Transmitting –  
100% duty cycle (typ/max)

15V Supply  
1.21/1.5W  
1.8/2.2W  
2.4/2.9W

**MECHANICAL**

Size  
Dimensions  
Weight

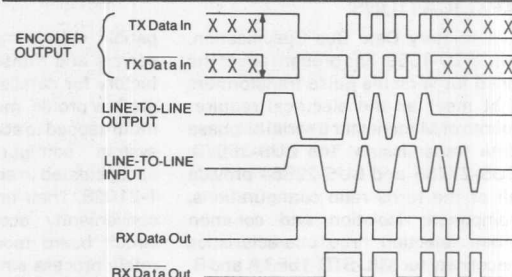
24 Pin DDIP  
1.4" x 0.8" x 0.2"  
.4 oz

Note: \*\* The Threshold Level, as referred to in this specification, is meant to be the maximum peak to peak voltage (measured on the Data Bus) that can be applied to the receivers' input without causing the output to change from the OFF state.

**TABLE 2. PIN CONNECTIONS**

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	TX Data Out	13	+15V
2	TX Data Out	14	NC
3	GND*	15	RX Data In
4	NC	16	RX Data In
5	NC	17	NC
6	NC	18	GND*
7	RX Data Out	19	–15V
8	Strobe	20	+5V
9	GND*	21	TX Inhibit
10	RX Data Out	22	TX Data In
11	NC	23	TX Data In
12	NC	24	NC

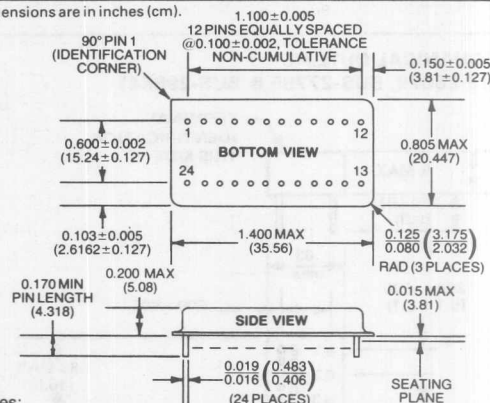
\*Connect all GND pins externally, close to hybrid.



- Notes:  
(1) TX Data In and RX Data Out are TTL signals.  
(2) TX Data In inputs must be at opposite logic levels during transmission, and at the same logic level when not transmitting.  
(3) LINE-TO-LINE output voltage is measured between TX Data Out and TX Data Out.  
(4) LINE-TO-LINE input voltage is measured on the Data Bus.

**FIGURE 2. TRANSCEIVER WAVEFORMS**

Dimensions are in inches (cm).



- Notes:  
(1) Metric equivalents are for general information only.  
(2) Lead identification numbers are for reference only.  
(3) Lead spacing dimensions apply only at seating plane.

**FIGURE 3. BUS-63105 AND 5962-86049 MECHANICAL OUTLINE**

**ORDERING INFORMATION**

5962-86049-01XX



# ISOLATION TRANSFORMERS



## DESCRIPTION AND APPLICATIONS

The military Data Bus Specification, MIL-STD-1553, has brought about the need for versatile pulse transformers that meet all the electrical requirements of Manchester II serial bi-phase data transmission. The BUS-25679, BUS-27765 and BUS-29854 provide all of the turns ratio configurations, component isolation and common mode rejection ratio characteristics necessary for MIL-STD-1553 A and B.

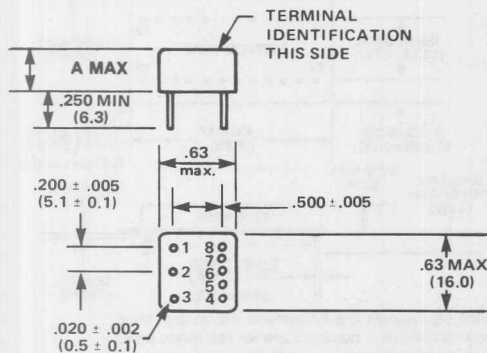
The step up and down ratios, available with these transformers, complement our entire product line and are com-

patible with competitive drivers, receivers and transceivers (contact the factory for details). The transformers are low profile, modular units that are multi-tapped to accommodate existing system configurations. They are encapsulated in accordance with MIL-T-21038. Their tin coated steel leads conveniently accommodate printed circuit board mounting. They accurately process sinusoidal or trapezoidal waveforms, in accordance with MIL-STD-1553 A and B and McDonnell Douglas specifications A-3818, A-5690, A-5232 and A-4905.

## FEATURES

- MANCHESTER II, BI-PHASE, 1MHz OPERATION
- FOR USE WITH MIL-STD-1553 A AND B AND MACAIR SPECIFICATIONS A-3818, A-5690, A-5232 AND A-4905
- 8 PIN, LOW PROFILE PACKAGE
- OPERATING TEMPERATURE: -55°C to +125°C

## MECHANICAL OUTLINE (BUS-25679, BUS-27765 & BUS-29854)



DIMENSION TABLE		
BUS-25679	BUS-27765	BUS-29854
A = 0.275 in. (7mm)	A = 0.300 in. (7.6mm)	A = 0.275 in. (7mm)

### Notes

1. Dimensions are maximums unless otherwise noted.
2. All dimensions are in inches (millimeters).
3. Pin callouts on bottom view are for reference only.

TURNS RATIO TABLE				
PRIMARY	SECONDARY	TURNS RATIO		
		BUS-25679	BUS-27765	BUS-29854
1, 3	4, 8	1.4 : 1	1 : 1	1 : 0.83
1, 3	5, 7	2 : 1	1 : .707 (1.4 : 1)	1 : 0.60

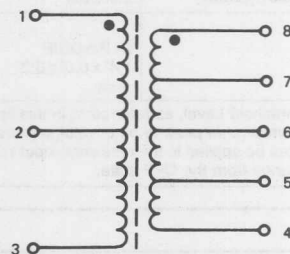


FIGURE 1. TURNS RATIO DIAGRAM

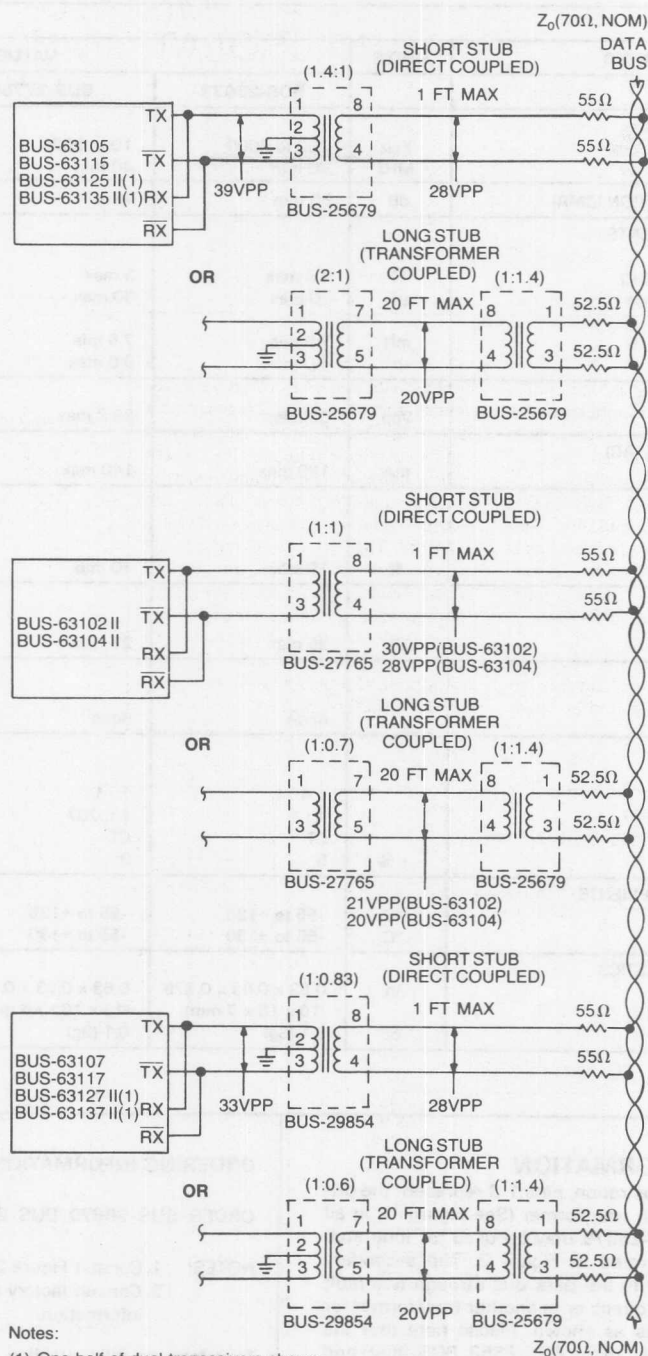


FIGURE 2. CONNECTION DIAGRAM

# BUS TRANSFORMERS

SPECIFICATIONS				
PARAMETER	UNITS	VALUE		
		BUS-25679	BUS-27765	BUS-29854
FREQUENCY RESPONSE				
Operating Range	KHz	250 to 3000	10 to 3000	250 to 3000
Self Resonance	MHz	40 min	40 min	40 min
COMMON MODE REJECTION (CMR)	dB	50 min	45 min	50 min
ELECTRICAL REQUIREMENTS				
Terminals 1, 3 & 4, 8				
Winding Resistance (RDC)	$\Omega$	1.5 max	3 max	1.9 max
Interwinding Capacitance	pF	70 max	30 max	70 max
Winding Inductance (LM)	mH	7.5 min	7.5 min	7.5 min
(LL)	uH	6.0 max	6.0 max	6.0 max
PEAK TO PEAK VOLTAGE				
Terminals 1, 3	Vpp	60 max	39.2 max	60 max
PEAK PULSE CURRENTS (AC)				
Terminals 1, 3 (primary)	mA	180 max	140 max	180 max
DROOP				
3 us Pulse Duration				
140 $\Omega$ Load Across				
Terminals 4-8	%	10 max	10 max	10 max
DECAY TIME				
140 $\Omega$ Load Across				
Terminals 4-8	ns	25 max	25 max	25 max
BACKSWING				
Across 140 $\Omega$ Load				
Terminals 4-8		none	none	none
URNS RATIOS				
Terminals				
1, 3 : 4, 8		1.4 : 1	1 : 1	1 : 0.83
1, 3 : 5, 7		2 : 1	1 : .707	1 : 0.60
2 : 6		CT	CT	CT
Winding Tolerance	$\pm$ %	5	3	5
TEMPERATURE REQUIREMENTS				
Operating (ambient)	$^{\circ}$ C	-55 to +125	-55 to +125	-55 to +125
Storage	$^{\circ}$ C	-55 to +130	-55 to +130	-55 to +130
PHYSICAL CHARACTERISTICS				
Size	in	0.63 x 0.63 x 0.275 (16 x 16 x 7 mm)	0.63 x 0.63 x 0.300 (16 x 16 x 7.6 mm)	0.63 x 0.63 x 0.275 (16 x 16 x 7 mm)
Weight	oz	0.1 (3g)	0.1 (3g)	0.1 (3g)

## TECHNICAL INFORMATION

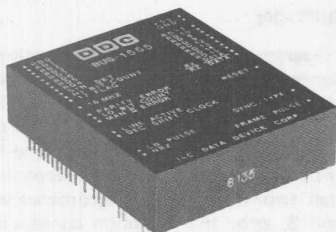
For the purpose of illustration, pins 1-3 represent the primary winding for each transformer (See Figure 1). In all applications the BUS-25679 may be used for long stub connections as illustrated in Figure 2. The secondary winding is connected to the Data Bus through two fault isolation resistors for direct, or to another transformer for long stub connections as shown. Please note that the transformers connected to the BUS-8553, BUS-8559 and BUS-63105 series transceivers require that their primary center tap winding be grounded.

## ORDERING INFORMATION

ORDER: BUS-25679, BUS-27765 or BUS-29854

NOTES: 1. Consult Figure 2 for correct unit for application.  
2. Consult factory for competitor cross reference information.

Transformers fully qualified to DESC Drawing No. 82030 are available. Consult factory for data sheet.



## MIL-STD-1553 MANCHESTER II DECODER FOR TEST EQUIPMENT

### FEATURES

- 16 MHz CLOCK RATE
- ERROR FLAGS FOR  
SYNC  
MANCHESTER II ERROR  
HIGH AND LOW BIT COUNT
- CONFORMS TO MIL-STD-1553  
A & B
- 16 BIT PARALLEL AND NRZ  
SERIAL OUTPUTS

### DESCRIPTION AND APPLICATIONS

Providing enhanced bit error capability and precise message error detection, the BUS-1555 Manchester II Decoder Module avails itself to a wide range of applications. The decoder is encapsulated in a 3.1 x 2.6 x 0.8 inch module and is compatible with receivers designed to meet MIL-STD-1553 A/B, DDC Models BUS-63105 and BUS-8559 are directly compatible with this decoder.

The BUS-1555 will sample Manchester II input data at 16 MHz, which improves bit recognition and overall system capability. Error flags are provided for low and high bit count, odd parity and Manchester II phasing errors. Control logic outputs include

Line Active, Frame, Sync Detector, Sync Type and Load Data Pulses. Internal logic may be initialized by means of the Reset Input function (see figure 1). The power supply input range is +4.5V to +5.5V and nominal power dissipation is 2.5 watts. The input is biphasc TTL complementary serial data, which is decoded and output as both 16 bit TTL parallel and NRZ serial data.

The BUS-1555 is well suited for use in MIL-STD-1553 test equipment and as a data bus monitor terminal where subsystem listening devices are used. Applications include both ground and on board avionics system.

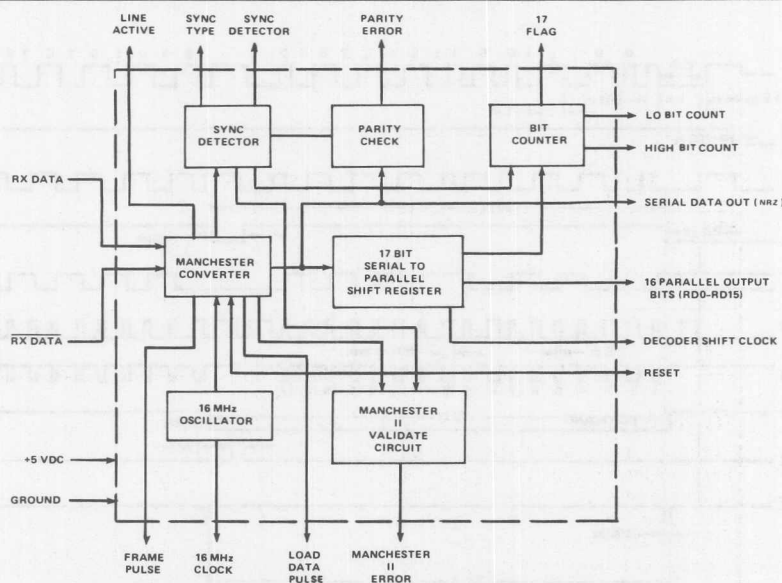


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS		
PARAMETER	UNITS	VALUE
<b>INTERNAL CLOCK OUTPUT</b>		
Oscillator Type	TTL	As per MIL-STD-1553B Long and short term stability
Frequency	MHz	16 $\pm$ 1000 Hz
Cross over variation	ns	$\pm$ 150
Drive capability	TTL	1 LS load
<b>DIGITAL IN/OUTPUTS</b>		
Serial Data Input	Bits	Complementary TTL bi-phase nonreturn zero, Manchester II format
	TTL	3 LS loads
<b>PARALLEL DATA</b>		
RDO-RD15	TTL	16 bit parallel positive logic (RD15 = MSB)
Drive Capability		8 LS loads (RDO-RD15 each)
Decoder Shift Clock Output	TTL	Synchronous output with respect to serial NRZ data output
Drive Capability	TTL	1 LS load
Control Logic	TTL	See pin connection for fan in/out and loading specifications
<b>POWER SUPPLY CHARACTERISTICS</b>		
Voltage Input Range	V	+4.5 to 5.5
Current	A	0.5 max @ +5V nominal
<b>TEMPERATURE RANGE</b>		
Operating	$^{\circ}$ C	0 to +70
Storage	$^{\circ}$ C	-55 $^{\circ}$ C to +125 $^{\circ}$ C
<b>PHYSICAL CHARACTERISTICS</b>		
Size	in.	3.1 x 2.6 x 0.8 (78 x 66 x 20mm)
Weight	oz	6 (170g)

Figure 1 is a block diagram of the BUS-1555, illustrating its functions of Manchester decoding, sync detection, serial to parallel conversion, and validation of MIL-STD-1553 Manchester coding, sync, parity and bit count. Use of a 16 MHz clock to sample the complementary (RX and RX) biphas Manchester data results in improved bit recognition and enhanced overall error detection. In accordance with MIL-STD-1553A and B, error free reception consists of a 20  $\mu$ sec word, with a 3  $\mu$ sec sync field, followed by a 16  $\mu$ sec data field, followed by a 1  $\mu$ sec parity bit. In addition, the sync field must be 2 equal 1.5  $\mu$ sec halves, and the data field and parity bit must be valid Manchester coding.

The error detection sequence starts with recognition of a valid (command or data) sync (figure 2), and ends with a BUS-1555 Load Data output pulse. Activity on error flag outputs is to be ignored except during the Load Data pulse interval. Upon receipt of a valid sync, the Sync Detect line goes high and the Frame Pulse Line is pulsed. After a valid sync, the next data bit time (1  $\mu$ sec) is checked for a valid Manchester transition. If a Manchester error has occurred in the first data bit, the Manchester error flag is activated, the low bit count error flag is inhibited, and a Load Data pulse is generated at the end of the frame. If the first data bit passes the Manchester test, the remaining 16 bits are checked for Manchester, bit count and parity.

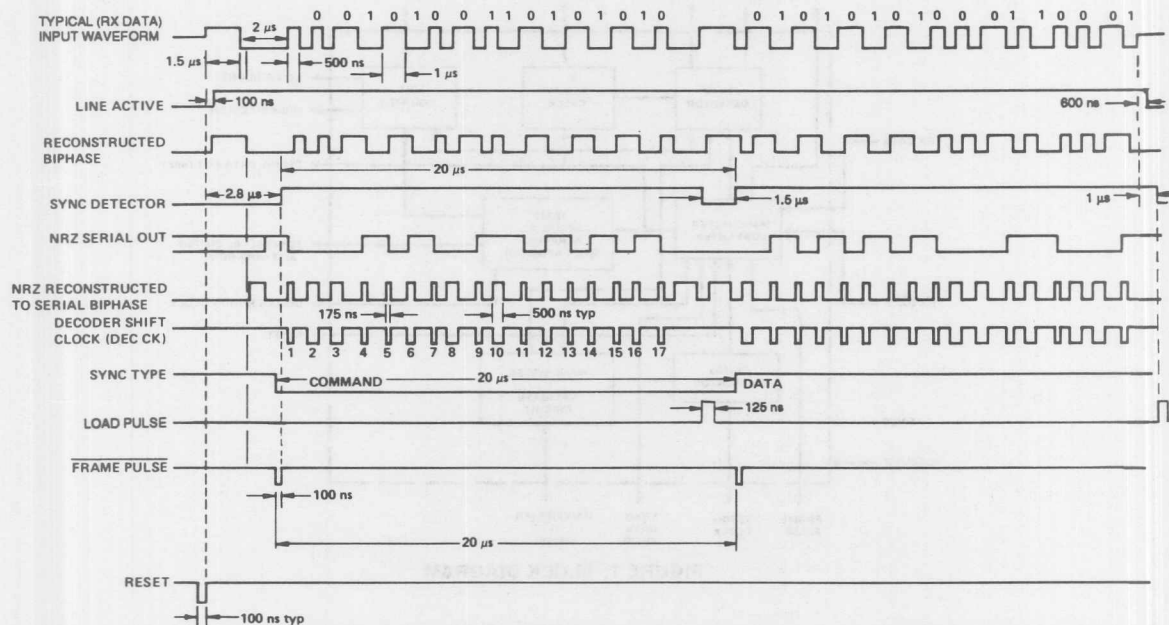


FIGURE 2. DECODER TIMING DIAGRAM



## Pin Function Table

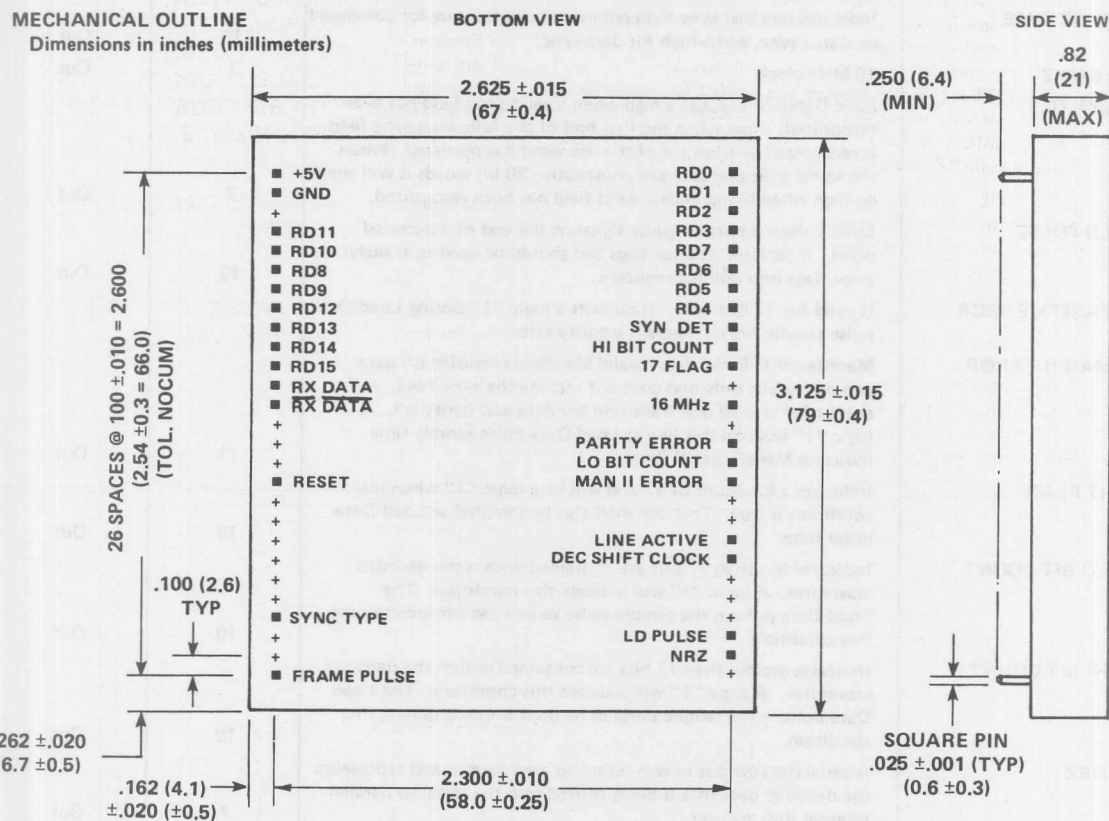
PIN	DESCRIPTION	LOADING	FAN IN/OUT
RX DATA	Receiver Data (TTL)	3	In
RX DATA	Receiver Data (TTL)	3	In
LINE ACTIVE	Monitors the data bus data and interprets valid activity. The output goes high when a valid sync on both RX and RX inputs is identified. It remains high if successive words are received and will go low 750 nanoseconds after the last bit of a valid word.	6	Out
FRAME PULSE	Identifies when a valid sync field has been detected and its trailing edge is coincident with the positive going edge of the SYN DET output.	6	Out
SYNC TYPE	Indicates received sync field polarity, outputs a low for command or status sync, and a high for data sync.	10	Out
16 MHZ	16 MHz clock	1	Out
SYN DET	Sync Detector outputs a high when a valid sync field has been recognized, a low when the first half of the following sync field is recognized or a last bit of the last word has occurred. When the signal goes low between consecutive 20 bit words it will again go high when the complete valid field has been recognized.	7	Out
LD PULSE	Load pulse is a positive pulse signaling the end of a decoded word. It samples all error flags and should be used to transfer error flags into holding registers.	10	Out
PARITY ERROR	Is valid for 17 bits only. It outputs a logic "1" during Load Data pulse sample time, if there is a parity error.		
MAN II ERROR	Manchester II Error flags invalid Manchester coding on data and parity bits only and does not include the sync field. It checks for at least one transition per data and parity bit. A logic "1" level on this line at Load Data pulse sample time indicates Manchester II Error.	10	Out
17 FLAG	Indicates a bit count of 17 and will be a logic "1" when this condition is true. This line shall also be sampled at Load Data pulse time.	10	Out
LO BIT COUNT	Indicates less than 17 bits are contained within the decoded waveform. A logic "1" will indicate this condition. The Load Data pulse is the sample pulse to be used for ascertaining this condition.	10	Out
HI BIT COUNT	Indicates greater than 17 bits are contained within the decoded waveform. A logic "1" will indicate this condition. The Load Data pulse is the sample pulse to be used for ascertaining this condition.	10	Out
NRZ	Is serial data output in non-return to zero format and represents the decoded data that is being shifted into the serial to parallel internal shift register.	7	Out
RD0-RD15	Parallel Data Out consists of 16 bits referred to as RD0-RD15, with RD15 being MSB. This is not latched data and is valid only if 17 bits are sent and all validation checks pass. Data shall be sampled at the Load Data pulse time.	8	Out
DEC SHIFT CLK	Decoder Shift Clock is the "sync'd clock line output for the serial data out (NRZ). There will be a maximum number of 17 clock pulses out on this line regardless if greater than 17 bits are sent and detected. For less than 17 bits the number of clock pulses resulting on this line will be equal to the number of bits sent.	1	Out
RESET	Reset pulse is an active low signal that resets the module.	1	In

A Manchester error at any bit time takes highest priority. It causes the low bit count error flag to be inhibited, the Manchester error flag to be activated, and a Load Data pulse to appear at the end of the frame.

It is to be noted that the BUS-1555 continues to monitor the input for valid sync after the error checking sequence has begun. As a result of this this, a bit time ending with no Manchester transition present, and 1.5  $\mu$ sec elapsed since the last Manchester transition, will be interpreted as half of a sync field. Under these conditions the bit counter will

not be incremented, and if the second half of the sync field doesn't occur, a low bit count error flag will result. If a bit time ends with no Manchester transition present, and 1.0  $\mu$ sec elapsed since the last Manchester transition, a Manchester error flag will result.

The valid word indicator is referred to as the 17 flag. This flag is activated when there are 16 data bits plus 1 parity bit valid Manchester transitions. The Parity Error flag is only valid when the 17 flag has been activated.



## ORDERING INFORMATION

BUS-1555



## MIL-STD-1553 ENCODER Generates Errors For Test Equipment

### FEATURES

- ENCODES PARALLEL DATA INTO SERIAL MANCHESTER
- ERROR GENERATION CAPABILITY:  
MANCHESTER CODING ERROR  
PARITY ERROR  
HIGH BIT COUNT ERROR  
LOW BIT COUNT ERROR  
SYNC FIELD ERROR
- CONFORMS TO MIL-STD-1553 A AND B
- USED IN TEST SYSTEMS WITH BUS-1555 DECODER

### DESCRIPTION

The BUS-1556 MIL-STD-1553 Encoder is a versatile building block, featuring capability for generating a number of different error types. The Manchester encoder is encapsulated in a 3.1 x 2.6 x 0.8 inch module and is compatible with transmitters designed to meet MIL-STD-1553 A/B. (DDC models BUS-63105 and BUS-8559).

The BUS-1556 converts 16-bit parallel input data to a Manchester II encoded serial output. All timing is derived from an externally supplied 2 MHz clock. The encoder outputs error-free data words or it may be pin programmed to output words containing one or more encoding errors. The errors generated by the BUS-1556 include Manchester II error in any of the 16 data bits, and parity bit positions; parity error, long word (one

extra bit) error, short word (one missing bit) error, and two different forms of sync field errors.

A Master Reset pin for initialization, an Encoder Enable input, an Encoder Active and T Load outputs are provided for handshaking with a parallel subsystem. Complementary bi-phase serial data output is provided via the TX DATA and TX DATA pins. The power supply input range is +4.5 V to +5.5 V and nominal power dissipation is 2.5 watts.

### APPLICATIONS

The BUS-1556 is intended for use in test fixtures as well as in Automatic Test Equipment (ATE) for testing MIL-STD-1553 A/B monitors, bus controllers and remote terminals. Applications include both ground support and on-board avionics systems.

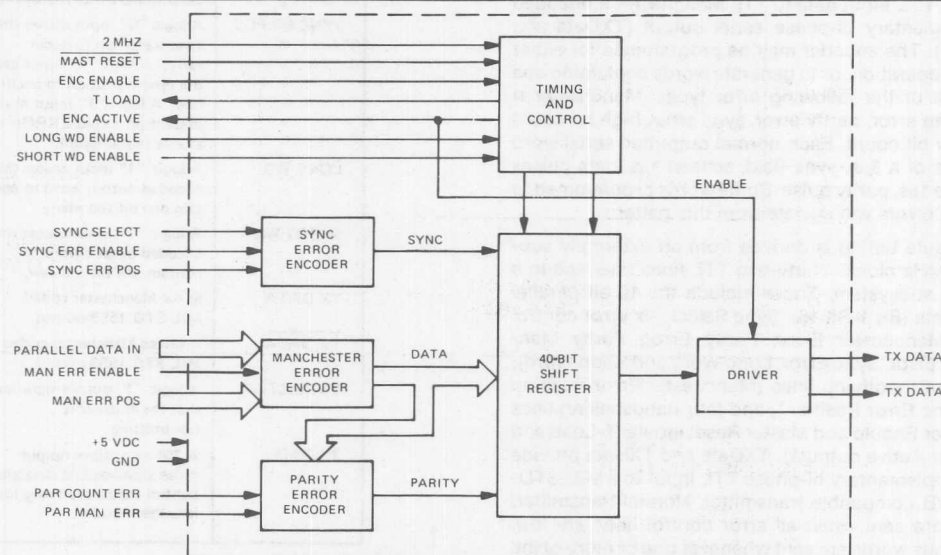


FIGURE 1. BUS-1556 BLOCK DIAGRAM

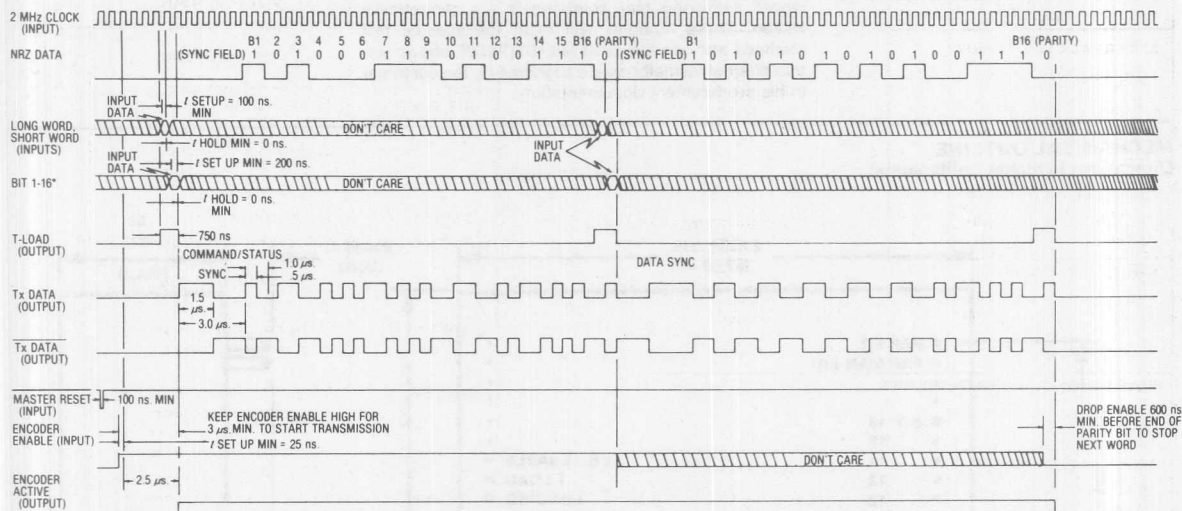
	UNITS	VALUE
<b>EXTERNAL CLOCK INPUT</b>		
Oscillator Type (2 MHz)	TTL	As per MIL-STD-1553 A/B long and short term stability requirements
Frequency	MHz	2.000 ± .001
Crossover Variation	ns	± 150
Loading		1 LS TTL load
<b>PARALLEL DATA INPUT</b>		
Bit 1 (MSB)-Bit 15 (LSB)	TTL	16-bit parallel positive logic
Loading		2 LS TTL loads
<b>SERIAL DATA OUTPUT</b>		
TX DATA and TX DATA	TTL	Complementary TTL Manchester bi-phase II format
Fan-Out		5 Standard TTL loads
<b>POWER SUPPLY CHARACTERISTICS</b>		
Voltage Input Range	V	+4.5 to +5.5
Current	A	0.65 max., 0.4 typ
<b>TEMPERATURE RANGE</b>		
Operating	°C	0 to + 70
Storage	°C	-55 to + 125
<b>PHYSICAL CHARACTERISTICS</b>		
Size	in	3.1 x 2.6 x 0.8 (78x66x20mm)
Weight	oz	6 (170g)

## TECHNICAL INFORMATION

The BUS-1556 error-generating encoder operates in accordance with MIL-STD-1553 A/B to convert 16 bit parallel TTL input data to TTL Manchester II encoded complementary bi-phase serial output (TXData and TXData). The encoder may be programmed for either normal operation, or to generate words containing one or more of the following error types: Manchester II encoding error, parity error, sync error, high bit count and low bit count. Each normal outputted serial word consists of a 3µs. sync field, sixteen 1µs. data pulses and one 1µs. parity pulse. Some words programmed to contain errors will deviate from this pattern.

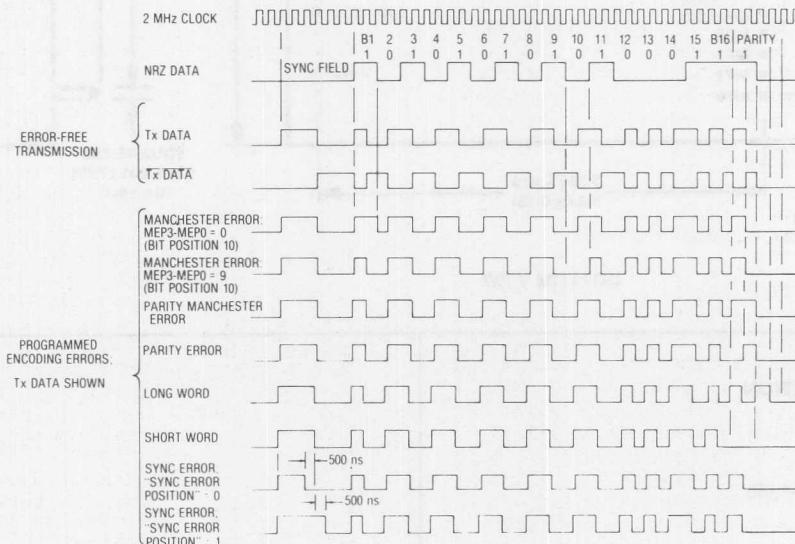
All module timing is derived from an externally supplied 2MHz clock. Thirty-two TTL lines interface to a parallel subsystem. These include the 16 bit parallel input data (Bit 1-Bit 16), Sync Select, six error control lines (Manchester Error, Parity Error, Parity Manchester Error, Sync Error, Long Word and Short Word), five error modifying lines (Manchester Error Position 0-3, Sync Error Position), and four handshaking lines (Encoder Enable and Master Reset inputs; T-Load and Encoder Active outputs). TXData and TXData provide the complementary bi-phase TTL input to a MIL-STD-1553 A/B compatible transmitter. Normal transmitted words are sent when all error control lines are low. Erroneous words are sent whenever one or more of the error control lines are asserted high.

PIN	DESCRIPTION	LS LOADS
BIT 1-BIT 16	Parallel data inputs.	2
SYNC SELECT	A logic "1" input causes a Command/Status sync output. A logic "0" input causes a Data sync output.	4
2 MHZ	2MHz clock input.	1
ENC ENABLE	A 3 µsec minimum duration logic "1" input enables the start of a MIL-STD-1553 encoded output word.	1
MAST RESET	A 100 nsec active low pulse input resets all encoder circuits.	1
MAN ER	A logic "1" input enables the generation of Manchester errors. The bit position of the error is determined by MP0-MP3.	2
MP0-MP3	Binary coded input representing the desired bit position of the Manchester error. A logic "1" input must be present on MAN ER to enable the function.	1
PAR ER	A logic "1" input causes a parity count error.	1
PAR MAN ER	A logic "1" input causes the Manchester error in the parity bit.	1
SYNC ERROR	A logic "1" input enables the generation of a sync error. The position of the error is determined by SYNC ER POS.	2
SYNC ER POS	A logic "0" input causes the sync transition to occur early. A logic "1" input causes the sync transition to occur late. A logic "1" input must be present on SYNC ERROR to enable the function.	2
LONG WD	A logic "1" input causes the encoded output word to contain one bit too many.	2
SHORT WD	A logic "1" input causes the encoded output word to contain one bit too few.	1
TX DATA	Serial Manchester coded MIL-STD-1553 output.	10
TX DATA	Inverted Manchester coded MIL-STD-1553 output.	10
ENC ACTIVE	A logic "1" output signifies that the encoder is transmitting.	7
T LOAD	A 750 ns positive output pulse signifies that data and control inputs are being loaded into the encoder.	10



**FIGURE 2. ENCODER TIMING DIAGRAM**

\*SYNC SELECT, SYNC ERROR, SYNC ERROR POSITION, MANCHESTER ERROR, MEP0-3, PARITY ERROR, PARITY MANCHESTER ERROR INPUTS ARE EXECUTED BETWEEN BIT TIMES 1-16



**FIGURE 3. ENCODING ERRORS**

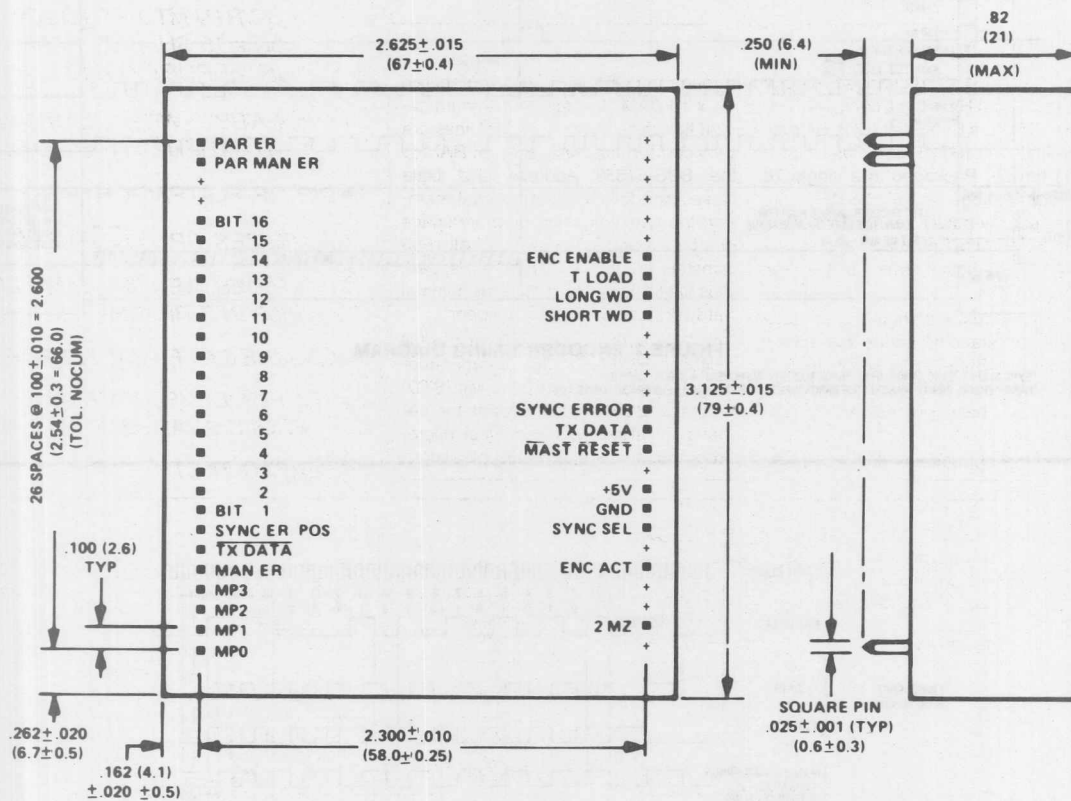


## TEST METHODS

BUS-1556 converter modules are high quality products whose semiconductor components are hermetically sealed. These modules will meet the specific test methods and conditions of MIL-STD-202E shown unless alternative methods are specified by the customer in his procurement documentation.

## MECHANICAL OUTLINE

Dimensions in inches (millimeters)

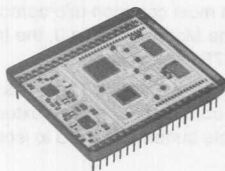


**BOTTOM VIEW**

## ORDERING INFORMATION

BUS-1556

## MIL-STD-1553 ADVANCED INTEGRATED MUX (AIM) HYBRID



**SEE ALSO  
USER'S GUIDE**

### FEATURES

- **COMPLETE INTEGRATED MUX INCLUDING:**
  - LOW POWER DUAL TRANSCEIVER
  - BC/RTU/MT PROTOCOL
  - 8K x 16 SHARED RAM
  - INTERRUPT LOGIC
- **COMPATIBLE WITH MIL-STD-1750 AND OTHER STANDARD CPUs**
- **DIP OR FLATPACK HYBRID**
- **MINIMIZES CPU OVERHEAD**
- **PROVIDES MEMORY MAPPED 1553 INTERFACE**
- **ON-LINE & OFF-LINE SELF-TEST**
- **IBM PC® DEVELOPMENT TOOLS AVAILABLE**
- **SEAFAC TESTED**

### DESCRIPTION

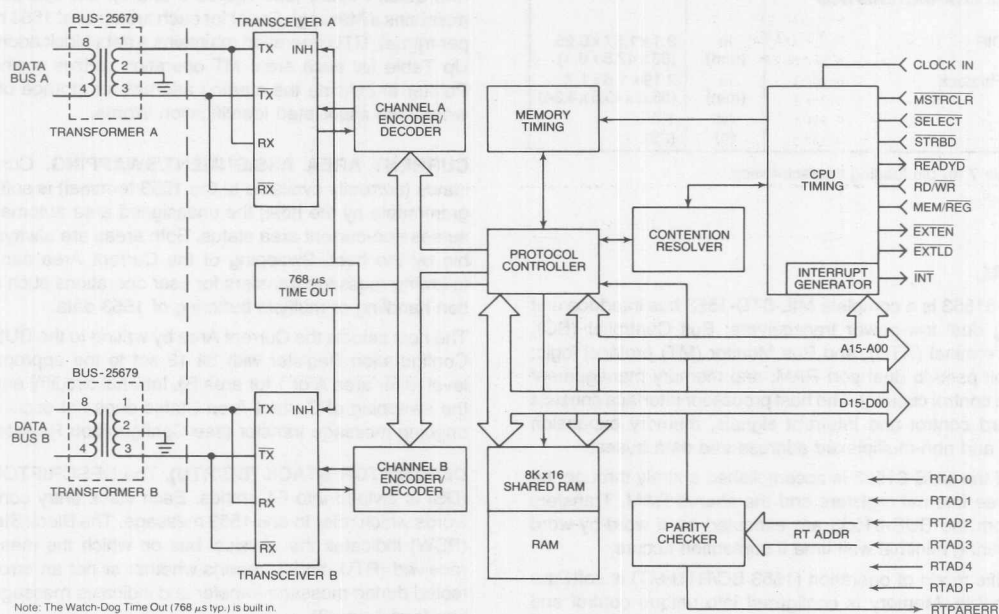
DDC's BUS-61553 Advanced Integrated Mux (AIM) Hybrid is a complete MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor (MT) device. Packaged in a single 78 pin DIP package, the BUS-61553 contains dual low-power transceivers, complete BC/RTU/MT protocol logic, a MIL-STD-1553-to-host interface unit and an 8K x 16 RAM.

Using an industry standard dual transceiver and standard status and control signals, the BUS-61553 simplifies system integration at both the MIL-STD-1553 and host processor interface levels.

All 1553 operations are controlled

through the CPU access to the shared 8K x 16 RAM. To ensure maximum design flexibility, memory control lines are provided for attaching external RAM to the BUS-61553 Address and Data Buses and for disabling internal memory; the total combined memory space can be expanded to 64K x 16. All 1553 transfers are entirely memory-mapped; thus the CPU interface requires minimal hardware and/or software support.

The BUS-61553 operates over the full military -55°C to +125°C temperature range. Available screened to MIL-STD-883, the BUS-61553 is ideal for demanding military and industrial micro-processor to 1553 interface applications.



Note: The Watch-Dog Time Out (768 μs typ.) is built in.

FIGURE 1. BUS-61553 BLOCK DIAGRAM

TABLE 1. BUS-61553 SPECIFICATIONS

Specifications at nominal power supply voltages.		
PARAMETER	VALUE	NOTES
<b>RECEIVER</b>		
Differential Input Voltage	$V_{p-p}$	40 max
Differential Input Impedance	K Ohms	7 min
CMRR	dB	40 min
<b>TRANSMITTER (Direct Coupled)</b>		
Differential Output Voltage	$V_{p-p}$	6.0 min, 9.0 max
Output Rise and Fall Times	n sec	100 min, 300 max
Output Offset Voltage	mV	±90 max
<b>LOGIC*</b>		
$V_{IH}$	V	2.2 min
$V_{IL}$	V	0.8 max
<b>CLOCK</b>	MHz	16
<b>POWER SUPPLIES</b>		
+5V (Logic)	V	+5±5%
-15VA (Chan A Transceiver)	V	-15±10%
-15VB (Chan B Transceiver)	V	-15±10%
+5VA (Chan A)	V	+5±5%
+5VB (Chan B)	V	+5±5%
Current Drain* (Total Package)		(Typ)/max
+5V (Idle)	mA	(85)/170
-15V (Idle)	mA	(45)/80
+5V (25% Duty Cycle)	mA	(85)/170
-15V (25% Duty Cycle)	mA	(80)/130
<b>TEMPERATURE RANGE</b>		
Operating (Case)	°C	-55 to +125
Storage	°C	-65 to +150
<b>PHYSICAL CHARACTERISTICS</b>		
Size		
78 pin DIP	in (mm)	2.1 x 1.87 x 0.25 (53 x 47.5 x 6.4)
82 pin Flatpack	in (mm)	2.19 x 1.6 x 1.7 (55.6 x 40.6 x 4.34)
Weight	oz (g)	1.0 (29)

\* See Table 7 for pin loading characteristics.

## GENERAL

The BUS-61553 is a complete MIL-STD-1553 bus interface unit containing dual low-power transceivers; Bus Controller (BC), Remote Terminal (RTU), and Bus Monitor (MT) protocol logic; 8K x 16-bit pseudo dual port RAM; and memory management arbitration control circuitry. The host processor interface consists of standard control and interrupt signals, memory expansion capability and non-multiplexed address and data buses.

Control of the BUS-61553 is accomplished entirely through the use of three internal registers and the shared RAM. Transfers to and from the BUS-61553 are executed on a word-by-word basis ensuring minimal wait time if contention occurs.

The specific mode of operation (1553 BC/RTU/MT) is software programmable. Memory is configured into unique control and data block areas based on the 1553 mode of operation. External registers are also supported by the BUS-61553 for manipulation of user data. In addition, the BUS-61553 provides dynamic, on-line and software initiated self-test capabilities.

## INTERFACING

The BUS-61553 is compatible with most common microprocessors including, but not limited to, the Motorola 680 x 0, the Intel 808x, Zilog Z800x and MIL-STD-1750 processors.

Interfacing the BUS-61553 to the MIL-STD-1553 Data Bus requires two DDC BUS-25679 pulse transformers and an external 16 MHz clock (see figure 2). Tri-state buffers are used to isolate the CPU's data and address lines.

External RAM can be used instead of or in conjunction with the BUS-61553's internal 8K x 16 bits. The external RAM used by the BUS-61553 can be any standard static memory with an access time of ≤55ns. The RAM can be expanded to 64 x 16.

Two control signals, MEMENA-IN (pin 69) and MEMENA-OUT (pin 31) are provided in addition to the standard memory I/O signals for internal/external memory access control (see figures 3-5). MEMENA-OUT and MEMENA-IN should be tied together for Internal Memory Only configuration. Memory CS signals can be generated for configurations using external memory.

## MEMORY MANAGEMENT

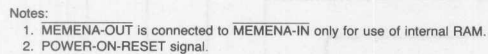
Memory can be configured to support two AREAs (A and B), each with an independent sequential stack and pointers for manipulating 1553 message and control data. The CPU can access the shared RAM while 1553 message transfers are taking place. Arbitration of the RAM is automatically implemented in a manner transparent to the subsystem (see figures 28-31). Variable length DATA BLOCKS are also stored in the shared RAM and can be addressed by setting pointers residing in Area A, Area B or both. For BC/RTU operation, each area contains a Descriptor Stack and Stack Pointer (see figures 6 and 7). BC operation further maintains a Message Count for each area (no. of 1553 messages per frame). RTU operation maintains a data block address Look-Up Table for each area. MT operation utilizes a single Stack Pointer to indicate the starting address for storage of received words and associated Identification Words.

**CURRENT AREA ASSIGNMENT/SWAPPING.** Current area status (currently available to the 1553 terminal) is software programmable by the host; the unassigned area automatically assumes non-current area status. Both areas are always accessible by the host. Swapping of the Current Area can be done following message transfers for user operations such as exception handling or multiple buffering of 1553 data.

The host selects the Current Area by writing to the BUS-61553's Configuration Register with bit 13 set to the appropriate logic level (0 for area A or 1 for area B). Internal circuitry ensures that the swapping of Current Area Status does not occur during an ongoing message transfer (see Configuration Register).

**DESCRIPTOR STACK (BC/RTU).** The DESCRIPTOR STACK (DS) is divided into 64 entries. Each stack entry contains four words which refer to one 1553 message. The Block Status Word (BSW) indicates the physical bus on which the message was received (RTU mode), reports whether or not an error was detected during message transfer and indicates message completion (see figure 8).

The user-supplied Time Tag word is loaded at the start of a message transfer and is updated at the end of the transfer (see Time Tagging).



**FIGURE 2. BUS-61553 EXAMPLE INTERCONNECTION**

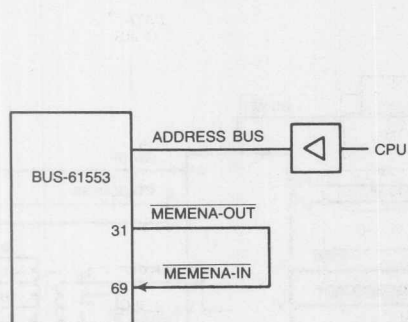


FIGURE 3. INTERNAL MEMORY ONLY

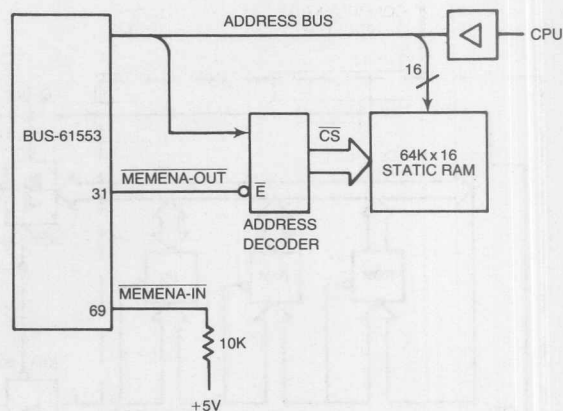


FIGURE 4. EXTERNAL MEMORY ONLY

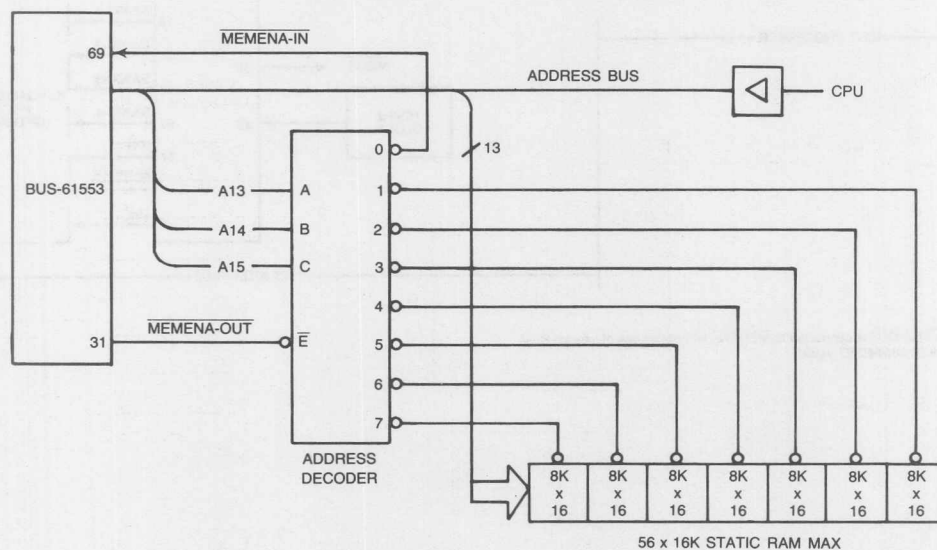
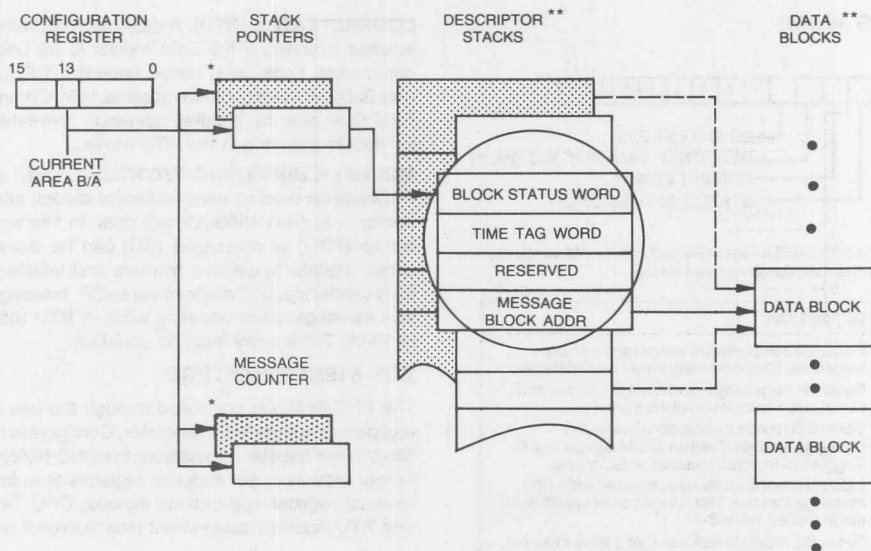


FIGURE 5. CONFIGURATION USING BOTH INTERNAL & EXTERNAL MEMORY

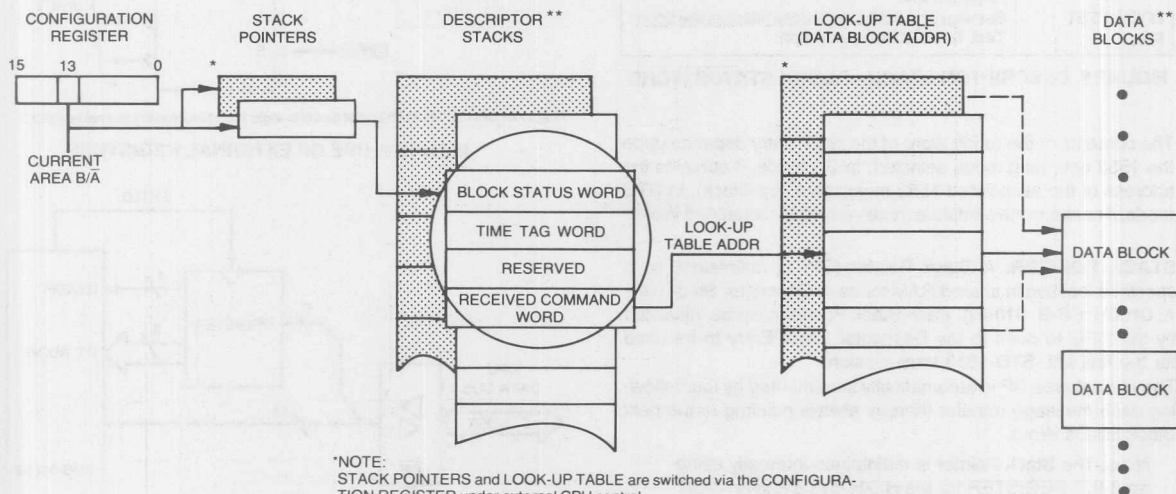




\*NOTE:  
STACK POINTERS and MESSAGE COUNTERS are switched via the CONFIGURATION REGISTER under external CPU control.

\*\*NOTE:  
DESCRIPTOR STACKS and DATA BLOCKS have 256 word boundaries which should be observed.

**FIGURE 6. USE OF DESCRIPTOR STACK – BC MODE**

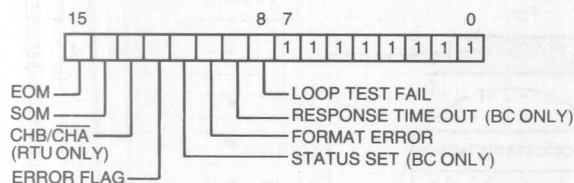


\*NOTE:  
STACK POINTERS and LOOK-UP TABLE are switched via the CONFIGURATION REGISTER under external CPU control.

\*\*NOTE:  
DESCRIPTOR STACKS and DATA BLOCKS have 256 word boundaries which should be observed.

**FIGURE 7. USE OF DESCRIPTOR STACK – RTU MODE**

## BLOCK STATUS WORD



Note: In BC operation, the BUS-61553 always writes the BSW to RAM with Bit-13, CHB/CHA toggles as per the message control word setting.

BIT NAME	DEFINITION
EOM	Set at the completion of a message transfer regardless of whether any errors were detected.
SOM	Set at the beginning of a message transfer and Reset upon completion of the transfer.
CHB/CHA	Set in RTU mode to indicate whether the message was received on 1553 bus A or bus B. Toggles to indicate channel, in BC mode.
ERROR FLAG	Indicates that an error was detected within the message transfer. The specific error condition(s) are identified in bits 8-11.
STATUS SET	Set in BC mode to indicate that a status flag bit was set within the received RTU Status Word or that the RTU address did not match the associated Command. Set in BC mode when the message error bit is set within the received RTU Status Word.
FORMAT ERROR	Also set in RTU mode (RT-RT transfer; BUS-61553 is acting as the receiving RT) when the transmitting RTU Status Word contains an incorrect address. Also, set in BC or RTU mode if the message violates MIL-STD-1553 (parity, Manchester, sync bit count, non-contiguous data or word count errors).
RESPONSE TIMEOUT	Set in BC mode if the addressed RTU did not respond within 14 $\mu$ s. Also set when acting as a receiving RT (RT-RT transfer) if the transmitting RT does not respond in the specified 1553 response time.
LOOP TEST FAIL	Set when the BUS-61553 does not pass the Loop Test. See Self Test paragraph.

FIGURE 8. DESCRIPTOR STACK - BLOCK STATUS WORD

The contents of the fourth word of the stack entry depends upon the 1553 operating mode selected. In BC mode, it contains the address of the associated 1553 message (Data Block). In RTU mode, it contains the complete (received) 1553 Command Word.

**STACK POINTER.** A Stack Pointer (SP) is maintained at a specified location in shared RAM for each Descriptor Stack (SP-A: 0100H; SP-B: 0104H). Each Stack Pointer must be initialized by the CPU to point to the Descriptor Stack Entry to be used for the first MIL-STD-1553 transmission.

The current area SP is automatically incremented by four following each message transfer thereby always pointing to the next Block Status Word.

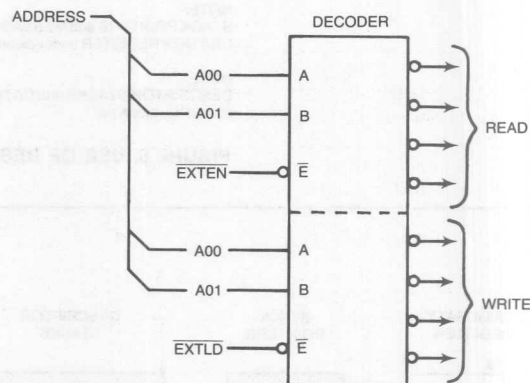
Note: The Stack Pointer is maintained internally using an 8-BIT REGISTER for the HIGH BYTE and an 8-BIT COUNTER for the LOW BYTE. The high byte remains constant (user value) while the low byte will wrap around from FF(H) to 00(H). For example: a current Stack Pointer value of 00 FF(H) will increment to 00 00(H) and not 01 00(H).

**LOOK-UP TABLE (RTU).** A data block address Look-Up Table is used to indicate the data blocks to be used for individual commands. Look-Up is based upon the T/R (transmit/receive) and Subaddress bits of the received 1553 Command Word. See RTU Operation for detailed operation; two tables are provided for double buffering in the RTU mode.

**MULTIPLE BUFFERING (BC/RTU).** Unused areas of shared RAM can be used to store additional stacks, tables, data blocks and/or user (non 1553-related) data. In this way, multiple data blocks (RTU) or messages (BC) can be stored for later use: simply update respective pointers and initiate the appropriate start conditions. (BC mode requires SP, message block address and message count updating while in RTU mode, the SP and Look-Up Table entry must be updated).

## BUS-61553 REGISTERS

The BUS-61553 is controlled through the use of three internal registers: Interrupt Mask Register, Configuration Register and a Start/Reset register. In addition, the BUS-61553 can access up to four external, user supplied registers (see table 2). Possible external register applications include: CPU Time Tag storage and RTU Address assignment (see figures 9 and 10).



Note: A02 of the BUS-61553 must be set to logic 1 to operate with external registers.

FIGURE 9. USE OF EXTERNAL REGISTERS

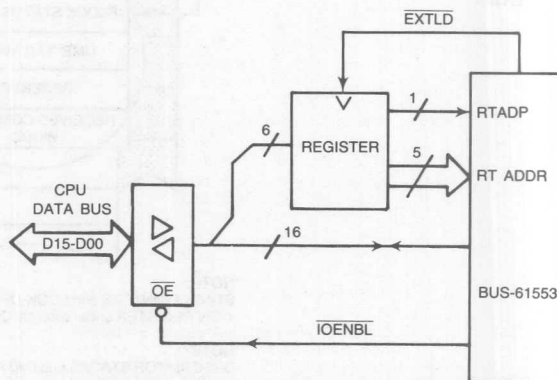
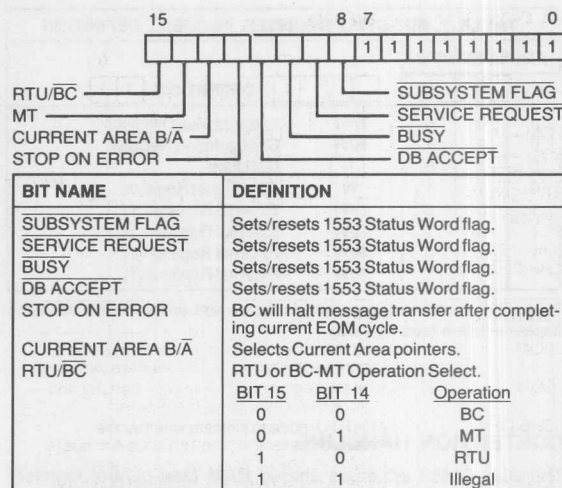


FIGURE 10. EXAMPLE CONFIGURATION USING EXTERNAL REGISTERS

**CPU TO REGISTER OPERATIONS.** The CPU selects a register by asserting MEM/REG low and A2 to a logic 0 (for internal registers) or logic 1 (for external registers) with A0 and A1 indicating the appropriate register address (see figures 28-32). The signals EXTEN and EXTLD are used to access the external registers.

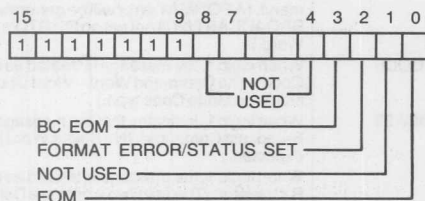
**CONFIGURATION REGISTER.** The Configuration Register is a 16-bit read/write register used to define the 1553 operating mode (BC, RTU, or MT); define selectable 1553 Status Word bits (RTU only); select stop-on-error option; and support the double buffering scheme (see figure 11).



Note: A logic 0 causes the corresponding bit within the RTU's status word to be set to a logic 1.

FIGURE 11. CONFIGURATION REGISTER

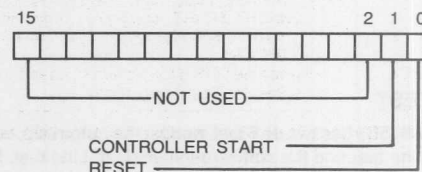
**INTERRUPT MASK REGISTER (BC/RTU).** This register is a 16-bit read/write register used to enable/mask interrupt conditions. If an interrupt condition occurs and the corresponding Interrupt Register bit has been enabled (set to logic 1) pin 72, INT will be pulsed low during the respective End of Message (EOM) cycle (see figure 12). Not Used bit locations can optionally be used for storing user flags.



INTERRUPT	DEFINITION
EOM	End of message. Set by BUS-61553 in BC or RTU mode following each 1553 transfer (regardless of validity).
FORMAT ERROR/STATUS SET	Set if one of the following occurs: <b>Loop Test Failure:</b> Received word does not match last word transmitted. <b>Message Error:</b> Received message contained a violation of any of the 1553 message validation criteria (parity, sync, Manchester encoding, bit/word count, etc.). <b>Time-Out:</b> Expected transmission was not received during the allotted time. <b>Status Set:</b> Received Status Word contained status bit(s) set or address error.
BC EOM	Bus Controller End of Message. Set by the BUS-61553 following transmission of all messages within the current Message Block. (Current area message count = FFFF).

FIGURE 12. INTERRUPT MASK REGISTER

**START/RESET REGISTER.** This write-only register is used to reset the BUS-61553 and to start the BC and MT operations, as illustrated in figure 13.



	BIT 1	BIT 0
START	1	0
RESET	0	1

BIT NAME	DEFINITION
CONTROLLER START	Issued by the CPU to start message block transmission (BC Operation) or to begin reception of 1553 messages (MT Operation).
RESET	Issued by the CPU to place the BUS-61553 in the power-on condition; (1) aborts 1553 transfers currently in progress, and (2) resets Configuration and Interrupt Mask Register bits (logic 0).

FIGURE 13. START/RESET REGISTER

TABLE 2. BUS-61553 REGISTER ADDRESS DEFINITION

ADDRESS BITS			DEFINITION	
A2	A1	A0		
0	0	0	R/W	Interrupt Mask Register
0	0	1	R/W	Configuration Register
0	1	0	—	Not Used
0	1	1	W	Start/Reset Register
1	0	0	R/W	External Register (1)
1	0	1	R/W	External Register (1)
1	1	0	R/W	External Register (1)
1	1	1	R/W	External Register (1)

Note: R/W (read/write) capability is dependent on the user's decoding implementation (see figure 9).

## CONTENTION HANDLING

The BUS-61553 arbitrates shared RAM (and control register) accesses between the host CPU and the internal 1553 protocol logic.

If the host attempts to access the RAM while an internal 1553 memory cycle is in progress, the BUS-61553 will delay the CPU's memory cycle by inserting wait states via the **READYD** control signal until the cycle has been completed. The maximum delay is 1.8  $\mu$ s.

If the internal 1553 protocol logic attempts to access the RAM while the host CPU has control of the memory, the internal 1553 logic will wait until the host CPU cycle has been completed. To ensure the integrity of 1553 data transfers, the host CPU must complete its memory cycle within 1.5  $\mu$ s (see figures 28-32).

## SELF TEST

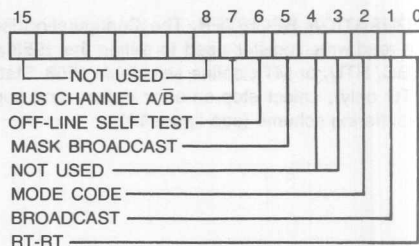
The BUS-61553 has two self-test modes: the automatic, continuous On-Line test and the software-initiated Off-Line test. In both tests the Loop Test Fail bit within the Block Status Word will be set to a logic 1 if a failure is detected.

**ON-LINE TEST.** The On-Line test occurs in BC and RTU modes during transmission of each message onto the 1553 bus. This test wraps around the last word transmitted, exercising the 1553 protocol logic through the 1553 transceivers.

While operating as a BC, the last word transmitted is received, decoded, and written back into memory location immediately following the last word within the message block. The host CPU can read and compare this Loop Back Word with the last word of the message Data Block; these two words should be identical. This insures data integrity between the CPU and the BUS-61553.

While in the RTU mode, the internal 1553 Status Word will be updated to reflect the result of the self test. The Status Word's Terminal Flag bit will be set to a logic 1 if a fault was indicated by the wrap-around, self-test.

**OFF-LINE TEST.** The software-initiated Off-Line test can be executed only when the BUS-61553 is configured as a BC. Set the Wrap-Around Test bit within the BC Control Word to a logic 1 and initiate any standard message transfer. This inhibits the 1553 transceivers and initiates the standard wrap-around test (i.e., internal 1553 encoder output is fed back into the decoder — the word is then written into memory). See BC Operation and Figure 14, BC Control Word for more detail.



BIT NAME	DEFINITION
BUS CHANNEL A/B	Determines whether the message will be transmitted on 1553 Bus A or Bus B. Logic 1 = A, logic 0 = B.
INITIATE OFF-LINE SELF TEST	Logic 1 performs internal off-line transmit/receive test. The last word of the message is looped back through the decoder and placed in RAM. See Self Test paragraph.
MASK BROADCAST (1)	When logic 1, prevents Broadcast RCVD bit of the 1553 Status Word response from signalling a status error as a result of a Broadcast command. (A FORMAT error will be generated if the BROADCAST bit is not set on the RTU's Status Word.)
MODE CODE	When logic 1, the message is treated as a Mode Code. (The Command Word — Word Count field indicates Mode Code type.)
BROADCAST	When logic 1, indicates that the message is a Broadcast Command. (No Status Word is expected.)
RT-RT	When logic 1, the message is treated as an RT-RT transfer. (The next two words are Command Words.) Both Status Word responses are validated.

Note:

1. MASK BROADCAST XOR BROADCAST BIT in Status Word = STATUS SET ERROR.
2. When the BC expects the BROADCAST bit set in the Status Word, a logic 1 will mask the Status Interrupt Error flag.

FIGURE 14. BC CONTROL WORD

## RESET

The BUS-61553 can be reset by pulsing the **MSTRCLR** (pin 71) low or by writing to the Start/Reset register. After a reset condition has occurred, the Configuration, Interrupt, and (internal) Block Status word register outputs are forced to a logic 0.

The BUS-61553 will automatically access an external, 3-state device (i.e., counter) at the start and end of each message in BC or RTU modes. The BUS-61553 output, TAGEN (pin 76), enables the device's output onto the common, 16-bit data highway while executing a memory-write cycle. The device's value is written into the second location of the Descriptor Stack Entry. If a counter is used, its clock, enable, and reset control lines are connected per system requirement (see figure 15). If no external device is attached to the data bus, an expected value of FFFF (H) will be written into the Time Tag location within the Descriptor Stack.

Note that the 8-bit Gap Time value generated in the 1553 MT mode of operation is implemented using an 8-bit counter internal to the BUS-61553 (see MT operation).

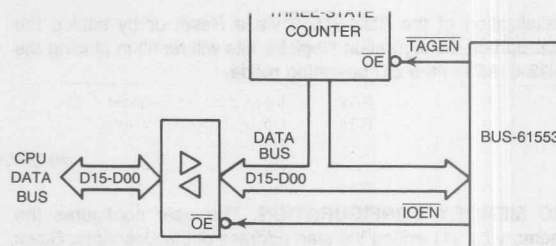


FIGURE 15. BC/RT TIME TAGGING (OPTIONAL)

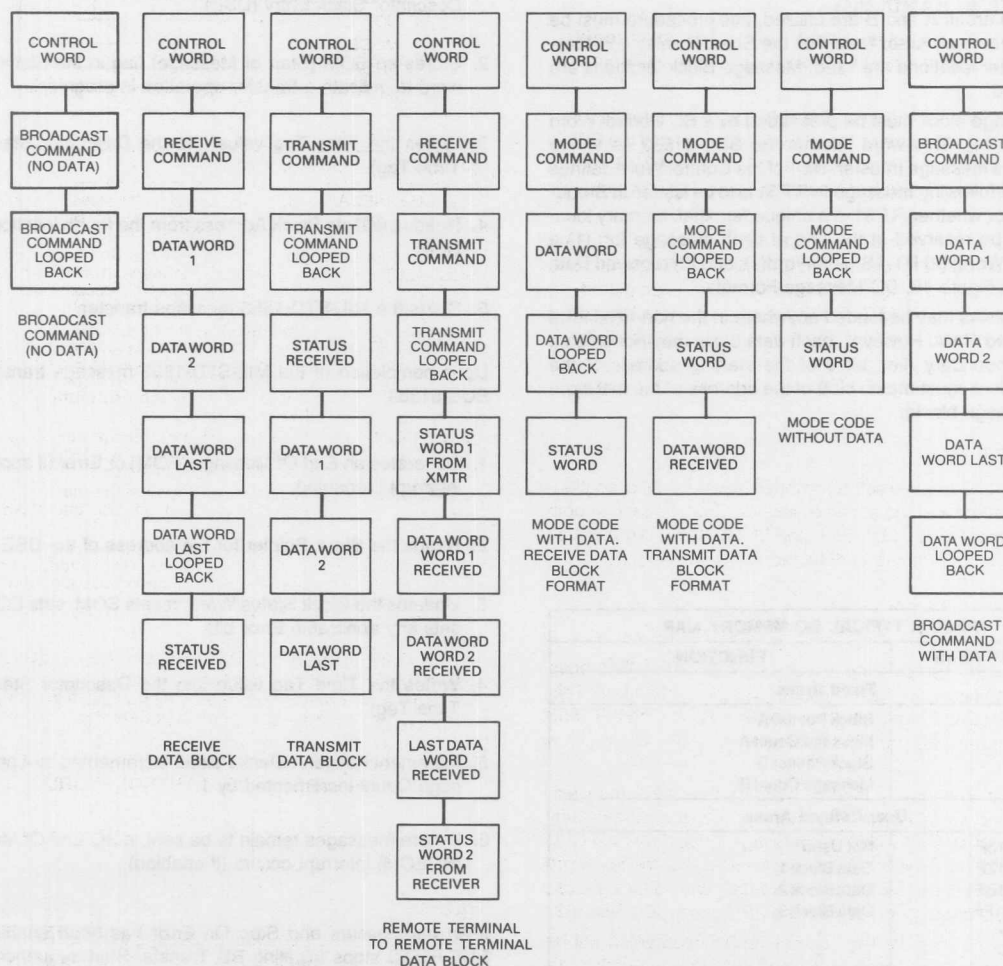


FIGURE 16. BC MESSAGE FORMATS



## BC OPERATION

Initialization of the BUS-61553 via a Reset or by setting the appropriate Configuration Register bits will result in placing the BUS-61553 in the BC operating mode.

**BC MEMORY CONFIGURATION.** The user configures the memory by: (1) writing the start address of the Descriptor Stack into the Current Area Stack Point location; (2) loading the fourth word of each Descriptor Stack Entry (DSE) with the start location of each message block; and (3) loading the Message Counter with the total number of messages to be transmitted. Note that the Message Count must be written in 1's complement. For example, to transmit one message, load 00FE(H) (see Table 3, BC Memory Map).

If both map areas A and B are utilized, this procedure must be performed for each area. Note that the Stack Pointer and Message Counter locations are fixed; Message Block locations are user-defined.

Each message block must be preceded by a BC Control Word (see figure 14). This word informs the BUS-61553 as to the format of the message transfer. Bit 1 of the Control Word defines whether the following message to RT 31 is to be issued in Broadcast Mode or whether RT 31 is a unique terminal. Memory locations must be reserved at the end of each message for: (1) a Loop Back Word; (2) RTU Status Word(s); and (3) received Data words. See Figure 16, BC Message Formats.

Message blocks may be loaded anywhere in the non-fixed area of the shared RAM. However, each data block may not cross a 256 word boundary (i.e., bit 8 of the starting address of the message block must match bit 8 of the address of the last word of the message block).

TABLE 3. TYPICAL BC MEMORY MAP	
HEX ADDRESS	FUNCTION
<b>Fixed Areas</b>	
0100	Stack Pointer A
0101	Message Count A
0104	Stack Pointer B
0105	Message Count B
<b>User Defined Areas</b>	
0108 - 013F	Not Used
0140 - 017F	Data Block 1
0180 - 01BF	Data Block 2
01C0 - 01FF	Data Block 3
.	.
0F00 - 0FFF	Descriptor Stack A
0000 - 00FF	Descriptor Stack B

**ADDITIONAL FEATURES.** The Configuration Register - STOP ON ERROR bit can be set. This causes the BUS-61553 to halt operation at the end of the current message transfer if an error is detected. In addition, setting the Interrupt Mask Register bits will result in a low pulse on the Interrupt (INT) pin with each occurrence of the respective error, end of message or end of message frame condition (See Configuration Register and Interrupt Register sections).

## BC TRANSFER-START SEQUENCE

After setting the CONTROLLER START bit in the Start/Reset Register, the BUS-61553 takes the following actions:

1. Reads the Current Area Stack Pointer for the address of the Descriptor Stack Entry (DSE).
2. Stores an SOM (Start of Message) flag in the Block Status word to indicate a transfer operation in progress.
3. Writes the Time Tag value into the Descriptor Stack (see Time Tag).
4. Reads the Data Block Address from the fourth location of the DSE.
5. Starts the MIL-STD-1553 message transfer.

Upon completion of the MIL-STD-1553 message transfer, the BUS-61553:

1. Generates an End Of Message (EOM) or Error (if applicable) interrupt if enabled.
2. Reads the Stack Pointer for the address of the DSE.
3. Updates the Block Status Word; resets SOM, sets EOM, and sets any applicable Error bits.
4. Writes the Time Tag value into the Descriptor Stack (see Time Tag).
5. Increment Pointers: Stack Pointer incremented by 4 and Message Count incremented by 1.
6. If more messages remain to be sent, a BC End Of Message (BCEOM) interrupt occurs (if enabled).

If an error occurs and Stop On Error has been enabled, the BUS-61553 stops initiating BC Transfer-Start sequences. The Stack Pointer will point to the next message to be transferred (see figure 17).

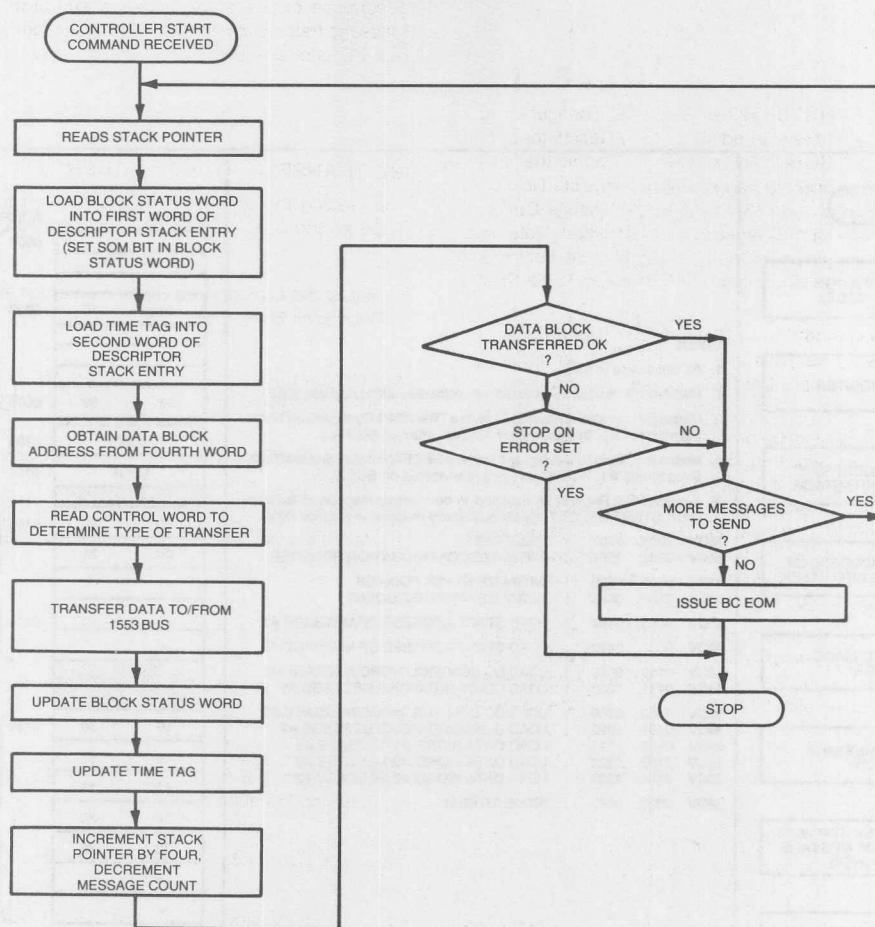


FIGURE 17. BC SEQUENCE OF OPERATION

# BC SETUP IMPLEMENTATION EXAMPLE

Figure 18a-c shows the BC mode examples for two message transfers, BASIC setup, and BC memory setup.

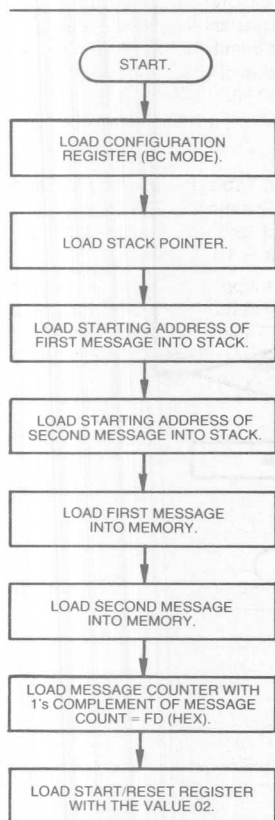


FIGURE 18a. BC SET-UP EXAMPLE FOR TWO MESSAGE TRANSFER

## GIVEN:

1. All values are in hex.
2. Map Area "A" is used and located from Address 0000 to Address 00FF.
3. Message 1, located at Address 0140, is a TRANSMIT Command to RT #1, Subaddress #1, Word Count = 1, transmitted on BUS A.
4. Message 2, located at Address 0180, is a RECEIVE Command to RT #3, Subaddress #1, Word Count = 3, transmitted on BUS B.
5. Configuration Register is assumed to be memory mapped at location 2001. START/RESET Register is memory mapped at location 2003.

```

MOV 2003, 0001 ; ISSUE RESET
MOV 2001, 0FFF ; INITIALIZE CONFIGURATION REGISTER

MOV 0100, 0000 ; INITIALIZE STACK POINTER
MOV 0101, 00FD ; INITIALIZE MESSAGE COUNT

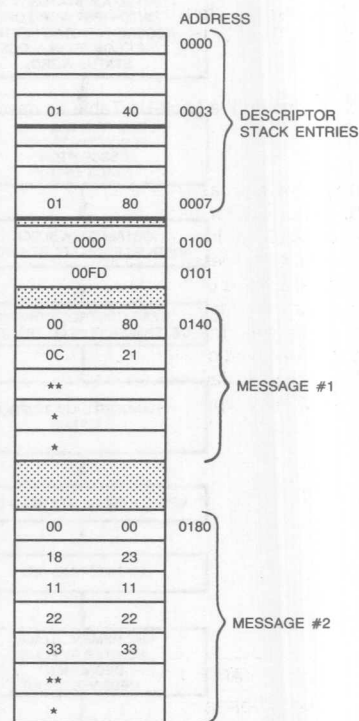
MOV 0003, 0140 ; LOAD START ADDRESS OF MESSAGE #1
MOV 0007, 0180 ; LOAD START ADDRESS OF MESSAGE #2

MOV 0140, 0080 ; LOAD BC CONTROL WORD MESSAGE #1
MOV 0141, 0C21 ; LOAD COMMAND WORD MESSAGE #1

MOV 0180, 0000 ; LOAD BC CONTROL WORD MESSAGE #2
MOV 0181, 1823 ; LOAD COMMAND WORD MESSAGE #2
MOV 0182, 1111 ; LOAD DATA WORD #1 MESSAGE #2
MOV 0183, 2222 ; LOAD DATA WORD #2 MESSAGE #2
MOV 0184, 3333 ; LOAD DATA WORD #3 MESSAGE #2

MOV 2003, 0002 ; ISSUE "START"
  
```

FIGURE 18b. SAMPLE BC SET-UP INSTRUCTIONS



\*Left empty for RTU's Status response.  
\*\*Loop Back word.

FIGURE 18c. BC SET-UP MEMORY MAP

FIGURE 18. EXAMPLE: BC SET-UP IMPLEMENTATION

## RTU OPERATION

The RTU mode is selected by resetting the BUS-61553 and setting the appropriate bits in the Configuration Register.

**RTU MEMORY CONFIGURATION.** The user configures the memory by:

1. Writing the start address of the Descriptor Stack into the Stack Pointer location and
2. Setting up the Look-Up Table as described below.

If both map areas (A and B) are utilized, this procedure must be performed for each area. Note that the Stack Pointer and Look-Up Table locations are fixed; Data Block(s) locations are user-defined. Message blocks may be loaded anywhere in the non-fixed areas of the shared RAM. However, each data block may not cross a 256 word boundary (i.e., bit 8 of the starting address of the message block must match bit 8 of the address of the last word of the message block). An example of a typical RTU Memory Map is given in table 4. Figure 19 shows the RTU Initialization steps.

TABLE 4. TYPICAL RTU MEMORY MAP	
HEX ADDRESS	FUNCTION
<b>Fixed Areas</b>	
0100	Descriptor Stack Pointer A
0101	Reserved
0104	Descriptor Stack Pointer B
0105	Reserved
0108 - 013F	Spare
0140 - 017F	Look-Up Table A
01C0 - 01FF	Look-Up Table B
<b>User Defined Areas</b>	
0180 - 019F	Data Block 1
01A0 - 01BF	Data Block 2
0200 - 021F	Data Block 3
.	.
.	.
0EE0 - 0EFF	Data Block 107
0000 - 00FF	Descriptor Stack A
0F00 - 0FFF	Descriptor Stack B

**RTU LOOK-UP TABLE.** The RTU mode uses a Look-Up Table in order to map the Data Blocks based upon incoming 1553 Command Words. The BUS-61553 uses the T/R and Subaddress fields to address the Look-Up Table. Each Look-Up Table (A and B) location contains a user-defined Data Block Pointer to an associated Data Block (see figures 20 and 21).

Note: The Data Block and Stack Pointers are maintained internally using an 8-BIT-REGISTER for the HIGH BYTE and an 8-BIT COUNTER for the LOW BYTE; the high byte remains constant (user value) while the low byte will wrap around from FF(H) to 00(H). For example: a current Pointer value of 10 FF(H) will increment to 10 00(H) and not 11 00(H).

The first 32 words of the Look-Up Table are reserved for Data Blocks associated with Receive Commands (T/R bit = 0). The remaining 32 words are reserved for Data Blocks associated with Transmit Commands (T/R bit = 1).

Mode Commands with data are mapped in the same manner as non-mode commands. A Synchronize With Data command maps to the first or thirty-second Table entry (depending upon subaddress: all 0's or all 1's), while a Transmit Vector Word command points to the thirty-third or sixty-fourth entry.

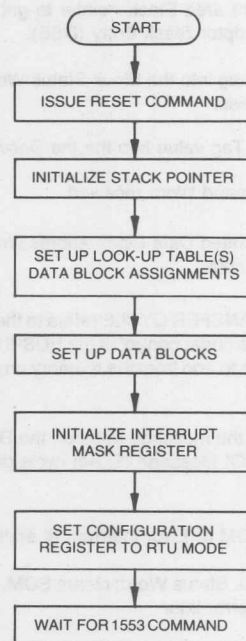


FIGURE 19. RTU INITIALIZATION

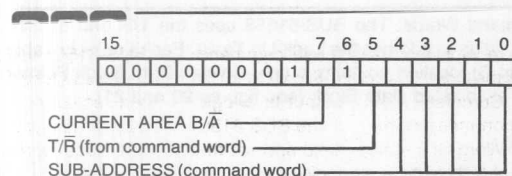


FIGURE 20. RTU LOOK-UP TABLE ADDRESS

				DATA BLOCK
T/R	SUBADD	WORD COUNT	LOOK-UP TABLE (A) ADDRESS	DATA BLOCK
0	00000	XXXXX	0140	USER DEFINED
0	00001	XXXXX	0141	USER DEFINED
0	00010	XXXXX	0142	USER DEFINED
	64 LOCATIONS			
			...	
1	11110	XXXXX	017E	USER DEFINED
1	11111	XXXXX	017F	USER DEFINED

FIGURE 21. LOOK-UP TABLE EXAMPLE

### RTU MESSAGE BLOCK TRANSFER SEQUENCE

RTU message transfer operations begin automatically upon receipt of a valid command word from the 1553 bus. A message transfer takes the form of an RTU Start Of Message (SOM) cycle followed by the 1553 Message Transfer Cycle and an RTU End Of Message (EOM) cycle (see figure 22).

During the RTU SOM cycle, the BUS-61553 takes the following actions:

1. Loads the 1553 command word.
2. Reads the current area Stack Pointer to get the address of the current Descriptor Stack Entry (DSE).
3. Stores an SOM flag into the Block Status Word to indicate a transfer in progress.
4. Writes the Time Tag value into the the Descriptor Stack.
5. Stores the Command Word received.
6. Reads the associated Data Block Address from the (current area) Look-Up Table.

The MESSAGE TRANSFER CYCLE refers to the actual transfer of the 1553 message under control of the BUS-61553. The BUS-61553 transfers data to and from the memory on a word-by-word basis.

Upon completion of the message transfer, the BUS-61553 executes an RTU End Of Message (EOM) cycle during which the BUS-61553:

1. Generates an EOM or Error interrupt (if enabled).
2. Updates the Block Status Word: clears SOM, sets EOM, and any appropriate error bits.
3. Writes the Time Tag value into the Descriptor Stack.
4. Increments the Stack Pointer by 4.

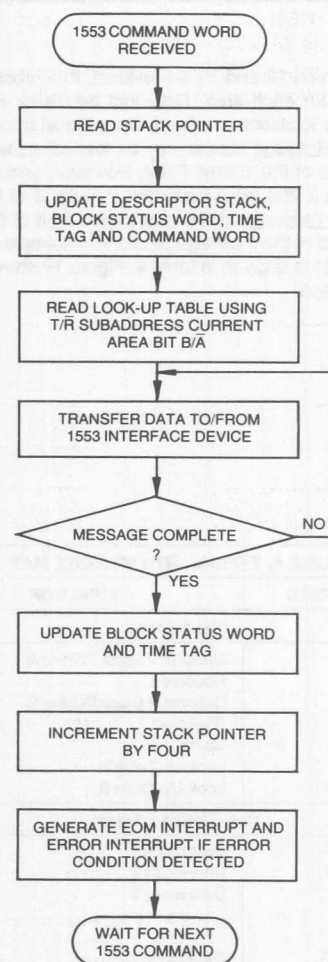


FIGURE 22. RTU MESSAGE TRANSFER OPERATION



**ADDITIONAL FEATURES.** Four 1553 Status Word flags can be programmed via the appropriate Configuration Register bits. In addition, setting Interrupt Mask Register bits will result in a low pulse on the Interrupt (INT) pin with each occurrence of the respective error or end of message condition. (See Configuration Register and Interrupt Register sections.)

**THIS RT:** Each command appearing on either 1553 Bus is decoded and tested for Manchester/protocol errors. If the BUS-61553 receives a valid command word containing a RTU address equivalent to the RTAD0-RTAD4 inputs (pins 10, 9, 50, 49, and 11, respectively), THIS-RT (pin 55) will be pulsed low. This signal can be used to identify specific 1553 commands. This signal is also active in the BC mode.

**Command Illegalization (Optional).** The BUS-61553 has the capability to illegalize MIL-STD-1553 mode commands. In addition, valid non-mode commands can be illegalized based upon the Command Word subaddress field. An illegal command is identified by driving the Illegal Command, ILLCMD (pin 12) input low. The BUS-61553 multiplexes the Word Count and Subaddress fields (pins SA/MC0 – SA/MC4).

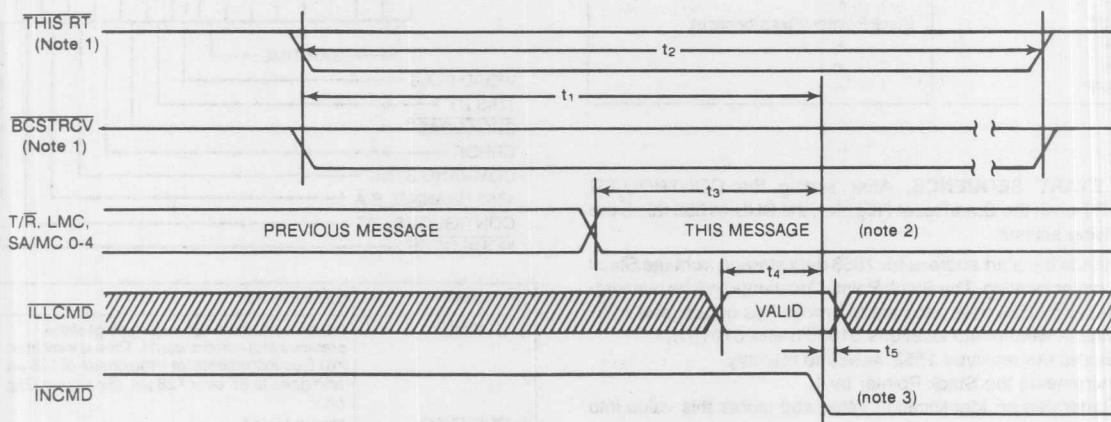
The BUS-61553 responds to illegalized commands by transmitting its Status Word with the Message Error bit set. No data

words are transmitted; received words, however, are placed in the shared RAM locations indicated by the current area Look-Up Table.

Upon receipt of a valid mode command, the BUS-61553 will output the Command Word-Word Count field and set the Latched Mode Command (LMC) output to a logic 1. Upon receipt of a valid non-mode command, the BUS-61553 will output the Command Word-Subaddress field and set the Latched Mode Command (LMC) output to a logic 0.

An external PROM can be used for command illegalization by decoding the word count/subaddress, LMC and Broadcast Received (BCSTRCV) bits and driving ILLCMD low where appropriate (see figure 23).

**BUSY BIT.** If the user asserts the BUSY bit low in the Configuration Register, the BUS-61553 will respond with a Status Word with the BUSY bit set. In addition, no data words will be transferred from the shared RAM as indicated by the corresponding value in the current area Look-Up Table. The AIM-Hy will transfer data associated with a Receive Command into memory but will not transmit data out onto the MIL-STD-1553 bus when busy upon receipt of a Transmit Command.



COMMAND ILLEGALIZATION TIMING					
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t <sub>1</sub>	THIS RT, BCSTRCV valid delay to INCMD	1.475	-	-	μs
t <sub>2</sub>	THIS RT, BCSTRCV validity time	3.7	-	4.3	μs
t <sub>3</sub>	T/R, LMC, SA/MC 0-4 setup time to INCMD	425	-	-	ns
t <sub>4</sub>	ILLCMD setup time to INCMD	175	-	-	ns
t <sub>5</sub>	ILLCMD hold time following INCMD	5	-	-	ns

**NOTES:**

1. THIS RT is asserted low for messages directed to the discrete terminal address.
2. BCSTRCV is asserted low for messages directed to Address 31, the Broadcast Address.
3. T/R, LMC, SA/MC 0-4 remain valid until receipt of next command or Master Reset.
4. ILLCMD input sampled internally on falling edge of INCMD.

**FIGURE 23. BROADCAST, T/R BIT, LMC, SUBADDRESS/MODE CODE ILLEGALIZATION TIMING**

## MT OPERATION

Initiate a Reset in order to initialize the BUS-61553. Configure the BUS-61553 as a Bus Monitor (MT) by setting the appropriate Configuration Register Bits. See figure 24 for MT initialization steps.

**MT MEMORY CONFIGURATION.** The user configures the memory by writing the start address for 1553 data storage into the Stack Pointer location. The Monitor Stack will automatically wrap around once the RAM has been filled (i.e., location 1FFF(H) of 8K x 16 RAM is followed by location 0000). An example of a typical MT Memory Map is given in table 5.

TABLE 5. TYPICAL MT MEMORY MAP	
HEX ADDRESS	FUNCTION
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification Word
0004	.
0005	.
0006	.
.	.
0100	Stack Pointer (Fixed location)
.	.
.	.
1FFF	.

**MT START SEQUENCE.** After setting the CONTROLLER START bit in the Start/Reset Register, the BUS-61553 takes the following actions:

1. Reads the start address for 1553 data storage from the Stack Pointer location. The Stack Pointer location(s) will be overwritten with 1553 data once the MT mode has begun [and 1553 data is written into locations 0100(H) and 0101(H)].
2. Stores the received 1553 word into memory.
3. Increments the Stack Pointer by 1.
4. Generates an Identification Word and stores this value into memory.
5. Repeats steps 2-4 until a Reset condition occurs.

**MT IDENTIFICATION WORD.** The Identification Word provides the CPU with information pertaining to the received 1553 word. Its format is shown in figure 25. This information allows the user to analyze the 1553 data.

**THIS-RT:** Each command appearing on either 1553 Bus is decoded and tested for Manchester/protocol errors. If the BUS-61553 receives a valid command word containing a Command Sync and a RTU address equivalent to the RTAD0-RTAD4 inputs (pins 10, 9, 50, 49, and 11, respectively), THIS-RT (pin 55) will be pulsed low. This signal can be used to identify specific 1553 commands or for switching to RTU mode upon receipt of a command to this address.

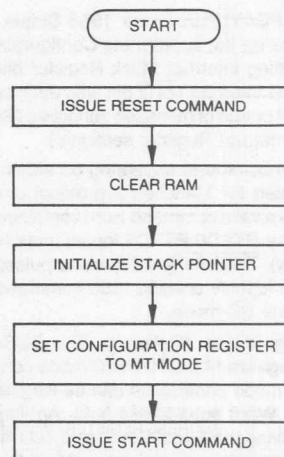
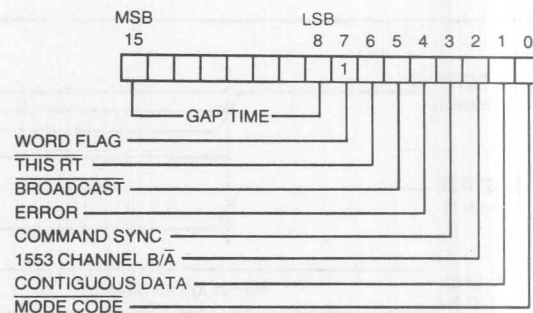


FIGURE 24. MT INITIALIZATION



BIT NAME	DEFINITION
GAP TIME	Indicates the time between receipt of the previous and current words. Time is indicated in 0.5 $\mu$ s increments for a maximum of 128 $\mu$ s and goes to FF over 128 $\mu$ s. (See Word Gap bit.)
WORD FLAG	Always logic 1.
THIS RT	Logic 0 indicates RT address field of the associated command or Status Word matches the RT address field of the BUS-61553.
BROADCAST	Logic 0 indicates the RTU address field of the command or Status Word corresponds to address 31 (decimal).
ERROR	Logic 1 indicates Manchester, Parity, Sync and/or low bit count error.
COMMAND SYNC	Logic 1 indicates 1553 Command or Status Word sync field. (Logic 0 indicates a Data Word sync field in received word.)
1553 CHANNEL B/A	Indicates word received on 1553 Bus A (1) or Bus B (0).
CONTIGUOUS DATA	Logic 1 indicates the word was received within 2 $\mu$ s of the previous word. If logic 0, bits 8-15 contain the measured gap between the words.
MODE CODE	When logic 0, the data transferred is a mode code command.

FIGURE 25. MT IDENTIFICATION WORD

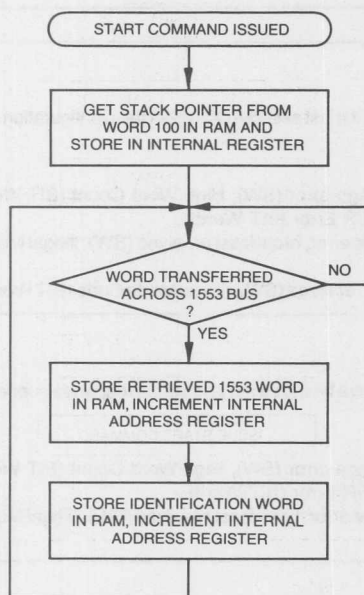


FIGURE 26. MT DATA STORAGE OPERATION

**MT DATA STORAGE.** Figure 26 shows the steps in a MT data storage operation.

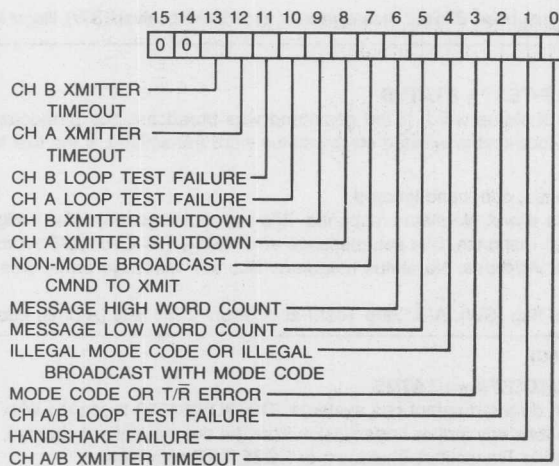
**INTERRUPTS:** SA/MC – 0 (pin 13), SA/MC – 1 (pin 15), and SA/MC – 2 (pin 52) represents B6, B7, and B8 counter outputs in the MT mode. B6 counts every 32 words transferred, B7 every 64 words, and B8 every 128 words. These counter outputs can be used to generate interrupts to the subsystem to insure proper servicing of Memory. The Data Word and Identification Word transfers increment the counter by two.

## BUILT-IN-TEST WORD (RTU MODE)

The BUS-61553 contains a 14 bit Built-In-Test (BIT) word register which stores information about the condition of the RTU. When a Mode Command is received to transmit BIT word, the contents of this register are transmitted over the 1553 data bus. Figure 27 shows the meaning of each bit in the BIT register. Information is included regarding transmitter timeouts, loop test failures, transmitter shutdown, subsystem handshake failure, and the results of individual message validations.

## MODE CODES

The BUS-61553 implements all mode codes applicable to dual-redundant systems. Mode codes can also be illegalized using the appropriate I/O signals. Mode command illegalization and handling are detailed in the RTU Operation section and listed in table 6.



### Notes:

- Bits 0-2 and 10-13 are latched and only cleared by a mode reset command or a master RESET.
- Bits 3-7 are cleared at the start of each new message and updated at the end of the message. They reflect the present command word.
- Bits 8-9 are set by the mode command for Transmitter Shutdown and are cleared by the mode command for Override Transmitter Shutdown, Reset RTU or a master RESET.

FIGURE 27. BUILT-IN-TEST WORD (RTU MODE)

TABLE 6. MODE CODES

**DYNAMIC BUS CONTROL (00000)****MESSAGE SEQUENCE = DBC \* STATUS**

The BUS-61553 responds with status. If the subsystem wants control of the bus, it must set DBACC within the Configuration Register.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

**SYNCHRONIZE WITHOUT DATA WORD (00001)****MESSAGE SEQUENCE = SYNC \* STATUS**

The BUS-61553 responds with status. If sent as a broadcast, the broadcast receive bit will be set and status response suppressed.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

**TRANSMIT STATUS WORD (00010)****MESSAGE SEQUENCE = TRANSMIT STATUS \* STATUS**

The status and BIT word registers are not altered by this command and contain the resulting status from the previous command.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

**INITIATE SELF-TEST (00011)****MESSAGE SEQUENCE = SELF-TEST \* STATUS**

The BUS-61553 responds with a status word. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Short-loop test is initiated on the status word transmitted. If the test fails, an RT fail flag is set.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).
5. **Faulty Test.** Bits set: terminal flag (SW), A/B Loop Test Fail, Current 1553 Bus (A or B) Loop Test Fail (BIT Word).

**TRANSMITTER SHUTDOWN (00100)****MESSAGE SEQUENCE = SHUTDOWN \* STATUS**

This command is only used with dual redundant bus systems. The BUS-61553 responds with status. At the end of the status transmission, the BUS-61553 inhibits any further transmission from the dual redundant channel. Once shutdown, the transmitter can only be reactivated by Override Transmitter Shutdown or RESET RT commands.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

\* = Status response time



TABLE 6. MODE CODES (CONTINUED)

## OVERRIDE TRANSMITTER SHUTDOWN (00101)

### MESSAGE SEQUENCE = OVERRIDE SHUTDOWN \* STATUS

This command is only used with dual redundant bus systems. The BUS-61553 responds with status. At the end of the status transmission, the BUS-61553 re-enables the transmitter of the redundant bus. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

## INHIBIT TERMINAL FLAG BIT (00110)

### MESSAGE SEQUENCE = INHIBIT TERMINAL FLAG \* STATUS

The BUS-61553 responds with status and inhibits further internal or external setting of the terminal flag bit in the status register. Once the terminal flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT command. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

## OVERRIDE INHIBIT TERMINAL FLAG BIT (00111)

### MESSAGE SEQUENCE = OVERRIDE INHIBIT TERMINAL FLAG \* STATUS

The RTU responds with status and reactivates the terminal flag bit in the status register. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

## RESET REMOTE TERMINAL (01000)

### MESSAGE SEQUENCE = RESET REMOTE TERMINAL \* STATUS

The BUS-61553 responds with status and internally resets. Transmitter shutdown, mode commands, BIT Word, and inhibit terminal flag commands will be reset. If the command was broadcast, the broadcast received bit is set and the status word is suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

## RESERVED MODE CODES (01001-01111)

### MESSAGE SEQUENCE = RESERVED MODE CODES \* STATUS

The BUS-61553 responds with status. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), Illegal Mode Code (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

\* = Status response time



TABLE 6. MODE CODES (CONTINUED)

## TRANSMIT VECTOR WORD (10000)

**MESSAGE SEQUENCE = TRANSMIT VECTOR WORD \* STATUS VECTOR WORD**

The BUS-61553 transmits a status word followed by a vector word.

### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, (BIT Word).

## SYNCHRONIZE WITH DATA WORD (10001)

**MESSAGE SEQUENCE = SYNCHRONIZE DATA WORD \* STATUS**

The data word received following the command word is transferred to the RAM. The status word is then transmitted. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), Low Word Count (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), T/R Error, High Word Count (BIT Word).
5. **Command T/R bit Set to Zero and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), High Word Count, T/R Error (BIT Word).

## TRANSMIT LAST COMMAND (10010)

**MESSAGE SEQUENCE = TRANSMIT LAST COMMAND \* STATUS LAST COMMAND**

The status and BIT word registers are not altered by this command. The SW contains the status from the previous command. The data word transmitted contains the previous valid command (providing it was not another TRANSMIT LAST COMMAND).

### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

## TRANSMIT BIT WORD (10011)

**MESSAGE SEQUENCE = TRANSMIT BIT WORD \* STATUS BIT WORD**

The BUS-61553 responds with status followed by the BIT word. The BIT word is not altered by this command; however, the next SW will reflect errors in this transmission.

### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bit set: message error (SW).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

\* = Status response time

## SELECTED TRANSMITTER SHUTDOWN (10100)

### MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA \* STATUS

The data word received is transferred to the subsystem and status is transmitted. No other action is taken by the BUS-65515. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Intended for use with RTs with more than one dual redundant channel.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count (BIT Word).

## OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101)

### MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA \* STATUS

The data word received after the command word is transferred to the subsystem. No other action is taken by the BUS-65515. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count, T/R Error (BIT Word).

## RESERVED MODE CODES

### MESSAGE SEQUENCE = RESERVED MODE CODE (T/R = 1) \* STATUS RESERVED MODE CODE (T/R = 0) \* STATUS

The BUS-61553 responds with status. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

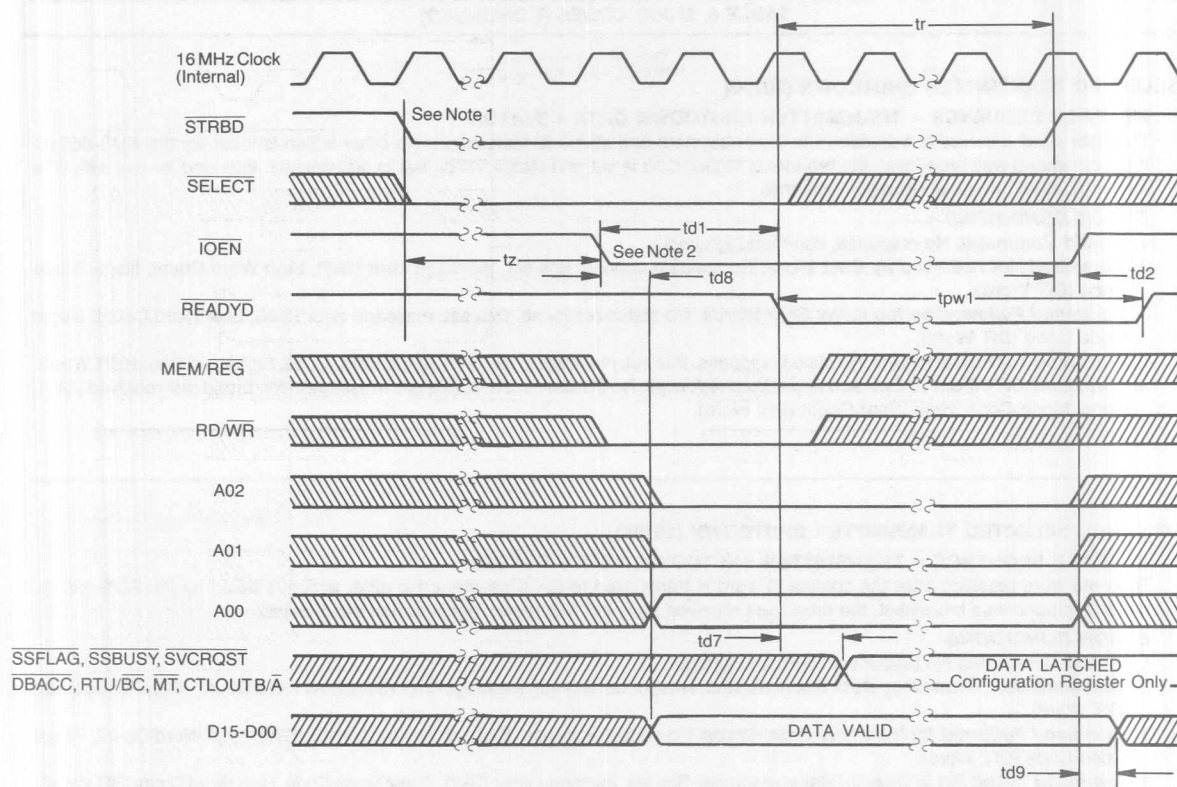
#### ERROR CONDITIONS (T/R = 1)

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

#### ERROR CONDITIONS (T/R = 0)

1. **Invalid Command.** No response, command ignored.
2. **Command not Followed by Contiguous Data Word.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

\* = Status response time

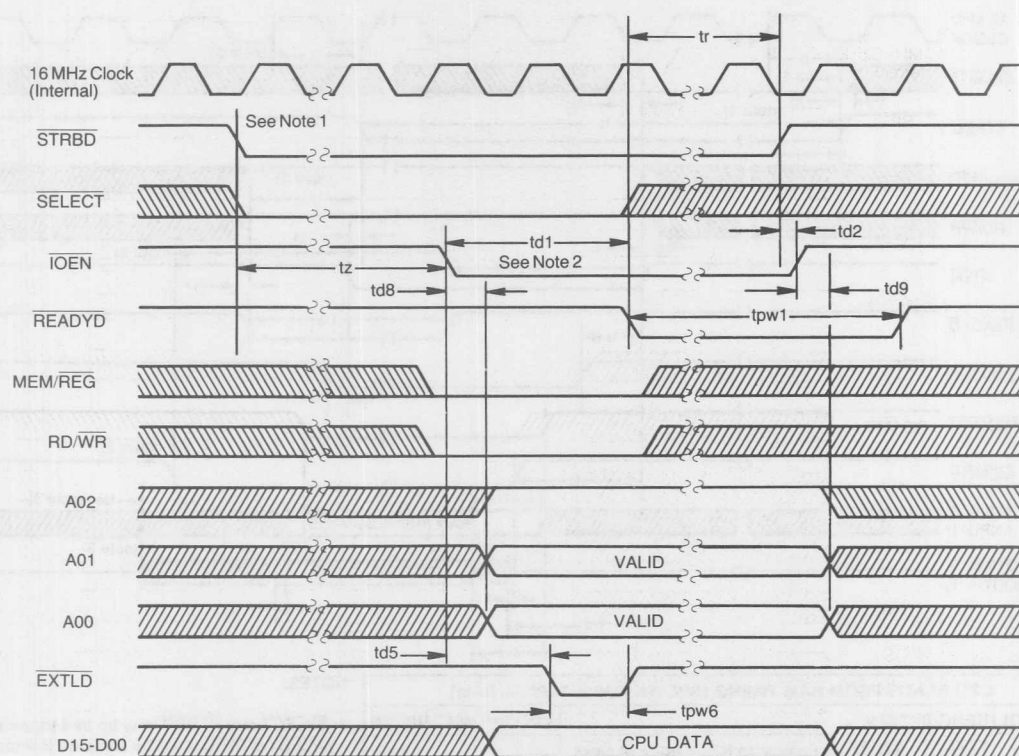


**Notes:**

1. STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus (1.8  $\mu$ s max).
2. CPU must release STRBD within 1.5  $\mu$ s of IOEN going active. READYD will go away within one clock cycle max.

CPU WRITES TO INTERNAL REGISTER				
SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td1	READYD low delay (CPU Handshake)	—	150	ns
td2	IOEN high delay (CPU Handshake)	—	20	ns
tpw1	READYD pulse width (CPU Handshake)	50	—	ns
td7	Internal Register delay (write)	—	60	ns
td8	Register Data/Address set-up time	—	30	ns
td9	Register Data/Address hold time	—	0	ns
tr	READYD to STRBD release	—	1.37	$\mu$ s
tz	(SELECT + STRBD) to IOEN	—	1.8	$\mu$ s

**FIGURE 28. CPU WRITES TO INTERNAL REGISTER**

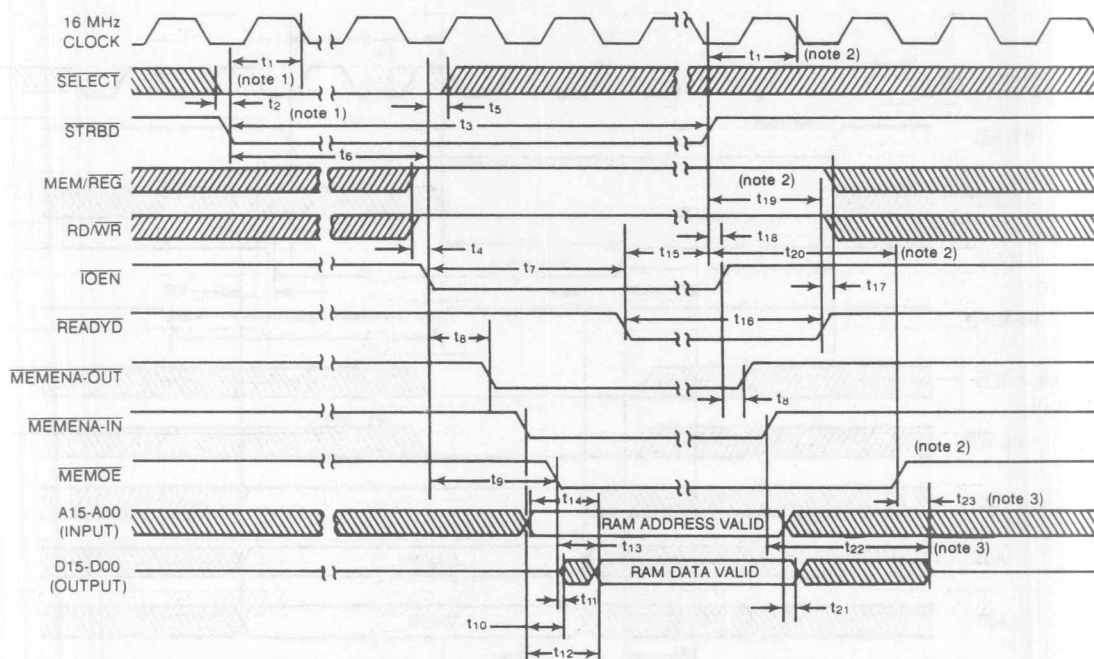


**Notes:**

1. STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus (1.8  $\mu$ s max).
2. CPU must release STRBD within 1.5  $\mu$ s of IOEN going active. READYD will go away within one clock cycle max.

CPU WRITES TO EXTERNAL REGISTER					
SYMBOL	DESCRIPTION	MIN	MAX	UNITS	
td1	READYD low delay (CPU Handshake)	—	150	ns	
td2	IOEN high delay (CPU Handshake)	—	20	ns	
tpw1	READYD pulse width (CPU Handshake)	50	—	ns	
td5	EXTLD low delay	50	—	ns	
td8	Register Data/Address set-up time	—	30	ns	
td9	Register Data/Address hold time	—	0	ns	
tpw6	EXTLD low pulse width	56	—	ns	
tr	READYD to STRBD release	—	1.37	$\mu$ s	
tz	(SELECT • STRBD) to IOEN	—	1.8	$\mu$ s	

FIGURE 29. CPU WRITES TO EXTERNAL REGISTER



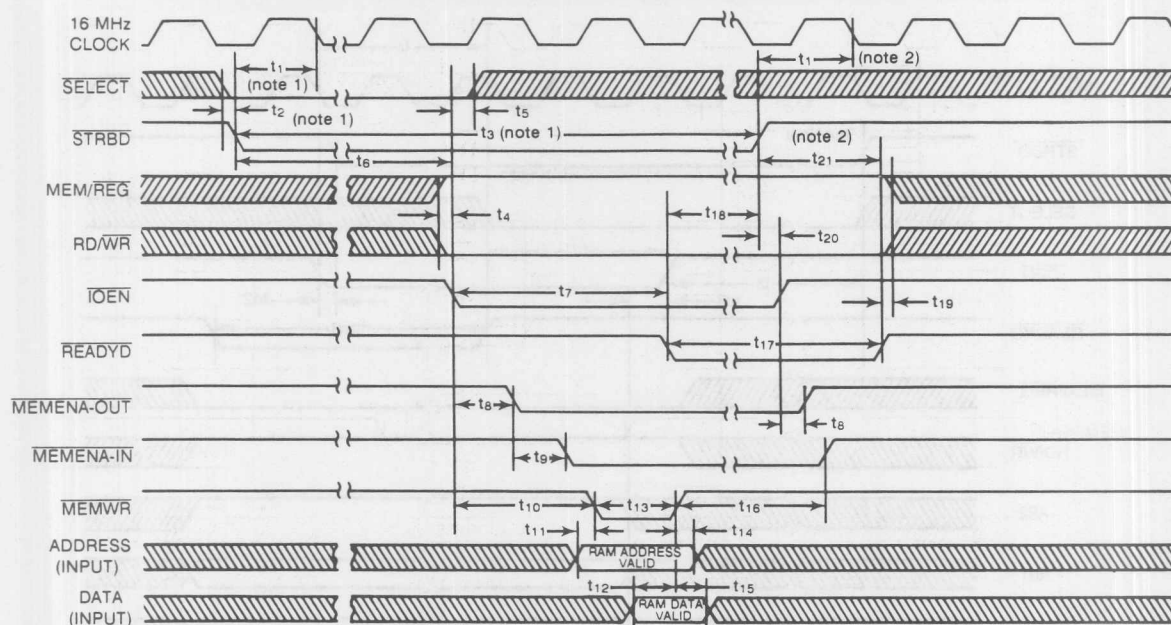
CPU READS FROM RAM TIMING (SHOWN FOR INTERNAL RAM)					
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t <sub>1</sub>	SELECT • STRBD setup time to falling edge of clock	30	-	-	ns
t <sub>2</sub>	SELECT setup time to STRBD	(Note 1)			ns
t <sub>3</sub>	STRBD width	(t <sub>6</sub> + t <sub>7</sub> + t <sub>15</sub> )			ns
t <sub>4</sub>	MEM/REG, RD/WR setup time to IOEN	0	-	-	ns
t <sub>5</sub>	SELECT hold time following IOEN	0	-	-	ns
t <sub>6</sub>	SELECT • STRBD to IOEN delay (without contention)	75	-	160	ns
t <sub>6</sub>	SELECT • STRBD to IOEN delay (with contention)	-	-	1.80	μs
t <sub>7</sub>	IOEN to READYD delay	115	125	150	ns
t <sub>8</sub>	IOEN to MEMENA-OUT delay	-	-	40	ns
t <sub>9</sub>	IOEN low to MEMOE delay	55	62.5	70	ns
t <sub>10</sub>	MEMENA-IN to data low-Z	5	-	-	ns
t <sub>11</sub>	MEMOE to data low-Z	0	-	-	ns
t <sub>12</sub>	MEMENA-IN to output data valid	-	-	55	ns
t <sub>13</sub>	MEMOE low to output data valid	-	-	30	ns
t <sub>14</sub>	Address access time to output data valid	-	-	55	ns
t <sub>15</sub>	READYD to STRBD release time	-	-	1.37	μs
t <sub>16</sub>	READYD pulse width	50	-	-	ns
t <sub>17</sub>	MEM/REG, RD/WR hold time following READYD high	0	-	-	ns
t <sub>18</sub>	STRBD high delay to IOEN high	-	-	20	ns
t <sub>19</sub>	STRBD high delay to READYD high (Note 2)	-	-	105	ns
t <sub>20</sub>	STRBD high delay to MEMOE high (Note 2)	115	-	170	ns
t <sub>21</sub>	Data hold time after address invalid	5	-	-	ns
t <sub>22</sub>	MEMENA-IN high to data tri-state	-	-	25	ns
t <sub>23</sub>	MEMOE high to data tri-state	-	-	25	ns

## NOTES:

1. SELECT and STRBD may be tied together. SELECT • STRBD must be sampled low for two consecutive falling edges of the 16 MHz clock when the BUS-61553's protocol/memory management logic is not using the data bus. When this occurs IOEN goes low, starting the transfer cycle. At this time, SELECT may be released high.
2. READYD goes high after the first falling edge of clock input (satisfying t<sub>1</sub>) following STRBD going high. MEMOE goes high after STRBD is sampled high for a second falling clock edge.
3. Data tri-state occurs after t<sub>22</sub> or t<sub>23</sub>, whichever occurs first.

**FIGURE 30.**  
**CPU READS FROM RAM TIMING**  
(Shown for Internal RAM)



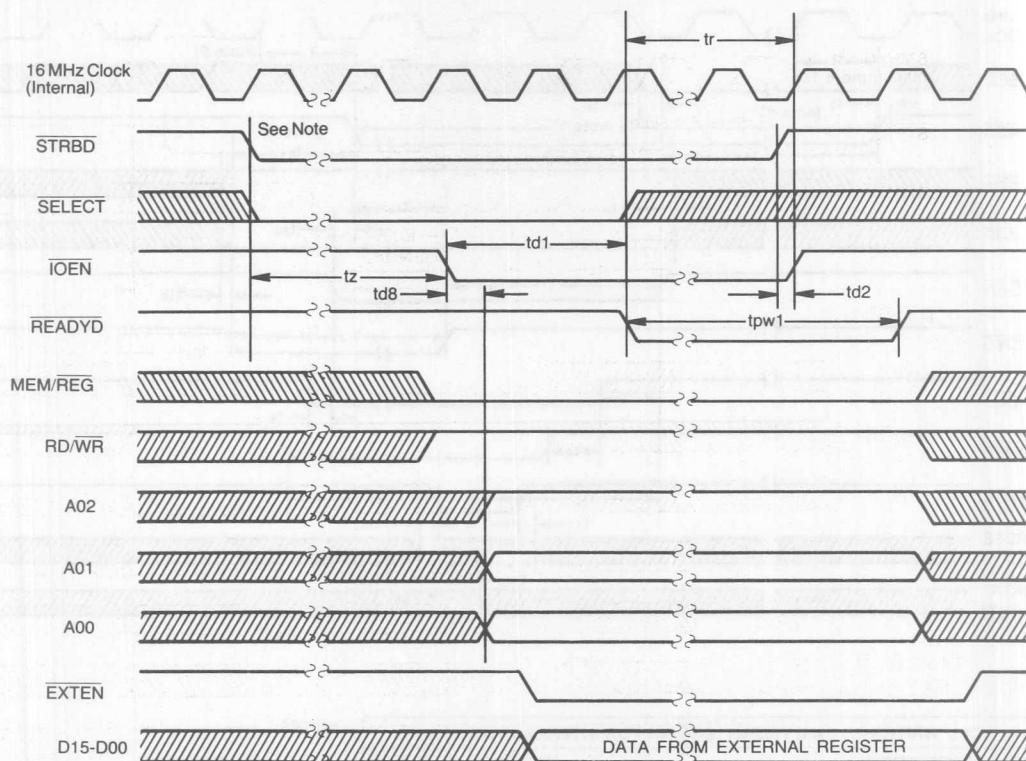


CPU WRITES TO RAM TIMING (SHOWN FOR INTERNAL RAM)					
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t <sub>1</sub>	SELECT + STRBD setup time to falling edge of clock	30	-	-	ns
t <sub>2</sub>	SELECT setup time to STRBD	(Note 1)			ns
t <sub>3</sub>	STRBD width	(t <sub>6</sub> + t <sub>7</sub> + t <sub>18</sub> )			ns
t <sub>4</sub>	MEM/REG, RD/WR setup time to IOEN	0	-	-	ns
t <sub>5</sub>	SELECT hold time following IOEN (Note 1)	0	-	-	ns
t <sub>6</sub>	SELECT + STRBD to IOEN delay (without contention)	75	-	160	ns
t <sub>6</sub>	SELECT + STRBD to IOEN delay (with contention)	-	-	1.80	μs
t <sub>7</sub>	IOEN to READY delay	115	125	150	ns
t <sub>8</sub>	IOEN to MEMENA-OUT delay	-	-	40	ns
t <sub>9</sub>	MEMENA-OUT to MEMENA-IN delay	-	-	50	ns
t <sub>10</sub>	IOEN to MEMWR delay	55	62.5	70	ns
t <sub>11</sub>	Address setup time to start of MEMWR	0	-	-	ns
t <sub>12</sub>	Data setup time to end of MEMWR	25	-	-	ns
t <sub>13</sub>	MEMWR pulse width	50	62.5	70	ns
t <sub>14</sub>	Address hold time following MEMWR high	0	-	-	ns
t <sub>15</sub>	Data hold time following MEMWR high	3	-	-	ns
t <sub>16</sub>	MEMENA-IN hold time following MEMWR high	0	-	-	ns
t <sub>17</sub>	READY pulse width	50	-	-	ns
t <sub>18</sub>	READY to STRBD release time	-	-	1.37	μs
t <sub>19</sub>	MEM/REG, RD/WR hold time following READY high	0	-	-	ns
t <sub>20</sub>	STRBD high delay to IOEN high	-	-	20	ns
t <sub>21</sub>	STRBD high delay to READY high (Note 2)	-	-	105	ns

#### NOTES:

1. SELECT and STRBD may be tied together. SELECT + STRBD must be sampled low for two consecutive falling edges of the 16 MHz clock when the BUS-61553's protocol/memory management logic is not using the data bus. When this occurs IOEN goes low, starting the transfer cycle. At this time, SELECT may be released high.
2. READY goes high after the first falling clock edge (satisfying t<sub>1</sub>) after STRBD goes high.

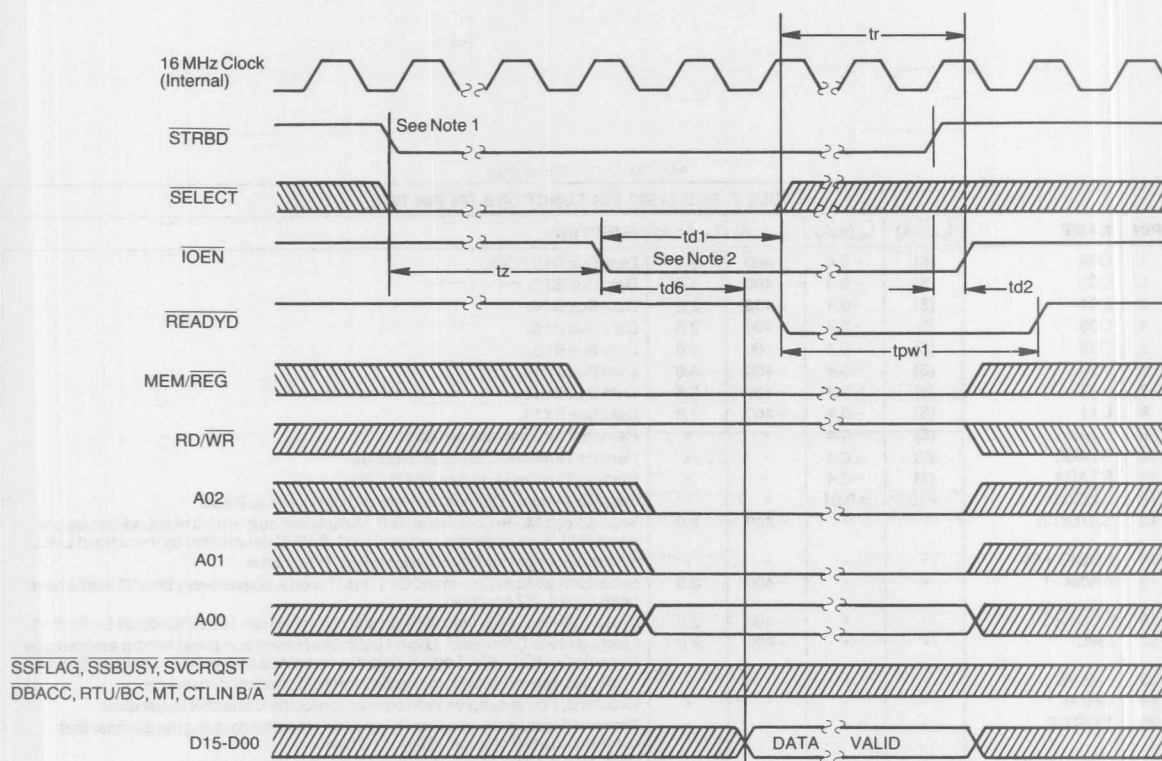
**FIGURE 31.**  
**CPU WRITES TO RAM TIMING**  
**(Shown for Internal RAM)**



Note:  
STRBD to IOEN (low) delay is two clock cycles. If contention occurs,  
delay is two clock cycles following release of bus.

CPU READS FROM EXTERNAL REGISTER				
SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td1	READYD low delay (CPU Handshake)	—	150	ns
td2	IOEN high delay (CPU Handshake)	—	20	ns
tpw1	READYD pulse width (CPU Handshake)	50	—	ns
td8	Register Data/Address set-up time	—	30	ns
tr	READYD to STRBD release	—	1.37	μs
tz	(SELECT • STRBD) to IOEN	—	1.8	μs

FIGURE 32. CPU READS FROM EXTERNAL REGISTER TIMING



Notes:

1. STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus (1.8  $\mu$ s max).
2. CPU must release STRBD within 1.5  $\mu$ s of IOEN going active. READY will go away within one clock cycle max.

CPU READS FROM INTERNAL REGISTER					
SYMBOL	DESCRIPTION	MIN	MAX	UNITS	
td1	READY low delay (CPU Handshake)	—	150	ns	
td2	IOEN high delay (CPU Handshake)	—	20	ns	
tpw1	READY pulse width (CPU Handshake)	50	—	ns	
td6	Internal Register delay (read)	—	60	ns	
tr	READY to STRBD release	—	1.37	$\mu$ s	
tz	(SELECT • STRBD) to IOEN	—	1.8	$\mu$ s	

FIGURE 33. CPU READS FROM INTERNAL REGISTER TIMING

TABLE 7. BUS-61553 PIN FUNCTIONS (78 PIN DIP)

PIN	NAME	$I_{IH} (\mu A)$	$I_{IL} (mA)$	$I_{OH} (\mu A)$	$I_{OL} (mA)$	FUNCTION
1	D00	(5)	-0.4	-400	3.6	Data Bus Bit 0 (LSB).
2	D02	(5)	-0.4	-400	3.6	Data Bus Bit 2.
3	D04	(5)	-0.4	-400	3.6	Data Bus Bit 4.
4	D06	(5)	-0.4	-400	3.6	Data Bus Bit 6.
5	D08	(5)	-0.4	-400	3.6	Data Bus Bit 8.
6	D10	(5)	-0.4	-400	3.6	Data Bus Bit 10.
7	D12	(5)	-0.4	-400	3.6	Data Bus Bit 12.
8	D14	(5)	-0.4	-400	3.6	Data Bus Bit 14.
9	RTAD1	(5)	-0.4	•	•	Remote Terminal Address Bit 1.
10	RTAD0	(5)	-0.4	•	•	Remote Terminal Address Bit 0 (LSB).
11	RTAD4	(5)	-0.4	•	•	Remote Terminal Address Bit 4 (MSB).
12	ILCMD	+10	$\pm 0.01$	•	•	Legal Command. Defines the received command as illegal.
13	SA/MC-0	•	•	-400	2.0	Subaddress/Mode Command Bit 0. Multiplexed output bit-0 of subaddress/word count field of the current command word. SA/MC determined by the state of LMC.
14	LOGIC +5V	•	•	•	•	+5V supply input for digital logic section. B6 counter.
15	SA/MC-1	•	•	-400	2.0	Subaddress/Mode Command Bit 1. In MT mode, pulses every time 32 words have been stored. B7 counter.
16	BCSTRCV	•	•	-400	2.0	Broadcast Received. Indicates current command is a 1553 Broadcast Command.
17	LMC	•	•	-400	2.0	Latched Mode Command. Logic 1 indicates current command word is a mode code and selects MC0-MC4. Logic 0 indicates non-mode command and selects SA0-SA4.
18	-15VB	•	•	•	•	-15V input power supply connection for the B channel transceiver.
19	GNDB	•	•	•	•	Ground B. Power supply return connection for the B channel transceiver.
20	TX/RX-B	•	•	•	•	Transmit/Receive transceiver-B. Input/output to the coupling transformer that connects to the B channel of the 1553 Bus.
21	LOGIC GND	•	•	•	•	Logic Ground. Power supply return for the digital logic section.
22	A01	(5)	-0.4	-400	3.6	Address Bit 1.
23	A03	(5)	-0.4	-400	3.6	Address Bit 3.
24	A05	(5)	-0.4	-400	3.6	Address Bit 5.
25	A07	(5)	-0.4	-400	3.6	Address Bit 7.
26	A09	(5)	-0.4	-400	3.6	Address Bit 9.
27	A11	(5)	-0.4	-400	3.6	Address Bit 11.
28	A13	(5)	-0.4	-400	3.6	Address Bit 13.
29	A15	(5)	-0.4	-400	3.6	Address Bit 15 (MSB).
30	MEMOE	•	•	-400	4.0	Memory Output Enable. A Logic 0 used to enable data output from memory when the 1553 or CPU reads from memory.
31	MEMENA-OUT	•	•	-400	4.0	Memory Enable Out. Low level output to enable external RAM. Used with MEMOE to read data or with MEMWR to write data into external RAM.
32	CLOCK IN	$\pm 20$	$\pm 0.02$	•	•	Clock Input. 16 MHz TTL clock.
33	MEM/REG	(6)	-0.7	•	•	Memory/Register. Input from CPU to select memory or register data transfer.
34	STRBD	(6)	-0.7	•	•	Strobe Data. Used in conjunction with SELECT to initiate a data transfer cycle to/from CPU.
35	EXTEN	•	•	-400	4.0	External Enable. Used to load data into external devices.
36	RD/WR	(6)	-0.7	•	•	Read/Write. Input from the CPU which defines the Data Bus transfer as a read or write operation.
37	EXTLD	•	•	-400	4.0	External load. Used to load data into external devices.
38	GNDA	•	•	•	•	Ground A. Power supply return connection for the A channel transceiver.
39	-15VA	•	•	•	•	-15V input power supply connection for the A channel transceiver.
40	TX/RX-A	•	•	•	•	Transmit/Receive transceiver-A. Input/output to the coupling transformer that connects to the A channel of the 1553 Bus.

**TABLE 7. BUS-61553 PIN FUNCTIONS (78 PIN DIP) (Continued)**

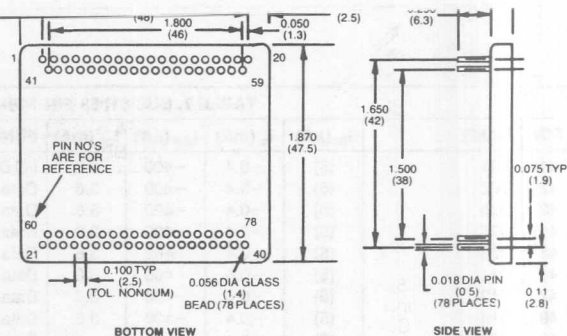
PIN	NAME	$I_{IH}$ ( $\mu A$ )	$I_{IL}$ (mA)	$I_{OH}$ ( $\mu A$ )	$I_{OL}$ (mA)	FUNCTION
41	D01	(5)	-0.4	-400	3.6	I/O Data Bus Bit 1.
42	D03	(5)	-0.4	-400	3.6	Data Bus Bit 3.
43	D05	(5)	-0.4	-400	3.6	Data Bus Bit 5.
44	D07	(5)	-0.4	-400	3.6	Data Bus Bit 7.
45	D09	(5)	-0.4	-400	3.6	Data Bus Bit 9.
46	D11	(5)	-0.4	-400	3.6	Data Bus Bit 11.
47	D13	(5)	-0.4	-400	3.6	Data Bus Bit 13.
48	D15	(5)	-0.4	-400	3.6	Data Bus Bit 15 (MSB).
49	RTAD3	(5)	-0.4	*	*	Remote Terminal Address Bit 3.
50	RTAD2	(5)	-0.4	*	*	Remote Terminal Address Bit 2.
51	RTADP	(5)	-0.4	*	*	Remote Terminal Address Parity Input.
52	SA/MC-2	*	*	-400	2.0	Subaddress/Mode Command Bit 2. B8 (MSB) counter.
53	SA/MC-4	*	*	-400	2.0	Subaddress/Mode Command Bit 4.
54	SA/MC-3	*	*	-400	2.0	Subaddress/Mode Command Bit 3.
55	THIS-RT	*	*	-400	2.0	Logic 0 pulse indicates receipt of a valid command word which contains the Remote Terminal address equivalent to the RTAD0-RTAD4 inputs.
56	RTPARERR	*	*	-400	2.0	RTU (address) Parity Error. Logic 0 indicates RTU address parity (odd parity: RTAD0-RTAD4, RTADP) has been violated.
57	T/R	*	*	-400	2.0	Transmit/Receive 1553 data. Latched T/R bit from current command word.
58	+5VB	*	*	*	*	+5V power supply connection for the B channel transceiver.
59	TX/RX-B	*	*	*	*	Transmit/Receive transceiver-B. Inverted I/O to coupling transformer that connects to channel B of the 1553 Bus.
60	A00	(5)	-0.4	-400	3.6	Address Bit 0 (LSB).
61	A02	(5)	-0.4	-400	3.6	Address Bit 2.
62	A04	(5)	-0.4	-400	3.6	Address Bit 4.
63	A06	(5)	-0.4	-400	3.6	Address Bit 6.
64	A08	(5)	-0.4	-400	3.6	Address Bit 8.
65	A10	(5)	-0.4	-400	3.6	Address Bit 10.
66	A12	(5)	-0.4	-400	3.6	Address Bit 12.
67	A14	(5)	-0.4	-400	3.6	Address Bit 14.
68	MEMWR	*	*	-400	4.0	Memory Write. Output pulse to write data into memory.
69	MEMENA-IN	$\pm 20$	$\pm 0.02$	*	*	Memory Enable In. Enables internal RAM only; connect directly to MEMENA-OUT.
70	INCMD	*	*	-400	2.0	In Command. Indicates BC or RTU currently in message transfer sequence.
71	MSTRCLR	(6)	-0.7	*	*	Master Clear. Power-on reset from CPU.
72	INT	*	*	-400	4.0	Interrupt. Interrupt pulse line to CPU.
73	IOEN	*	*	-400	4.0	Input/Output Enable. Output to enable external buffers/latches connecting the hybrid to the address/data bus.
74	SELECT	(6)	-0.7	*	*	Select. Input from the CPU. When active, selects BUS-61553 for operation.
75	READYD	*	*	-400	4.0	Ready Data. When active indicates data has been received from, or is available to, the CPU.
76	TAGEN	*	*	-400	4.0	Tag Enable. Enables an external time to counter for transferring the time tag word into memory.
77	+5VA	*	*	*	*	+5V input power supply connection for the channel A transceiver.
78	TX/RX-A	*	*	*	*	Transmit/Receive transceiver-A. Inverted I/O to the coupling transformer that connects to Channel A of the 1553 Bus.

**Notes:**

1.  $I_{IH}$  is specified at:  $V_{cc} = 5.5V$ ,  $V_{IH} = 2.7V$ .
2.  $I_{IL}$  is specified at:  $V_{cc} = 5.5V$ ,  $V_{IL} = 0.4V$ .
3.  $I_{OH}$  is specified at:  $V_{cc} = 4.5V$ ,  $V_{IH} = 2.4V$ .
4.  $I_{OL}$  is specified at:  $V_{cc} = 4.5V$ ,  $V_{IH} = 0.4V$ .
5. Internal Pull-up Resistor = 30K Ohms, typ.
6. Internal Pull-up Resistor = 16K Ohms, typ.
7. PIN 13 = B6, PIN 15 = B7, and PIN 52 = B8(MSB). B6, B7, and B8 are the MSB lines of an 8 BIT Counter used in the BC and MT mode to count 32 WORD TRANSFERS to memory (16 words received off the bus) for a total of 128 DATA and Tag words (in MT mode). (See page 17 for discussion.)

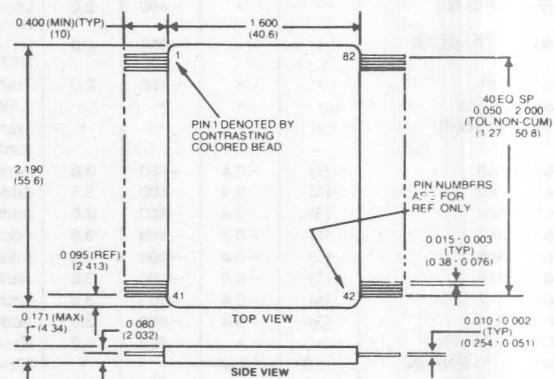


	FUNCTION	PIN	FUNCTION
1	NC	42	NC
2	D00	43	TX/RX-A
3	D01	44	TX/RX-A
4	D02	45	-15VA
5	D03	46	+5V
6	D04	47	GNDA
7	D05	48	TAGEN
8	D06	49	EXTLD
9	D07	50	READYD
10	D08	51	RD/WR
11	D09	52	SELECT
12	D10	53	EXTEN
13	D11	54	IOEN
14	D12	55	STRBD
15	D13	56	INT
16	D14	57	MEM/REG
17	D15	58	MSTRCLR
18	RTAD1	59	CLOCK IN
19	RTAD3	60	INCMD
20	RTAD0	61	MEMENA-OUT
21	RTAD2	62	MEMENA-IN
22	RTAD4	63	MEMOE
23	RTADP	64	MEMWR
24	ILLCMD	65	A15
25	SA/MC-2	66	A14
26	SA/MC-0	67	A13
27	SA/MC-4	68	A12
28	LOGIC +5V	69	A11
29	SA/MC-3	70	A10
30	SA/MC-1	71	A09
31	THIS-RT	72	A08
32	BCSTRCV	73	A07
33	RTPARERR	74	A06
34	LMC	75	A05
35	T/R	76	A04
36	-15VB	77	A03
37	+5VB	78	A02
38	GNDB	79	A01
39	TX/RX-B	80	A00
40	TX/RX-B	81	LOGIC GND
41	NC	82	NC



Note: Dimensions are in inches (millimeters).

FIGURE 34. MECHANICAL OUTLINE (DDIP)



Note: Dimensions are in inches (millimeters).

FIGURE 35. MECHANICAL OUTLINE (FLATPACK)

### ORDERING INFORMATION

BUS-61553-883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883.

B = Screened to MIL-STD-883 but without QCI testing.

κ = 0° to 70° C

Power Supply:

3 = -15V Transceivers

4 = -12V Transceivers

5 = +5V Transceivers - Call Factory

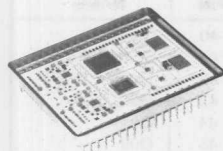
6 = Transceiverless - use with BUS-63102 II - Call Factory

Packaging:

5 = DDIP

6 = Flatpack

## MIL-STD-1553 ADVANCED INTEGRATED MUX (AIM) HYBRID



**PLEASE REFERENCE BUS-61555  
DATA SHEET FOR TIMING  
SPECIFICATIONS**

### DESCRIPTION

DDC's BUS-61555 Advanced Integrated Mux (AIM) Hybrid is a complete MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor (MT) device requiring only a +5 volt power supply. Packaged in a single 78 pin DIP package, the BUS-61555 contains dual low-power transceivers, complete BC/RTU/MT protocol logic, a MIL-STD-1553-to-host interface unit and an 8K x 16 RAM.

Using an industry standard dual transceiver and standard status and control signals, the BUS-61555 simplifies system integration at both the MIL-STD-1553 and host processor interface levels.

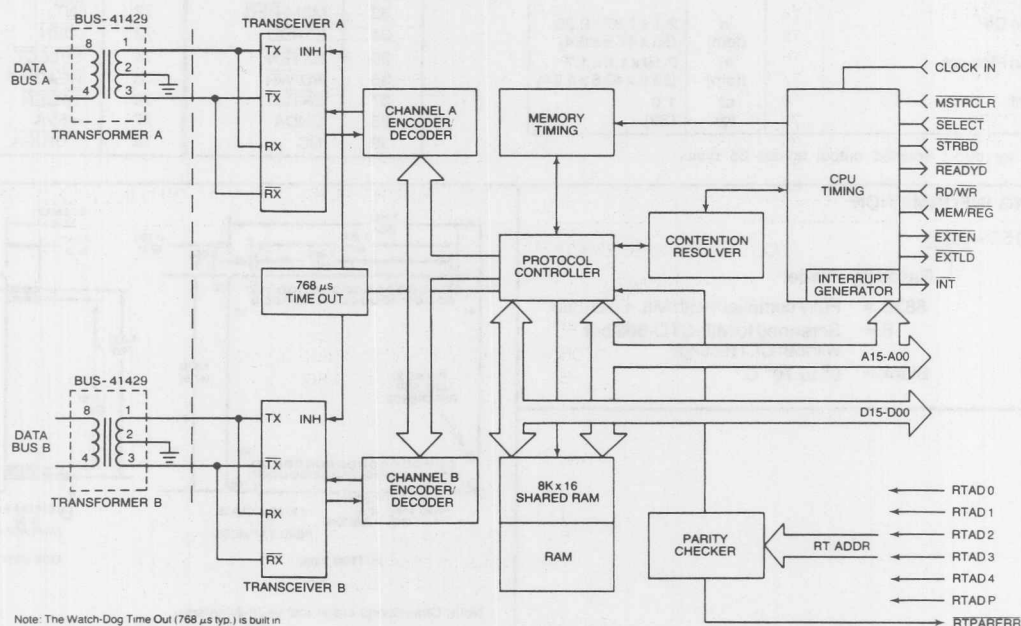
The CPU controls all 1553 operations by

accessing the shared 8K x 16 RAM. To ensure maximum design flexibility, memory control lines are provided for attaching external RAM to the BUS-61555 Address and Data Buses and for disabling internal memory; the total combined memory space can be expanded to 64K x 16. All 1553 transfers are entirely memory-mapped; thus the CPU interface requires minimal hardware and/or software support.

The BUS-61555 operates over the full military -55°C to +125°C temperature range. Available screened to MIL-STD-883, the BUS-61555 is ideal for demanding military and industrial microprocessor to 1553 interface applications.

### FEATURES

- +5 VOLT ONLY
- VERY LOW POWER
- COMPLETE INTEGRATED MUX INCLUDING:
  - LOW POWER DUAL TRANSCEIVER
  - BC/RTU/MT PROTOCOL
  - 8K x 16 SHARED RAM
  - INTERRUPT LOGIC
- COMPATIBLE WITH MIL-STD-1750 AND OTHER STANDARD CPUs
- MINIMIZES CPU OVERHEAD
- PROVIDES MEMORY MAPPED 1553 INTERFACE
- ON-LINE AND OFF-LINE SELF-TEST
- IBM PC <sup>®</sup> DEVELOPMENT TOOLS AVAILABLE



**FIGURE 1. BUS-61555 BLOCK DIAGRAM**

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TABLE 1. BUS-61555 SPECIFICATIONS

Specifications at nominal power supply voltages.		
PARAMETER	VALUE	NOTES
<b>RECEIVER</b>		
Differential Input Voltage	$V_{p-p}$	40 max
Differential Input Impedance	K Ohms	7 min
CMRR	dB	40 min
<b>TRANSMITTER (Direct Coupled)*</b>		
Differential Output Voltage	$V_{p-p}$	6.0 min, 9.0 max
Output Rise and Fall Times	n sec	100 min, 300 max
Output Offset Voltage	mV	±90 max
<b>LOGIC</b>		
$V_{IH}$	V	2.2 min
$V_{IL}$	V	0.8 max
<b>CLOCK</b>	MHz	16
<b>POWER SUPPLIES</b>		
+5V (Logic)	V	+5 ± 10%
+5VA (Chan A)	V	+5 ± 10%
+5VB (Chan B)	V	+5 ± 10%
Current Drain (Total Package)		(Typ)/max
$I_{dsc}$	mA	(70)/160
25% Duty Cycle	mA	(205)/310
50% Duty Cycle	mA	(340)/460
100% Duty Cycle	mA	(610)/760
<b>TEMPERATURE RANGE</b>		
Operating (Case)	°C	-55 to +125
Storage	°C	-65 to +150
<b>PHYSICAL CHARACTERISTICS</b>		
Size		
78 pin DIP	in (mm)	2.1 x 1.87 x 0.25 (53 x 47.5 x 6.4)
82 pin Flatpack	in (mm)	2.19 x 1.6 x 1.7 (55.6 x 40.6 x 4.34)
Weight	oz (g)	1.0 (29)

\*Given for direct coupled output across 35 ohms.

TABLE 2. BUS-61555 PIN OUTS

PIN	NAME	PIN	NAME
1	D00	40	TX/RX-A
2	D02	41	D01
3	D04	42	D03
4	D06	43	D05
5	D08	44	D07
6	D10	45	D09
7	D12	46	D11
8	D14	47	D13
9	RTAD1	48	D15
10	RTAD0	49	RTAD3
11	RTAD4	50	RTAD2
12	ILLCMD	51	RTADP
13	SA/MC-0	52	SA/MC-2
14	LOGIC +5V	53	SA/MC-4
15	SA/MC-1	54	SA/MC-3
16	BCSTRCV	55	THIS-RT
17	LMC	56	RTPARERR
18	NC	57	T/R
19	GNDB	58	+5VB
20	TX/RX-B	59	TX/RX-B
21	LOGIC GND	60	A00
22	A01	61	A02
23	A03	62	A04
24	A05	63	A06
25	A07	64	A08
26	A09	65	A10
27	A11	66	A12
28	A13	67	A14
29	A15	68	MEMWR
30	MEMOE	69	MEMENA-IN
31	MEMENA-OUT	70	INCMD
32	CLOCK IN	71	MSTRCLR
33	MEM/REG	72	INT
34	STRBD	73	IOEN
35	EXTEN	74	SELECT
36	RD/WR	75	READYD
37	EXTLD	76	TAGEN
38	GNDA	77	+5VA
39	NC	78	TX/RX-A

## ORDERING INFORMATION

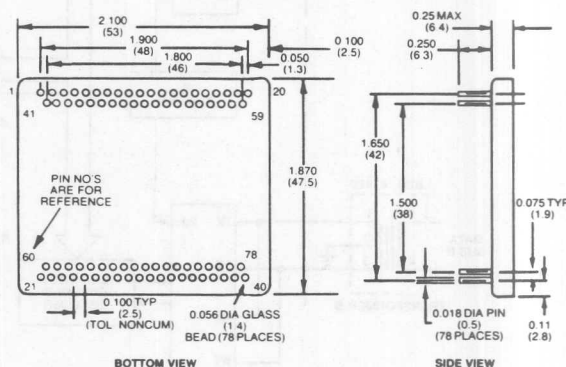
BUS-61555-883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883.

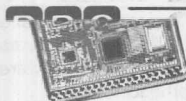
B = Screened to MIL-STD-883 but without QCI testing.

Blank = 0° to 70° C



Note: Dimensions are in inches (millimeters).

FIGURE 2. MECHANICAL OUTLINE (DDIP)



# INTEGRATED MUX HYBRIDS (AIM HY'ER)

CALL FOR UPDATED  
DATA SHEET.

## FEATURES

## DESCRIPTION

DDC's BUS-61559 series of Advanced Integrated Mux Hybrids with Enhanced RT Features (AIM HY'ER) comprise a complete interface between a microprocessor and a MIL-STD-1553B Notice 2 bus, implementing Bus Controller (BC), Remote Terminal (RT), and Monitor Terminal (MT) modes. Packaged in a single 78-pin DIP or 82-pin flat package, the BUS-61559 series contains dual low-power transceivers and encoder/decoders, complete BC/RT/MT protocol logic, memory management and interrupt logic, 8K X 16 of shared static RAM, and a direct, buffered interface to a host processor bus.

In addition to incorporating DDC's latest generation of low-power monolithic transceiver chips, the BUS-61559 includes a number of advanced features in support of MIL-STD-1553B Notice 2. Other salient features of the BUS-61559 serve to provide the benefits of reduced board space requirements, enhanced software flexibility, and reduced host processor overhead.

The BUS-61559 contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus. Alternatively, the buffers may be operated in a fully transparent mode in order to interface to up to 64K words of external shared RAM and/or connect directly to DDC's component set supporting the 20 MHz STANAG 3910 bus.

The memory management scheme for RT mode provides an option for separation of broadcast data, in compliance with 1553B Notice 2. A circular buffer option for RT message data blocks off-loads the host processor for bulk data transfer applications.

Other AIM HY'ER features include an internal Time Tag Register, an Interrupt Status Register, and internal command illegalization for RT mode.

The BUS-61559 series hybrids operate over the full military temperature range of -55°C to +125°C. Available screened to MIL-STD-883B, the hybrids are ideal for demanding military and industrial microprocessor-to-1553 applications.

- COMPLETE INTEGRATED 1553B NOTICE 2 BC, RT, AND MT INTERFACE
- FUNCTIONAL SUPERSET OF BUS-61553 SERIES
- INTERNAL ADDRESS AND DATA BUFFERS FOR DIRECT SHARED RAM INTERFACE TO PROCESSOR BUS
- RT SUBADDRESS CIRCULAR BUFFERS TO SUPPORT BULK DATA TRANSFERS
- OPTIONAL SEPARATION OF RT BROADCAST DATA
- INTERNAL INTERRUPT STATUS AND TIME TAG REGISTERS
- INTERNAL RT COMMAND ILLEGALIZATION

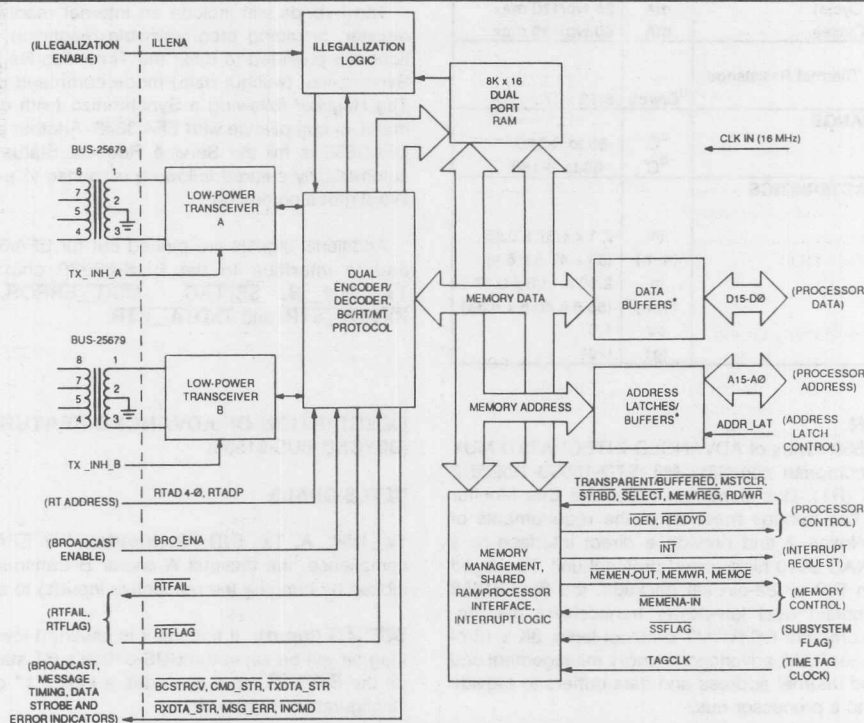


FIGURE 1. BUS-61559 BLOCK DIAGRAM

TABLE 1. BUS-61559 SERIES SPECIFICATIONS		
Specifications at Nominal Power Supply Voltages		
PARAMETER	UNITS	VALUE
<b>RECEIVER</b>		
Differential Input Voltage	Vp-p	40 max
Differential Input Impedance	Kohms	7 min
CMRR (through BUS-25679 transformer at 1.0 MHz)	db	50 min
<b>TRANSMITTER</b>		
Differential Output Voltage	Vp-p	6.0 min, 9.0 max
Direct Coupled	Vp-p	18 min, 27 max
Transformer Coupled	nsec	100 min, 300 max
Output Rise and Fall Times	mV	± 90 max
Output Offset Voltage(Direct Coupled)		
<b>LOGIC</b>		
V <sub>IH</sub>	Volts	2.2 min
V <sub>IL</sub>	Volts	0.8 max
<b>CLOCK</b>		
Frequency		
Nominal Value	MHz	16.0
Long Term Tolerance	%	± 0.1
Short Term Tolerance, 1 second	%	± 0.01
Duty Cycle	%	40 min, 60 max
<b>POWER SUPPLIES</b>		
+ 5V (Logic)	Volts	+ 5 ± 0.5
+ 5V (Transceivers)	Volts	+ 5 ± 0.5
-15V	Volts	-15 ± 1.5
Current Drain (Total Package)		
+ 5V (Idle)	mA	85 typ/170 max
-15V (Idle)	mA	45 typ/80 max
+ 5V (25% Duty Cycle)	mA	85 typ/170 max
-15V (25% Duty Cycle)	mA	80 typ/130 max
<b>THERMAL</b>		
Junction-To-Case Thermal Resistance (Hottest Die)	°C/watt	6.13
<b>TEMPERATURE RANGE</b>		
Operating (Case)	°C	-55 to +125
Storage	°C	-65 to +150
<b>PHYSICAL CHARACTERISTICS</b>		
Size		
78 pin DIP	in (mm)	2.1 x 1.87 x 0.25 (53 x 47.5 x 6.4)
82 pin Flatpack	in (mm)	2.19 x 1.60 x 0.17 (55.6 x 40.6 x 4.34)
Weight	oz (g)	1.0 (29)

## INTRODUCTION

DDC's BUS-61559 series of ADVANCED INTEGRATED MUX (AIM) HYBRIDS comprise complete MIL-STD-1553B Notice 2 Remote Terminal (RT), Bus Controller (BC), and Bus Monitor (MT) Terminals. The hybrids meet all of the requirements of MIL-STD-1553B Notice 2 and provide a direct interface to a BUS-63930 STANAG 3910 high-speed protocol unit. Packaged in a single 78-pin DIP or 82-pin flat package, the BUS-61559 series hybrids contain dual low-power transceivers and encoder/decoders, complete BC/RT/MT protocol logic, 8K x 16 of internal shared buffer RAM, advanced memory management and interrupt logic, and internal address and data buffers to provide a direct interface to a processor bus.

While maintaining functional and software compatibility to the BUS-61553 series AIM hybrids, the BUS-61559 incorporates a number of advanced features to support 1553B Notice 2 and EFA/ STANAG 3838. Additional benefits of these features include reduced board space requirements, enhanced software flexibility, and reduced host processor overhead.

The BUS-61559 series hybrids contain internal address latches and bidirectional data buffers to provide a direct interface to either a multiplexed or non-multiplexed processor bus. Alternatively, the buffers may be operated in a fully transparent mode in order to interface to the BUS-63930 chip and/or up to 64K x 16 of external shared RAM.

The memory management scheme for RT mode provides expanded capability beyond that of the BUS-61553 series hybrids. In compliance with 1553B Notice 2 and EFA/3838, data for broadcast messages may be optionally separated from non-broadcast received data. For each subaddress, either a single-message block or a variable-sized (128 to 8192 words) circular buffer may be allocated for data storage. In addition to helping to ensure for data consistency, the circular buffer feature provides a means of greatly reducing host processor overhead for bulk data transfer applications. End-of-message interrupts may be enabled either globally, on a Tx/Rx/Bcst subaddress basis, or when any particular subaddress circular buffer crosses its lower boundary and rolls over. An interrupt status register allows the host processor to determine the cause of an interrupt by means of a single read operation.

The hybrids will include an internal read/writable time tag register, providing programmable resolution. In addition, options are provided to clear the Time Tag Register following a Synchronize (without data) mode command or load the Time Tag Register following a Synchronize (with data) mode command, in compliance with EFA/3838. Another option to support EFA/3838 is for the Service Request Status Word bit to be automatically cleared following response to a Transmit Vector Word mode command.

Additional signals are pinned out for EFA/3838 compliance and to interface to the BUS-63930 chip: Tx\_INH\_A, Tx\_INH\_B, SSFLAG, MSG\_ERROR, CMD\_STR, RXDTA\_STR, and TXDTA\_STR.

## DESCRIPTION OF ADVANCED FEATURES (BEYOND BUS-61553)

### NEW SIGNALS

**Tx\_INH\_A, Tx\_INH\_B (inputs):** For EFA/STANAG 3838 compliance, the channel A and/or B transmitters may be inhibited by bringing the respective input(s) to a logic "1" level.

**SSFLAG (input):** If this input is asserted low, the Subsystem Flag bit will be set in the BUS-61559's RT status words. A low on the SSFLAG input overrides a logic "1" of the respective Configuration Register bit.



**TRANSPARENT/BUFFERED (input):** If this input is high, the buffers for the address and data buses operate in a transparent mode, functionally compatible to the BUS-61553. This supports an interface to BUS-63930 chip and/or external shared RAM. If this input is low, the address and data buffers provide isolation between the processor data/address buses and the internal memory data/address buses.

**MEMOE/ADDR\_LAT (output/input):** In the transparent mode, this pin provides a memory output enable (MEMOE) signal, similar to the same signal for the BUS-61553. In the buffered mode, this input puts the address latch/buffers for A15-A0 in the transparent mode when high or the latched mode when low.

**ILLENA (input):** Illegalization Enable. If connected to logic 1, designates shared RAM addresses 0300 - 03FF to be used for command illegalization in RT mode.

The following four signals are provided to allow a direct interface to BUS-63930 chip:

**MSG\_ERROR (output):** This output will be asserted as a low level following a word or format error and remain low until the start of the next message.

**CMD\_STR (output):** In RT mode, this output will pulse low for nominally 125 nsec when a received command word is on D15-D0.

**RXWDTA\_STR (output):** In RT mode, this output will pulse low for nominally 125 nsec when a data word received from the 1553 bus is on D15-D0.

**TXDTA\_STR (output):** In RT mode, this output will pulse low for nominally 500 nsec when a data word to be transmitted on the 1553 bus is required to be on D15-D0.

## BUFFERED PROCESSOR INTERFACE

As a means of reducing P.C. board space requirements, 16-bit address and data buffers are incorporated into the BUS-61559 hybrid.

As determined by the strapping of the input signal **TRANSPARENT/ BUFFERED**, the BUS-61559 processor interface may be configured for either of two modes.

In the transparent mode, the memory control signals **MEMWR**, **MEMOE**, **MEMENA-OUT** and **MEMENA-IN** operate as in the BUS-61553. The transparent mode must be used to interface to the BUS-63930 chip and/or up to 64K words of external shared RAM. Internal RAM access is determined by the **MEMENA-IN** input asserted low. External RAM access is specified by **MEMENA-IN** asserted high. In the transparent mode, the address buffers drive the CPU address onto the internal memory address bus for CPU transfers; for 1553 transfers, the internal memory address is asserted on the external address bus. The data buffers are directed outward for the CPU reading internal RAM (or register), for 1553 write accesses, or for 1553 read

accesses from internal RAM. The data buffers are directed inward (toward the memory data bus) for CPU write accesses to internal RAM or registers or the 1553 reading external RAM. The data buffers are disabled for the CPU accessing external RAM.

In the buffered interface mode, the shared memory is limited to the 8K x 16 of internal RAM. In this mode, the address and data buffers serve to isolate the external processor address/data buses from the internal memory address/data buses. The BUS-61559 supports a direct interface to a multiplexed processor bus by means of the input signal **ADDR\_LAT**. When this signal is high, the buffers for A15-A0 are in transparent mode. When **ADDR\_LAT** is low, the buffers for A15-A0 are in their latched mode. In the buffered mode, the address buffers are directed inward for CPU accesses and are disabled for 1553 accesses. The data buffers are directed inward for CPU write transfers, outward for CPU read transfers and are disabled for 1553 transfers.

## ADDITIONAL SOFTWARE CONTROLLABLE FEATURES (VIA CONFIGURATION REGISTER BITS)

The following Configuration Register bits are added, supplementing the bits of the BUS-61553 Configuration Register. All of these bits initialize to logic zero(0) following **MSTCLR** being brought low or software reset. This results in a mode of operation compatible to the BUS-61553.

### COMMON/SEPARATE LOOK-UP TABLE FOR BROADCAST MESSAGE DATA:

If this bit is low, the data pointers for both broadcast and non-broadcast receive messages are stored in a common area of the RT look-up table, as in the BUS-61553. If this bit is high, broadcast data is segregated from non-broadcast receive data by means of the separate areas of the RT look-up tables provided for broadcast messages. Refer to the section of this data sheet on Optional Broadcast Separation for more details.

### COMPATIBLE/ENHANCED RT MEMORY MANAGEMENT:

If this bit is low, the BUS-61559 RT memory management is compatible to the BUS-61553, providing a single data buffer for all transmit, receive and (optionally) broadcast subaddress. In this mode, each data block is repeatedly overread or overwritten. If this bit is set high, the BUS-61559 RT memory management capability is expanded to allow for either the "single-buffer" mode or for a variable-sized circular buffer (128 to 8192) words) for the individual transmit, receive or broadcast subaddresses. Refer to the section of this data sheet on Enhanced RT Memory Management for more details.

**CLEAR SERVICE REQUEST:** If this bit is low, the Service Request RT status word bit is under direct software control of the host processor, as in the BUS-61553. If the bit is high, the Service Request bit may still be set and cleared under software (register) control. In addition, the **SERVICE REQUEST** Configuration Register bit will automatically clear (go to logic 1)

after the BUS-61559 RT has responded to a Transmit Vector Word mode code command. That is, if the Clear Service Request bit is set to 1 while **SERVICE REQUEST** is set to 0, the RT will respond with the Service Request Status bit set for all commands until the RT processes a Transmit Vector Word command, with the Service Request still set. Following this message, **SERVICE REQUEST** in the Configuration Register automatically clears to a one. It stays high (cleared) for subsequent messages until it is re-asserted to a zero(0) by the host processor.

**PULSE/LEVEL INTERRUPT:** If this bit is low, the Interrupt Request output, **INT**, will be a negative pulse of approximately 500 nsec width. If this register bit is high, an interrupt will be requested by asserting **INT** as a low level. **INT** will be reset high when a "1" is written to the **INTERRUPT RESET** bit of the Start/Reset Register. The power turn-on mode for this bit is "0", enabling a pulse **INT** output.

**CLEAR TIME TAG FOLLOWING SYNCHRONIZE (WITHOUT DATA):** If this bit is set, reception of a Synchronize (without data) mode command will cause the value of the internal Time Tag Register to clear to 0000.

**LOAD TIME TAG FOLLOWING SYNCHRONIZE (WITH DATA):** If this bit is set, reception of a Synchronize (with data) mode command will cause the data word from the Synchronize message to be loaded into the internal Time Tag Register.

**CLEAR INTERRUPT STATUS REGISTER:** If this bit is set, the value of the Interrupt Status Register will clear to 0000 after it has been read by the host processor.

## ADDITIONAL START/RESET REGISTER BIT

**INTERRUPT RESET:** Writing a "1" to this bit resets the value of the Interrupt Status Register to 0000. In addition, if the **PULSE/LEVEL** Configuration Register bit is set to a "1", writing a "1" to this bit clears the **INT** output to a high level.

## ADDITIONAL INTERRUPT MASK REGISTER BITS

The following interrupt conditions are added to the Interrupt Mask Register:

**TIME TAG ROLLOVER:** If set, enables an interrupt if the 16-bit Time Tag Register rolls over from FFFF to 0000.

**RT SUBADDRESS CONTROL WORD EOM:** If this bit is set and the BUS-61559 is in the Enhanced Memory Management RT mode and the "Interrupt at EOM" bit is set in the subaddress control word for the respective Tx/Rx/Bcst subaddress, an interrupt will occur at the end of the current message.

**RT SUBADDRESS CIRCULAR BUFFER ROLLOVER:** If this bit is set and the BUS-61559 is in the Enhanced Memory Management RT mode and the "Interrupt at Rollover" bit is set in the

subaddress control word for the respective Tx/Rx/Bcst subaddress, an interrupt will occur at the end of the current message if the data look-up address pointer crossed the lower boundary of the respective circular buffer, resulting in a rollover.

## INTERRUPT STATUS REGISTER:

The Interrupt Status Register will allow the host processor to determine the cause of an interrupt request by means of a single read operation. There are nine (9) bits in this register. This register will be cleared after it has been read, if the **CLEAR INTERRUPT STATUS REGISTER** Configuration Register bit is set.

The nine bits of this register are: **MASTER INTERRUPT**, **EOM**, **BC EOM**, **FORMAT ERROR**, **STATUS SET**, **R.T. ADDRESS PARITY ERROR**, **TIME TAG ROLLOVER**, **RT SUBADDRESS CONTROL WORD EOM**, AND **RT SUBADDRESS CIRCULAR BUFFER ROLLOVER**.

**MASTER INTERRUPT** is in bit position 15 (MSB). **MASTER INTERRUPT** will be set if any of the other bits of the Interrupt Status Register are set. The other eight bits align with the respective bit positions of the Interrupt Mask Register.

## OPTIONAL BROADCAST SEPARATION AND ENHANCED RT MEMORY MANAGEMENT

(Reference Tables 2.3, and Figure 2)

In order to comply with Notice 2 of MIL-STD-1553B and the EFA implementation of STANAG 3838, the BUS-61559 provides enhanced RT memory management capabilities beyond those of the BUS-61553. These new features allow broadcast message data to be separated from non-broadcast receive data, help to ensure data consistency for transmitted and received data blocks and serve to offload the host processor for bulk data transfer applications.

As in the BUS-61553, the BUS-61559 provides a global double buffering mechanism by means of bit 13, **CURRENT AREA A/B**, of the Configuration Register. At any point in time, this allows for one stack pointer, stack area, look-up table and set of data blocks to be designated as "active" (used for the processing of 1553 messages) and the alternate set of respective data structures to be designated as "non-active". Both the "active" and "non-active" RAM areas are **always accessible** by the host processor.

Referring to Table 2, the RT lookup tables are expanded beyond those of the BUS-61553. In the 61553, the look-up tables are 64 words each, containing the look-up table pointers for the 32 receive subaddresses and the 32 transmit subaddresses. For the BUS-61559, there are an additional 64 words in each of the two look-up tables. Thirty two (32) of these words provide optional separation of broadcast messages. The last 32 words

are subaddress control words, one appropriated for each RT subaddress.

TABLE 2. RT LOOK-UP TABLES			
AREA A	AREA B	DESCRIPTION	COMMENT
0140	01C0	Rx(/Bcst)_SA0	Receive (/Broadcast) Lookup Table
015F	01DF	Rx(/Bcst) SA31	
0160	01E0	Tx_SA0	
			Transmit Lookup Table
017F	01FF	Tx SA31	
0180	0200	Bcst_SA0	
			Broadcast Lookup Table (Optional)
019F	021F	Bcst SA31	
01A0	0220	SACW_SA0	
			Subaddress Control Word Lookup Table (Optional)
01BF	023F	SACW SA31	

Referring to Table 3, in the Enhanced RT Memory Management mode, each of the 32 subaddress control words specifies the memory management and interrupt schemes for the respective subaddress. For each Subaddress Control Word, five bits control the memory management scheme and interrupts for each of transmit, receive and (optionally separated) broadcast messages.

For each transmit (or receive or broadcast) subaddress, three bits specify the memory management scheme. The scheme may be selected as "single buffer" (as in the BUS-61553 or "compatible" mode), or "circular buffer". In the single buffer mode, a single data block is repeatedly overread (for transmit data) or overwritten (for receive or broadcast data). Alternatively, in the circular buffer mode, data words for successive messages to/from any particular Tx/Rx/Bcst subaddresses are read from or written to the next contiguous block of locations in the respective circular buffer. The size of the circular buffer for each transmit, receive, or broadcast subaddress may be programmed as 128, 256, 512, 1024, 2048, 4096, or 8192 words. For each Tx/Rx/Bcst subaddress, two bits of the subaddress control word are used to enable interrupts. One of these bits will result in an interrupt following every message directed to the respective Tx/Rx/Bcst subaddress. The other of these two bits will result in an interrupt at the end of a message if the message resulted in the look-up table pointer crossing the lower boundary of the circular buffer, rolling over to the top of the buffer.

Table 3a. SUBADDRESS CONTROL WORD		
BIT	DESCRIPTION	COMMENT
15	NOT USED	—
14	TRANSMIT MESSAGE CONTROL	See Table 3b. 5-bit Tx/Rx/Bcst SUBADDRESS CONTROL FIELD
10		
9		
5	RECEIVE (/BROADCAST) MESSAGE CONTROL	See Table 3b. 5-bit Tx/Rx/Bcst SUBADDRESS CONTROL FIELD
4		
0		
	BROADCAST MESSAGE CONTROL (OPTIONAL)	See Table 3b. 5-bit Tx/Rx/Bcst SUBADDRESS CONTROL FIELD

Table 3b.		
5-bit Tx/Rx/Bcst SUBADDRESS CONTROL FIELD		COMMENT
* INTERRUPT ON EOM (MSB)		See Table 3c. MEMORY MANAGEMENT SCHEME FOR Tx/Rx/Bcst
* INTERRUPT ON EOM FOLLOWING CIRCULAR BUFFER ROLLOVER		
* MM2 (MEMORY MANAGEMENT 2)		
* MM1 (MEMORY MANAGEMENT 1)		
* MM0 (MEMORY MANAGEMENT 0) (LSB)		

Table 3c. MEMORY MANAGEMENT SCHEME FOR Tx/Rx/Bcst				
MM2	MM1	MM0	DESCRIPTION	COMMENT
0	0	0	SINGLE BUFFER	CIRCULAR BUFFER OF SPECIFIED SIZE
0	0	1	128-WORD	
0	1	0	256-WORD	
0	1	1	512-WORD	
1	0	0	1024-WORD	
1	0	1	2048-WORD	
1	1	0	4096-WORD	
1	1	1	8192-WORD	

The operation of the circular buffer RT memory management mode is illustrated in Figure 2. As in the "compatible" (BUS-61553) mode, the individual Look-up Table entries are initially loaded by the host processor. At the start of each message, the lookup table entry is stored in the third position ("RESERVED" for BUS-61553) of the respective message block descriptor in the stack area of RAM. Receive or transmit data is transferred to (from) the circular buffer, starting at the location referenced by the lookup table pointer. At the end of a **valid** message, the location **after** the last word accessed for the message is stored into the respective lookup table location. In this way, data for the **next** message for the respective Tx/Rx/Bcst subaddress will be accessed to/from the next lower contiguous block of locations in the circular buffer. If there is an error in the message, the lookup table pointer will **not** be updated at the end of the message. This allows failed messages in a bulk data transfer to be retried without intervention by the RT's host processor.

When the pointer reaches the lower boundary of the circular buffer (located at 128, 256, . . . 8192-word boundaries in the shared RAM address space), the pointer moves to the top boundary of the circular buffer, as shown in Figure 2.

It should be noted that the pointer to the start of the RT message block is stored in the third location of the message block descriptor (in the stack) for the "compatible" (BUS-61553) single buffer mode as well as for the circular buffer mode.

## INTERNAL TIME TAG

One of the requirements of the EFA implementation of STANAG 3838 is to provide a "Synchronization" clock, or real time clock. The internal read/writable Time Tag Register of the BUS-61559 fulfills this requirement.

The resolution of the Time Tag Register is software programmable. The choices for resolution are 2, 4, 8, 16, 32, 64, or "EXTERNAL"  $\mu\text{s}/\text{LSB}$ . In the "EXTERNAL" mode, the Time Tag Register is clocked from an external oscillator by means of the TAGCLK input.

If the "CLEAR TIME TAG FOLLOWING SYNCHRONIZE (WITHOUT DATA)" and/or the "LOAD TIME TAG FOLLOWING SYNCHRONIZE WITH DATA" Configuration Register bit(s) are set, the Time Tag Register will be cleared or loaded (from the received data word) following reception of the respective mode code command.

If the TIME TAG ROLLOVER bit of the Interrupt Mask Register is set, an interrupt request will be issued when the Time Tag Register rolls over from FFFF to 0000.

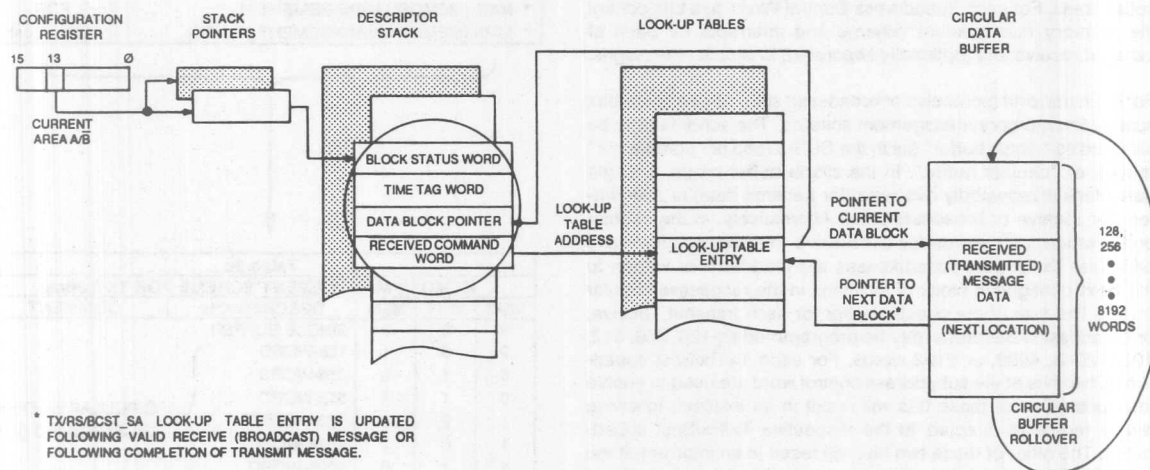


FIGURE 2. R.T. MEMORY MANAGEMENT – USING CIRCULAR BUFFER



## BUS-61559 INTERFACE TO BUS-63930 STANAG 3910 HIGH-SPEED PROTOCOL CHIP

(Reference Figures 3 and 4)

Figure 3 illustrates a block diagram of a complete STANAG 3838 BC/RT/MT and STANAG 3910 remote terminal. The 3838 BC/RT/MT is comprised of the DDC BUS-61559 hybrid and the two BUS-25679 transformers. The 61559 is configured in the transparent mode, interfacing to the host processor by means of external data and address buses.

The STANAG 3910 remote terminal is comprised of a BUS-63930 high-speed RT protocol chip, BUS-63920 data recovery unit, and BUS-63910 fiber optic transceiver. High-speed message RAM, up to a maximum of 2 Mwords, interface to the BUS-63930 through internally buffered address and data buses.

Figure 4 provides a more detailed interconnection drawing, interfacing a host processor to the BUS-61559 and to the BUS-63930. The BUS-63930 operates by monitoring the data, address, and various control signals. The control signals monitored

by the BUS-63930 are: CMD\_STR, TXDTA\_STR, RXDTA\_STR, MSG\_ERROR, BCSTRCV, and MEMENA-OUT. In addition, the BUS-63930 provides the MEMENA-IN input to the BUS-61559.

In operation, the BUS-63930 monitors for received Command Words to the high-speed subaddress and for high-speed Action Words being transferred to the low-speed RAM, internal to the BUS-61559. In the transparent mode, these transfers may be monitored on the BUS-61559's external address and data buses. The BUS-63930 performs all high-speed protocol operations, transmitting and receiving messages over the 3910 fiber optic bus (via the BUS-63920 and BUS-63910). When the BUS-61559 receives a transmit command to the high-speed subaddress, the BUS-63930 observes the command and provides the High-Speed Status Word, BIT Word, and the last Action Word (and possibly up to 29 additional data words) over the BUS-61559's data bus. When it does this, it presents the MEMENA-IN input to the BUS-61559 high, de-selecting the BUS-61559 internal RAM. The BUS-61559 then responds over the 3838 bus with the data words provided by the BUS-63930.

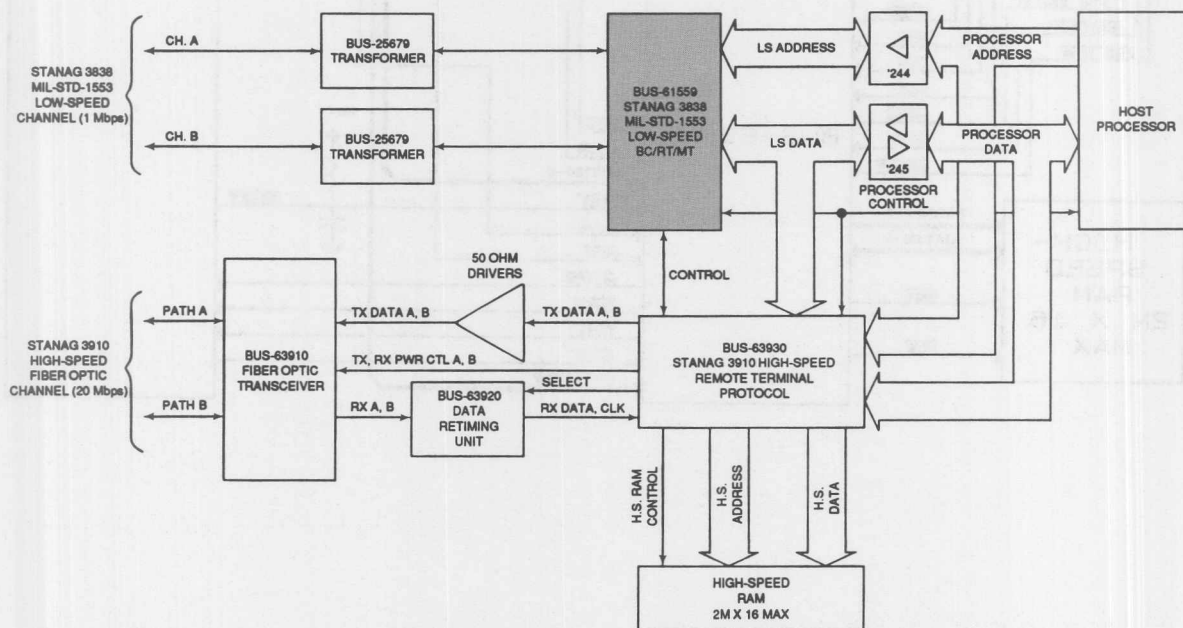


FIGURE 3. STANAG 3838/3910 BLOCK DIAGRAM



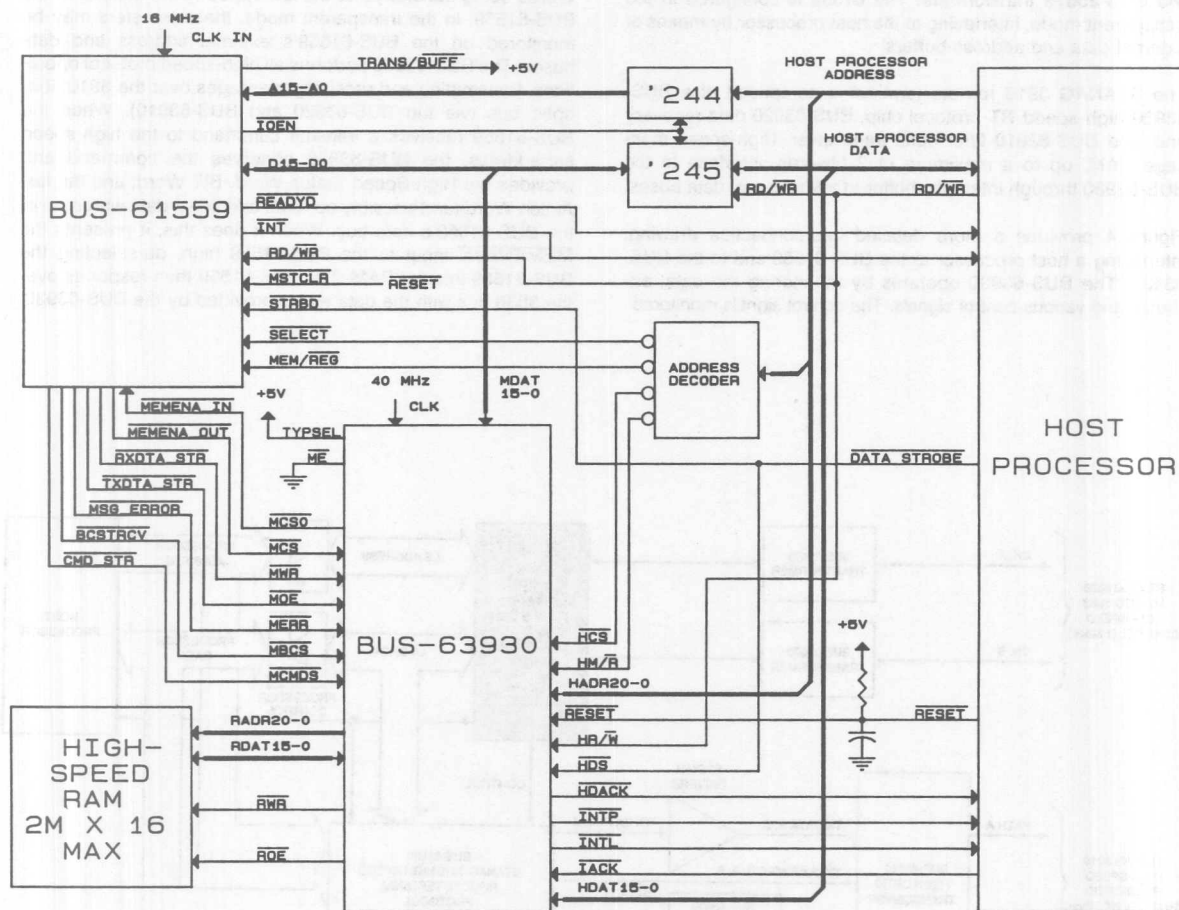
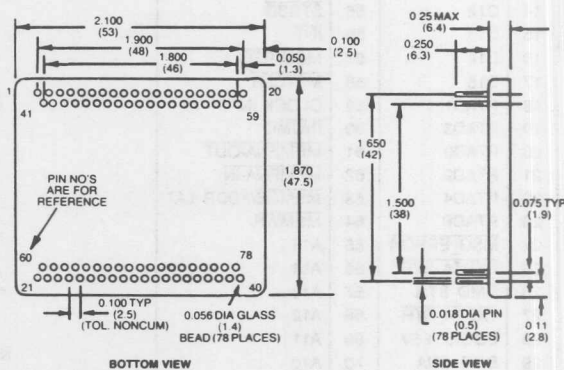


FIGURE 4. BUS-61559/BUS-63930 INTERCONNECTION DIAGRAM

TABLE 4.  
PIN ASSIGNMENTS (DDIP)BUS-61559

PIN	NAME	PIN	NAME
1	D00	40	TX/RX-A
2	D02	41	D01
3	D04	42	D03
4	D06	43	D05
5	D08	44	D07
6	D10	45	D09
7	D12	46	D11
8	D14	47	D13
9	RTAD1	48	D15
10	RTAD0	49	RTAD3
11	RTAD4	50	RTAD2
12	MSG ERROR	51	RTADP
13	CMD STR	52	RXDTA_STR
14	LOGIC +5V	53	TXDTA_STR
15	TAGCLK	54	BRO_ENA
16	BCSTRCV	55	RTFAIL
17	ILLENA	56	RTFLAG
18	-15V B	57	TX_INH_B
19	GND B	58	+5V B
20	TX/RX-B	59	TX/RX-B
21	LOGIC GND	60	A00
22	A01	61	A02
23	A03	62	A04
24	A05	63	A06
25	A07	64	A08
26	A09	65	A10
27	A11	66	A12
28	A13	67	A14
29	A15	68	MEMWR
30	MEMOE/ADDR_LAT	69	MEMENA-IN
31	MEMENA-OUT	70	INCMD
32	CLOCK IN	71	MSTCLR
33	MEM/REG	72	INT
34	STRBD	73	IOEN
35	TRANSP/BUFF	74	SELECT
36	RD/WR	75	READYD
37	SSFLAG	76	TX_INH_A
38	GND A	77	+5V A
39	-15V A	78	TR/RX A

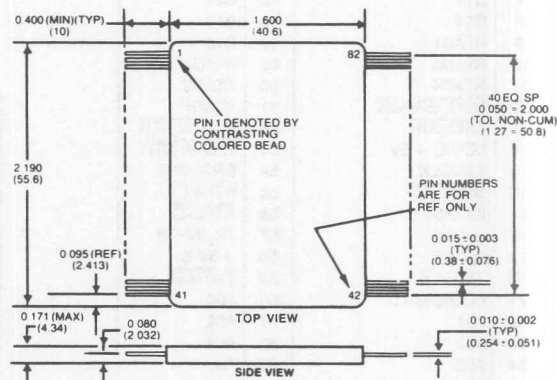


Note: Dimensions are in inches (millimeters).

FIGURE 5. MECHANICAL OUTLINE (DDIP)

TABLE 5.  
PIN ASSIGNMENTS  
FLATPACK BUS-61569

PIN	NAME	PIN	NAME
1	NC	42	NC
2	D00	43	TX/RX-A
3	D01	44	TX/RX-A
4	D02	45	-15V (-12V) XCVR
5	D03	46	+ 5V XCVR
6	D04	47	GND A
7	D05	48	TX_INH_A
8	D06	49	SSFLAG
9	D07	50	READYD
10	D08	51	RDWR
11	D09	52	SELECT
12	D10	53	TRANSP/BUFF
13	D11	54	IOEN
14	D12	55	STRBD
15	D13	56	INT
16	D14	57	MEM/REG
17	D15	58	MSTCLR
18	RTAD1	59	CLOCK IN
19	RTAD3	60	INCMD
20	RTAD0	61	MEMENA-OUT
21	RTAD2	62	MEMENA-IN
22	RTAD4	63	MEMOE/ADDR_LAT
23	RTADP	64	MEMWR
24	MSG_ERROR	65	A15
25	RXD <sub>TA</sub> _STR	66	A14
26	CMD_STR	67	A13
27	TXD <sub>TA</sub> _STR	68	A12
28	LOGIC + 5V	69	A11
29	BRO_ENA	70	A10
30	TAGCLK	71	A09
31	RTFAIL	72	A08
32	BCSTRCV	73	A07
33	RTFLAG	74	A06
34	ILLENA	75	A05
35	TX_INH_B	76	A04
36	-15V B	77	A03
37	+ 5V B	78	A02
38	GND B	79	A01
39	TX/RX-B	80	A00
40	TX/RX-B	81	LOGIC GND
41	NC	82	NC



Note: Dimensions are in inches (millimeters).

**FIGURE 6. MECHANICAL OUTLINE (FLATPACK)**

## ORDERING INFORMATION

BUS- 61559 - 883B

Reliability Grade:

883B = Fully compliant with  
MIL-STD-883

B = Screened to MIL-STD-883  
but without QCI testing

Blank = 0° to 70° C operation

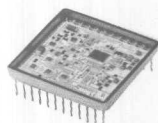
Power Supply and Packaging\*:

59 = +5V/-15V DDIP

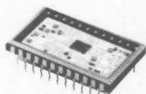
69 = +5V/-15V Flatpack

\* Consult factory for other voltage and packaging options.

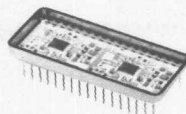
## MIL-STD-1553 DATA BUS SINGLE AND DUAL TRANSCEIVERS



BUS-63102 II



BUS-63105 II



BUS-63125 II

### DESCRIPTION

The BUS-63100 II transceivers are complete transmitter and receiver pairs conforming fully to MIL-STD-1553A and 1553B. Features available with selected models of this high reliability series include: Smiths and Harris interface type choices,  $\pm 12V/\pm 15V$  power supply voltage range, variable threshold levels, and single (24 pin DDIP or square) and completely independent dual redundant (36 pin DDIP) packaging configurations. All models are also available in flatpacks.

The receiver section of the BUS-63100 II series accepts phase-modulated bipolar data from a MIL-STD-1553 Data Bus and produces TTL signal data at its outputs: RX Data Out and RX Data Out. These outputs represent positive and negative variations of the input data sig-

nals beyond an internally fixed or externally set threshold level. An external STROBE input enables or disables the receiver outputs.

The transmitter section accepts bipolar TTL signal data at its TX Data and TX Data input lines and produces phase-modulated bipolar data at the TX Data and TX Data outputs. The transmitters' output voltage level is typically 28Vpp to 30Vpp. An external input, INHIBIT, takes priority over the transmitter inputs and disables the transmitter when activated with a logic "1".

The small size and different model capabilities available with the BUS-63100 II series simplify engineering design, making it an excellent choice for interfacing with any MIL-STD-1553 system.

### FEATURES

- CONFORMS FULLY TO MIL-STD-1553A AND 1553B
- SOME MODELS AVAILABLE TO MILITARY (DESC) DRAWINGS
- MODEL CAPABILITIES:  
SINGLE OR DUAL  
REDUNDANT PACKAGING  
– 12V/– 15V POWER SUPPLY  
VOLTAGE RANGE AVAILABLE  
HARRIS OR SMITHS I/O  
COMPATIBILITY
- SMALL SIZE:  
SINGLE – 24 DDIP OR SQUARE  
DUAL – 36 DDIP FLATPACKS
- LOW POWER
- HIGH RELIABILITY – LSI

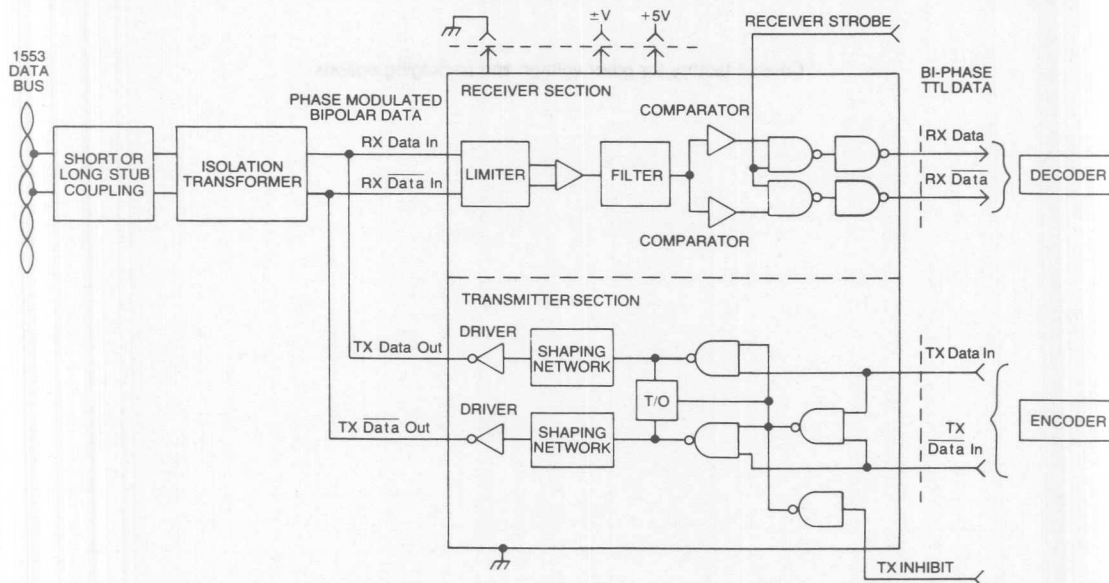


FIGURE 1. BUS-63100 II SERIES BLOCK DIAGRAM



## GENERAL

The BUS-63100 II series offers complete transmitter and receiver pairs packaged in either single or dual redundant form which are designed for use in any MIL-STD-1553 application.

Figure 1 illustrates a BUS-63100 II series transceiver with connections to a MIL-STD-1553 Data Bus. Once transformer isolated, coupling to a MIL-STD-1553 Data Bus can be either short stub (direct) or long stub (transformer). Figure 2 illustrates the different configurations and lists the recommended DDC transformer bus product for use with each model.

## TRANSCIVER CAPABILITIES

DDC's BUS-63100 II series of transceivers offer a wide range of capabilities (on selected models) which include: power supply voltage levels, packaging configurations, Smiths or Harris type Encoder/Decoder direct compatibility, and internal (pre-set) and/or external (adjustable) threshold levels. The capabilities of the different models are described in the following paragraphs and summarized in table 1.

## Power Supply Voltages

Power supply voltage requirements on BUS-63102 II and BUS-63104 II are met over a range from  $\pm 12V$  to  $\pm 15V$ . All models operate with either  $-12V$  or  $-15V$  supplies. All models require  $+5V$  supply. See table 1.

## Packaging Configurations

Single transceivers, BUS-63102 II and BUS-63104 II are packaged in 24 pin square packages, all other single transceivers are packaged in 24 pin DDIPs. Dual transceivers are packaged in 36 pin DDIPs.

## Encoder/Decoder Compatibility

BUS-63105II, BUS-63107II, BUS-63125 II, and BUS-63127 II are directly compatible to Harris 15530 type of Encoder/Decoders. All other transceivers are directly compatible to Smiths type. Transceivers which are directly compatible with one type can be converted for use with the other by simply switching the output lines, RX Data and RX Data, and inverting their signals by means of external inverting gates.

## Waveforms

All transceivers conform fully to MIL-STD-1553 requirements. BUS-63102 II additionally conforms to MACAIR standards, producing sinusoidal waveforms at 1MHz.

## Threshold Levels

All models offer internal (factory preset) threshold levels. BUS-63102 II and BUS-63104 II additionally offer externally set threshold levels. These external threshold levels are adjustable from 0V to 2V, with the use of two external 10K Ohm potentiometers (see figure 5).

## TRANSMIT OPERATING MODE

The transmitter section accepts encoded TTL data and converts this data to phase-modulated bipolar form by means of a wave-shaping network and driver circuitry. These driver outputs are coupled to a MIL-STD-1553 Data Bus via a transformer which is driven from the TX Data Out and TX Data Out terminals. These output terminals can be put into a high impedance state when transmitting by enabling INHIBIT (logic '1'), or by placing both inputs at the same logic level. Table 2, Transmit Operating Mode, lists the functions for the output data and input data in reference to the state of INHIBIT.

The transceivers are able to operate in a "wraparound" mode. This allows output data to be monitored by the receiver section and returned to the decoder where it can be checked for errors.

TABLE 2. TRANSMIT OPERATING MODE

TX Data In	TX Data In	TX INHIBIT	DRIVER OUTPUT <sup>(2)</sup>
X <sup>(1)</sup>	X	H	OFF <sup>(3)</sup>
0	0	X	OFF
0	1	L	ON
1	0	L	ON
1	1	X	OFF

Notes:

(1) X = Don't care.

(2) DRIVER OUT = TX Data Out and TX Data Out.

(3) DRIVER OUTPUT terminals are in the high impedance mode during OFF time, independent of INHIBIT status.

## BUS-63100 II SERIES SPECIFICATIONS

Specifications for all transceivers are listed in table 3.

TABLE 1. TRANSCIVER CAPABILITIES

	$\pm 12VDC$ to $\pm 15VDC$	$-12VDC$	$-15VDC$	24 PIN DDIP	24 PIN SQUARE	36 PIN DDIP	I/O COMPATIBILITY		THRESHOLD		MACAIR	MIL-STD- 1553	FLATPACK MODEL NO.
							SMITHS	HARRIS	INT	EXT			
<b>Single</b>													
BUS-63102 II	●				●		●		●	●	●	●	BUS-63112 II
BUS-63104 II	●				●		●		●	●		●	BUS-63114 II
BUS-63105 II			●	●				●	●			●	BUS-63106 II
BUS-63107 II		●		●				●	●			●	BUS-63108 II
BUS-63115 II			●	●			●		●			●	BUS-63116 II
BUS-63117 II		●		●			●		●			●	BUS-63118 II
<b>Dual</b>													
BUS-63125 II			●			●		●	●			●	BUS-63126 II
BUS-63127 II		●				●		●	●			●	BUS-63128 II
BUS-63135 II			●			●	●		●			●	BUS-63136 II
BUS-63137 II		●				●	●		●			●	BUS-63138 II

TABLE 3. BUS-63100 II SPECIFICATIONS

TRANSCEIVER NUMBER	BUS-63102 II <sup>(1)</sup> BUS-63112 II		BUS-63104 II BUS-63114 II	BUS-63105 II † BUS-63106 II	BUS-63115 II BUS-63116 II	BUS-63107 II BUS-63108 II	BUS-63117 II BUS-63118 II
CHANNELS	Single		Single	Single	Single	Single	Single
POWER SUPPLIES	±12V to ±15V		±12V to ±15V	–15V	–15V	–12V	–12V
ENCODER/DECODER INTERFACE TYPE	Smiths		Smiths	Harris	Smiths	Harris	Smiths
MATCHING TRANSFORMER MODEL	BUS-27765		BUS-27765	BUS-25679	BUS-25679	BUS-29854	BUS-29854
RECEIVER							
Strobe	1 'LS Load	*		1TTL	*	*	*
Input Level	40Vpp, Diff, max	*		*	*	*	*
Threshold Level (Internal) <sup>(2)(3)</sup>	0.5Vpp min, 1.0Vpp max	*		0.56Vpp min, 1.0Vpp max	*	*	*
CMRR	40 db, min	*		*	*	*	*
Input Resistance-Diff	7K Ohm, min	*		*	*	*	*
Input Capacitance-Diff	5pf, max	*		*	*	*	*
Output Fan Out	10 TTL Loads	*		*	*	*	*
TRANSMITTER							
TX Inhibit	1 'LS Load	*		1TTL	*	*	*
Input Level	1 'LS Load	*		1TTL	*	*	*
Output Level (Direct Coupled) <sup>(4)</sup>	29Vpp, nom	*		*	*	*	*
	across 140 Ohm load	*		*	*	*	*
Rise/Fall Time	280ns, typ	150ns, typ		125ns, typ	*	115ns, typ	*
Output Noise	10mVpp, Diff, max	*		*	*	*	*
Output Offset Voltage	±90mVpp, max across	*		*	*	*	*
	35 Ohm load	*		*	*	*	*
Output Impedance – Non-Transmitting							
Output Resistance-Diff	10K Ohm, min	*		*	*	*	*
Output Capacitance-Diff	5pf, max	*		*	*	*	*
LOGIC							
TTL/CMOS Compatible							
All Inputs	2 'LS Loads, max	*		1 TTL	*	*	*
All Outputs	10 TTL Loads, min	*		*	*	*	*
POWER SUPPLY REQUIREMENTS							
	+5V ±10%	+12V to +15V ±5%	–12V to –15V ±5%	+5V ±10%	–15V ±5%	+5V ±10%	–12V ±5%
Non-Transmitting – (typ/max)	30/45mA	24/30mA	51/65mA	30/45mA	40/60mA	30/45mA	40/60mA
Transmitting – 50% duty cycle (typ/max)	30/45mA	85/114mA	118/135mA	30/45mA	75/100mA	30/45mA	95/125mA
Transmitting – 100% duty cycle (typ/max)	30/45mA	140/180mA	175/195mA	30/45mA	150/195mA	30/45mA	190/245mA
THERMAL							
Operating Junction Temperature	–55°C to +160°C	*		*	*	*	*
Operating Case Temperature	–55°C to +125°C	*		*	*	*	*
Storage Temperature	–65°C to +150°C	*		*	*	*	*
Thermal Impedance –							
Junction to Case	40°C/W (Hottest Die)	*		7.0°C/W	*	*	*
Case to Air (typ)	21°C/W (24 Pin Square)	*		30°C/W (24 Pin DDIP)	*	30°C/W (24 Pin DDIP)	*
POWER DISSIPATION							
Single Channel	12V Supply	15V Supply		15V Supply	*	12V Supply	*
Non-Transmitting – (typ/max)	1.05/1.37W	1.28/1.58W		0.90/1.35W	*	0.78/1.18W	*
Transmitting – 50% duty cycle (typ/max)	1.86/2.49W	2.47/3.24W		1.30/2.13W	*	1.20/1.95W	*
Transmitting – 100% duty cycle (typ/max)	2.48/3.28W	3.43/4.40W		1.75/2.91	*	1.69/2.75W	*
POWER DISSIPATION							
Hottest Die <sup>(5)</sup>	12V Supply	15V Supply		15V Supply	*	12V Supply	*
Non-Transmitting – (typ/max)	0.0W	0.0W		0.45/0.68W	*	0.39/0.59W	*
Transmitting – 50% duty cycle (typ/max)	0.12/0.15W	0.15/0.18W		0.85/1.45W	*	0.81/1.36W	*
Transmitting – 100% duty cycle (typ/max)	0.24/0.29W	0.30/0.36W		1.30/2.23W	*	1.30/2.16W	*
MECHANICAL							
Size	24 Pin Square	*		24 Pin DDIP	*	*	*
Dimensions	1.258" x 1.258" x 0.175"	*		1.400" x 0.805" x 0.200"	*	*	*
Size	24 Pin Square Flatpack	*		24 Pin Flatpack	*	*	*
Dimensions	1.255" x 1.255" x 0.160"	*		1.275" x 0.775" x 0.175"	*	*	*
Weight	0.6 oz	*		0.6 oz	*	*	*

**TABLE 3. BUS-63100 II SPECIFICATIONS - Continued**

BUS-63125 II †† BUS-63126 II †† Dual -15V Harris BUS-25679	BUS-63135 II BUS-63136 II Dual -15V Smiths BUS-25679	BUS-63127 II BUS-63128 II Dual -12V Harris BUS-29854	BUS-63137 II BUS-63138 II Dual -12V Smiths BUS-29854
1'LS * * * * * *	* * * * * *	* * * * * *	* * * * * *
1'LS 1'LS * * 150ns, typ * * * * * *	* * * * * * * * * *	* * * * * * * * * *	* * * * * * * * * *
2'LS *	* *	* *	* *
(Total Hybrid)	(Total Hybrid)	(Total Hybrid)	(Total Hybrid)
+5V±10%    -15V±5%	+5V±10%    -15V±5%	+5V±10%    -12V±5%	+5V±10%    -12V±5%
60/90mA    40/60mA 60/90mA    115/160mA 60/90mA    190/255mA	60/90mA    40/60mA 60/90mA    115/160mA 60/90mA    190/255mA	60/90mA    40/60mA 60/90mA    135/185mA 60/90mA    230/305mA	60/90mA    40/60mA 60/90mA    135/185mA 60/90mA    230/305mA
* * * 7.0°C/W 20°C/W (36 Pin DDIP)	* * * * *	* * * * *	* * * * *
(Total Hybrid, One Channel Transmitting)	(Total Hybrid, One Channel Transmitting)	(Total Hybrid, One Channel Transmitting)	(Total Hybrid, One Channel Transmitting)
0.90/1.35W 1.30/2.13W 1.75/2.91	0.90/1.35W 1.30/2.13W 1.75/2.91W	0.78/1.18W 1.20/1.95W 1.69/2.75W	0.78/1.18W 1.20/1.95W 1.69/2.75W
(Each Channel)	(Each Channel)	(Each Channel)	(Each Channel)
0.45/0.68W 0.85/1.45W 1.30/2.23W	0.45/0.68W 0.85/1.45W 1.30/2.23W	0.39/0.59W 0.81/1.36W 1.30/2.16W	0.39/0.59W 0.81/1.36W 1.30/2.16W
36 Pin DDIP 1.895" x 0.775" x 0.210" 36 Pin Flatpack 1.905" x 0.785" x 0.165" 0.6 oz	* * * * *	* * * * *	* * * * *

Notes:

- (1) On BUS-63102 II, filtering eliminates harmonics above 1 MHz. Differential group delay is ±35ns (10KHz-2MHz).
  - (2) The Threshold Level, as referred to in this specification, is meant to be the maximum peak to peak voltage (measured on the Data Bus) that can be applied to the receivers' input without causing the output to change from the OFF state.
  - (3) On BUS-63102 II and BUS-63104 II, external threshold levels are adjustable from 0V to 2V, with two external 10K potentiometers. Connect one pot between pin 5 and GND and the other between pin 12 and GND.
  - (4) On BUS-63102 II, Output Level (direct coupled) is 30Vpp.
  - (5) On BUS-63102 II and BUS-63104 II, Hottest Die are defined as the driver transistors.
- \* Same as value to the left.  
 † BUS-63105 II available as Military (DESC) drawing 5962-86049-022C.  
 †† BUS-63125 II and BUS-63126 II available as Military (DESC) drawing 5962-87579.

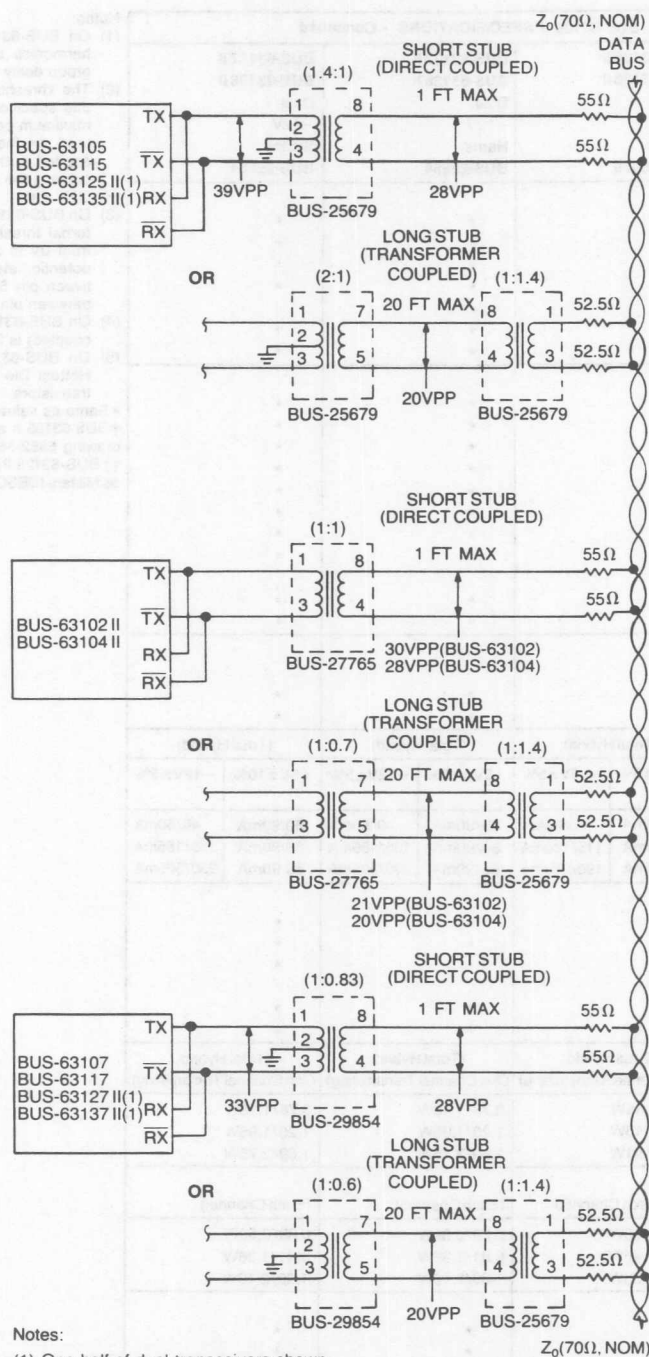


FIGURE 2. BUS COUPLING CONFIGURATIONS

## RECEIVER OPERATING MODE

The receiver section accepts data from a MIL-STD-1553 Data Bus when properly coupled through a transformer in either of the two possible configurations (long or short stub). This data is converted to bi-phase TTL and made available for decoding at the RX Data and RX Data output terminals. Applying a logic "1" to the STROBE input allows data to pass through to the receiver output. Applying a logic "0" to the STROBE input, turns the output OFF.

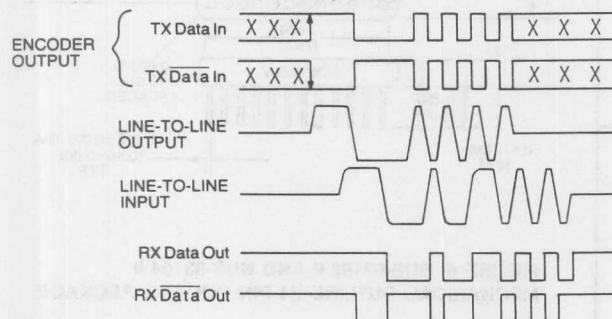
BUS-63102 II, BUS-63104 II, BUS-63115 II, BUS-63135 II, BUS-63117 II, and BUS-63137 II receiver outputs are both at a logic "1" when they are either strobed off, or no signal is being received. This makes these models directly compatible with Smiths type of encoder/decoder. All other models (BUS-63105 II, BUS-63107 II, BUS-63125 II, and BUS-63127 II) receiver outputs are both at

logic "0" when they are either strobed off, or no signal is being received. This makes this type directly compatible with Harris 15530 type of encoder/decoders.

## BUS-63100 SERIES WAVEFORMS

Waveforms for BUS-63100 II series transceivers (BUS-63102 II, BUS-63104 II, BUS-63115 II, BUS-63117 II, BUS-63135 II, and BUS-63137 II) which are directly compatible to Smiths type Encoders/Decoders are illustrated in figure 3. Waveforms for transceivers (BUS-63105 II, BUS-63107 II, BUS-63125 II, and BUS-63127 II) which are directly compatible with Harris type Encoder/Decoders are illustrated in figure 4.

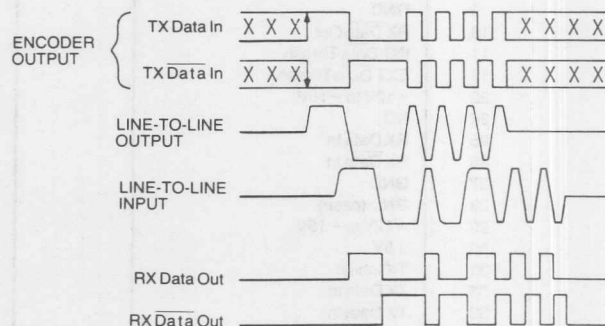
Data and  $\overline{\text{Data}}$  inputs must be complementary waveforms of 50% duty cycle. Care must be taken that the Manchester bi-phase truth table is followed (see timing diagram below).



**FIGURE 3. WAVEFORMS (SMITHS DIRECT COMPATIBILITY)**

## Notes:

- (1) TX Data In and RX Data Out are TTL signals.
- (2) TX Data In inputs must be at opposite logic levels during transmission, and at the same logic level when not transmitting.
- (3) LINE-TO-LINE output voltage is measured between TX Data Out and TX Data Out.
- (4) LINE-TO-LINE output voltage for BUS-63102 II are sinusoidal waveforms for 1 MHz operating frequency.
- (5) LINE-TO-LINE input voltage is measured on the Data Bus.



**FIGURE 4. WAVEFORMS (HARRIS DIRECT COMPATIBILITY)**

Notes:

- (1) TX Data In and RX Data Out are TTL signals.
- (2) TX Data In inputs must be at opposite logic levels during transmission, and at the same logic level when not transmitting.
- (3) LINE-TO-LINE output voltage is measured between TX Data Out and TX Data Out.
- (4) LINE-TO-LINE input voltage is measured on the Data Bus.



# 24 PIN SQUARE AND 24 PIN SQUARE FLATPACK TRANSCEIVERS

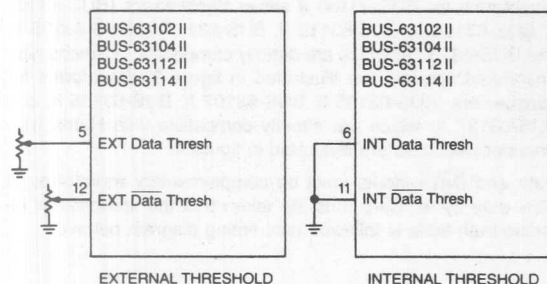


FIGURE 5. THRESHOLD CONNECTIONS

<b>TABLE 4</b> <b>BUS-63102 II, BUS-63104 II</b> <b>(24 PIN SQUARE)</b> <b>AND</b> <b>BUS-63112 II, BUS-63114 II</b> <b>(24 PIN SQUARE FLATPACK)</b> <b>PIN CONNECTIONS</b>	
PIN	FUNCTION
1	TX Data Out
2	TX Data Out
3	GND
4	+12V to +15V
5	EXT Data Thresh
6	INT Data Thresh
7	RX Data Out
8	Strobe
9	GND
10	RX Data Out
11	INT Data Thresh
12	EXT Data Thresh
23	+12V to +15V
24	NC
25	RX Data In
26	RX Data In
27	GND
28	GND (case)
29	-12V to -15V
30	+5V
31	TX Inhibit
32	TX Data In
33	TX Data In
34	-12V to -15V

Note:  
For internal threshold levels, ground pins 6 and 11.  
For external threshold, connect two 10K Ohm pots  
(one between pin 5 and GND, and one between pin  
12 and GND). (See figure 5.)

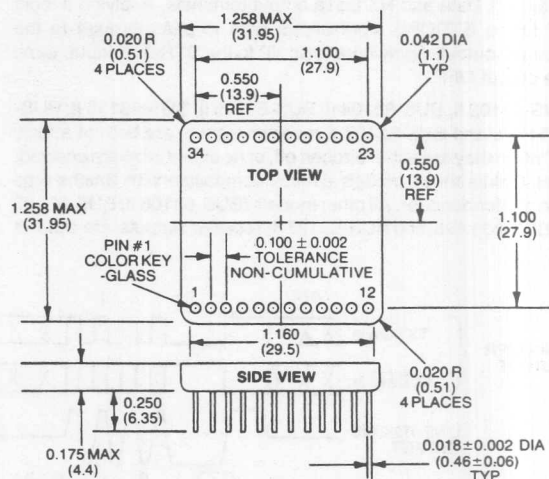


FIGURE 6. BUS-63102 II AND BUS-63104 II  
MECHANICAL OUTLINE-24 PIN SQUARE PACKAGE

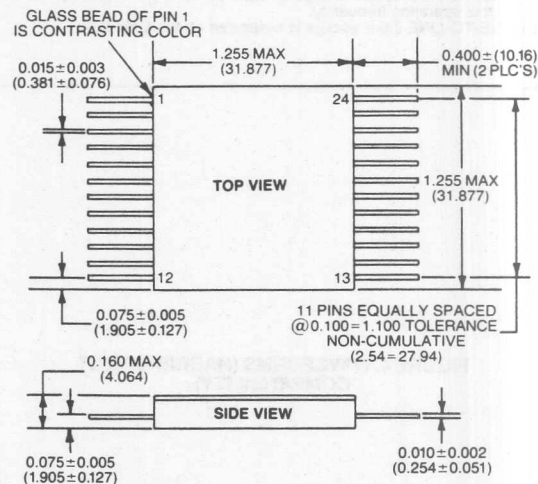
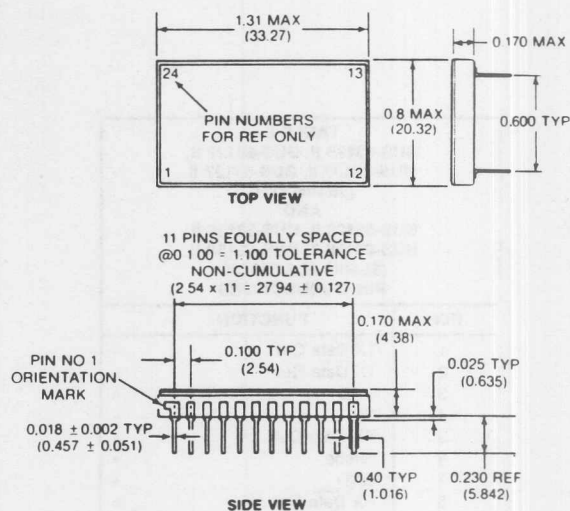


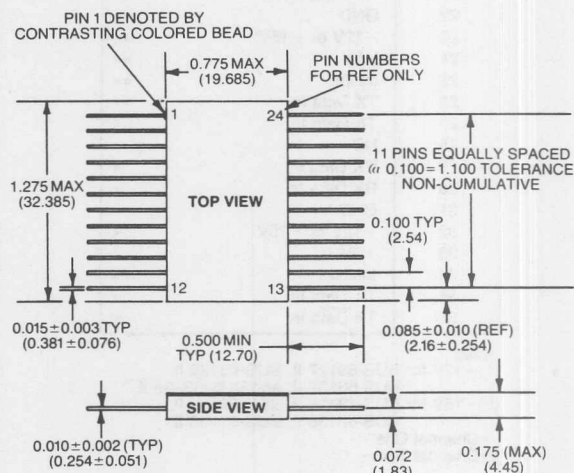
FIGURE 7. BUS-63112 II AND BUS-63114 II  
MECHANICAL OUTLINE-24 PIN SQUARE FLATPACK

## 24 PIN DDIP AND 24 PIN FLATPACK TRANSCEIVERS

<b>TABLE 5</b> <b>BUS-63105 II, BUS-63107II</b> <b>BUS-63115 II, BUS65117II</b> <b>(24 PIN DDIP)</b> <b>AND</b> <b>BUS-63106 II, BUS63108 II</b> <b>BUS-63116 II, BUS-63118 II</b> <b>(24 PIN FLATPACK)</b> <b>PIN CONNECTIONS</b>	
PIN	FUNCTION
1	TX Data Out
2	TX Data Out
3	GND
4	NC
5	NC
6	NC
7	RX Data Out
8	Strobe
9	GND
10	RX Data Out
11	NC
12	NC
13	NC
14	NC
15	RX Data In
16	RX Data In
17	NC
18	GND
19	-12V or -15V
20	+5V
21	TX Inhibit
22	TX Data In
23	TX Data In
24	NC



**FIGURE 8. BUS-63105II, BUS-63107II, BUS-63115II, AND BUS-63117II MECHANICAL OUTLINE-24PIN DDIP**



**FIGURE 9. BUS-63106II, BUS-63108II, BUS-63116II, AND BUS-63118II MECHANICAL OUTLINE-24PIN FLATPACK**

## 36 PIN DDIP AND 36 PIN FLATPACK TRANSCEIVERS

PIN	FUNCTION	
1	TX Data Out	*
2	TX Data Out	*
3	GND	*
4	NC	*
5	RX Data Out	*
6	Strobe	*
7	GND	*
8	RX Data Out	*
9	GND (case)	*
10	TX Data Out	**
11	TX Data Out	**
12	GND	**
13	NC	**
14	RX Data Out	**
15	Strobe	**
16	GND	**
17	RX Data Out	**
18	NC	
19	NC	
20	RX Data In	**
21	RX Data In	**
22	GND	**
23	-12V or -15V	**
24	+5V	**
25	Inhibit	**
26	TX Data In	**
27	TX Data In	**
28	NC	
29	RX Data In	*
30	RX Data In	*
31	GND	*
32	-12V or -15V	*
33	+5V	*
34	Inhibit	*
35	TX Data In	*
36	TX Data In	*

Notes:

(1) -12V for BUS-63127 II, BUS-63128 II,  
BUS-63137 II, and BUS-63138 II.  
(2) -15V for BUS-63125 II, BUS-63126 II,  
BUS-63135 II, BUS-63136 II.

\*Channel One

\*\*Channel Two

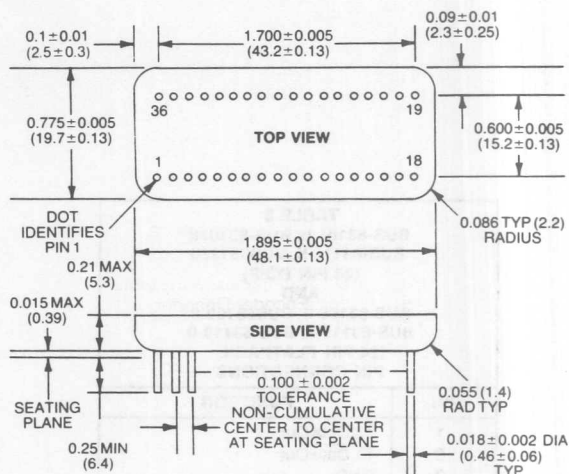


FIGURE 10. BUS-63125 II, BUS-63127 II, BUS-63135 II, AND BUS-63137 II MECHANICAL OUTLINE-36 PIN DDIP

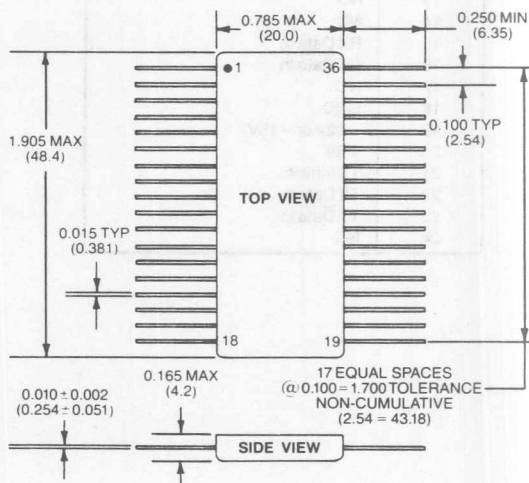


FIGURE 11. BUS-63126 II, BUS-63128 II, BUS-63136 II, AND BUS-63138 II MECHANICAL OUTLINE-36 PIN FLATPACK

## ORDERING INFORMATION

### SINGLE TRANSCEIVERS

#### BUS-63105 II-883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL-STD-883 but without QCI testing
  - Blank = 0<sup>u</sup> to 70°C
- Power Supply Voltage Range/Package
  - 5 = -15VDC/DDIP
  - 6 = -15VDC/Flatpack
  - 7 = -12VDC/DDIP
  - 8 = -12VDC/Flatpack
- Enc-Dec Compatibility:
  - 0 = Compatible with Harris Encoder/Decoder
  - 1 = Compatible with Smiths Encoder/Decoder

BUS-63105 II available as Military (DESC) drawing 5962-86049-02ZC.

See figure 2 for mating transformer.

#### BUS-63102 II-883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL-STD-883 but without QCI testing
  - Blank = 0<sup>u</sup> to 70°C
- 2 = Universal transceiver (MACAIR and 1553)  $\pm 12V$  to  $\pm 15V$  power supply range, compatible with Smiths Encoder/Decoder.
- 4 = 1553,  $\pm 12V$  to  $\pm 15V$  power supply range, compatible with Smiths Encoder/Decoder.
- Packaging:
  - 0 = 24 pin square
  - 1 = 24 pin square flatpack

See figure 2 for mating transformer.

### DUAL TRANSCEIVERS

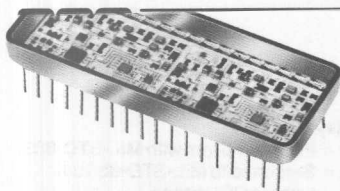
#### BUS-63125 II-883B

- Reliability Grade: (See note.)
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL-STD-883 but without QCI testing
  - Blank = 0<sup>u</sup> to 70°C
- Power Supply Voltage Range/Package
  - 5 = -15VDC/DDIP
  - 6 = -15VDC/Flatpack
  - 7 = -12VDC/DDIP
  - 8 = -12VDC/Flatpack
- Enc-Dec Compatibility:
  - 2 = Compatible with Harris Encoder/Decoder
  - 3 = Compatible with Smiths Encoder/Decoder

BUS-63125 II and BUS-63126 II available as Military (DESC) drawing 5962-87579.

See figure 2 for mating transformer.

Note: Available as BUS-63125 II-641 (BUS-65612 compatible Transceiver).



## +5V DUAL TRANSCEIVER

### FEATURES

- ONLY REQUIRES +5V POWER SUPPLY
- SMALL SIZE – 36 PIN DDIP
- LOW POWER
- MIL-STD-883B SCREENING AVAILABLE
- DUAL REDUNDANT PACKAGING
- HARRIS I/O COMPATIBILITY
- CONFORMS FULLY TO MIL-STD-1553A AND 1553B

### DESCRIPTION

The BUS-63147 transceiver is a complete transmitter and receiver pair conforming fully to MIL-STD-1553A and 1553B. Features include: +5V power supply voltage, Harris interface type, completely independent dual redundant operation, and small size (36 pin DDIP).

The receiver section of the BUS-63147 series accepts phase-modulated bipolar data from a MIL-STD-1553 Data Bus and produces TTL signal data at its outputs: RX DATA OUT and RX DATA OUT. These outputs represent positive and negative variations of the input data signals beyond an internally fixed threshold level. An external STROBE input enables or disables the receiver's outputs.

The transmitter section accepts bi-phase TTL signal data at its TX DATA and TX DATA inputs and produces phase-modulated bipolar data at the TX DATA and TX DATA outputs. The transmitter's output voltage level is typically 30Vpp. An external input, INHIBIT, takes priority over the transmitter inputs and disables the transmitter when activated with a logic "1".

The small size, +5V power supply voltage, and compliance with MIL-STD-1553 simplify engineering design, making it an excellent choice for interfacing with any MIL-STD-1553 system.

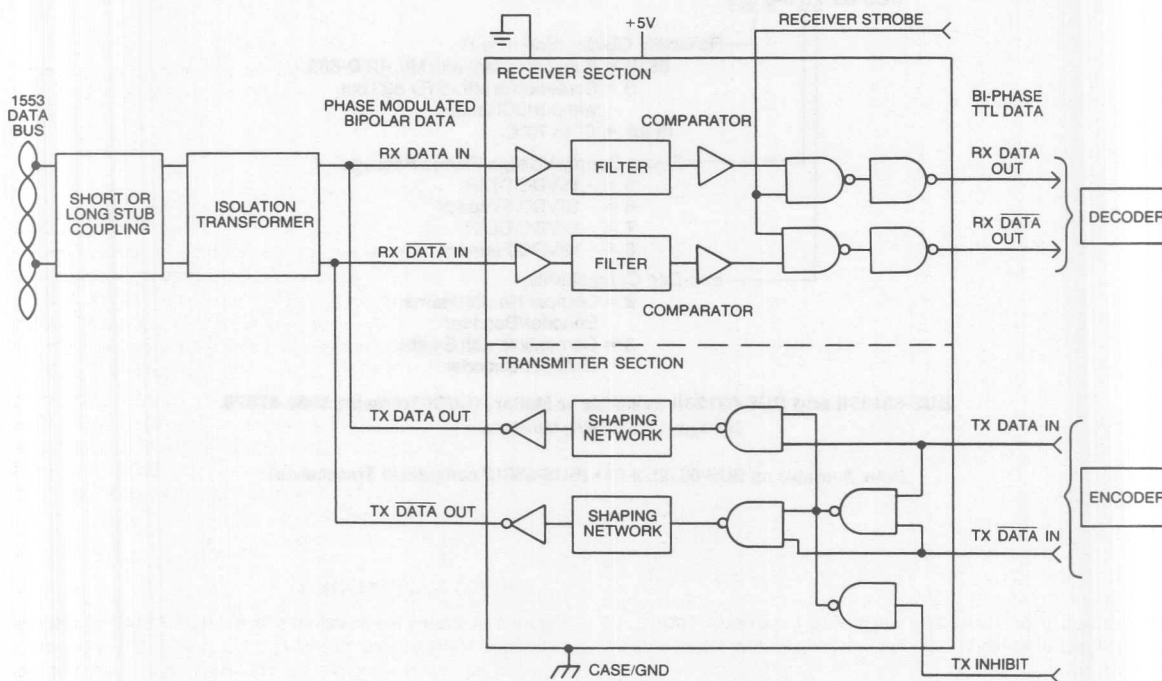


FIGURE 1. BUS-63147 BLOCK DIAGRAM



**TABLE 1. BUS-63147 SPECIFICATIONS**

<b>RECEIVER</b>	
Strobe	2 LS Loads
Input Level	40Vpp, Diff, max
Threshold Level*	0.56Vpp min, 1.0Vpp max
CMRR	40 db, min
Input Resistance – Diff	2K $\Omega$ , min
Input Capacitance – Diff	5pf, max
Output Fan Out	10 LS Loads
<b>TRANSMITTER</b>	
TX DATA Input	2 TTL Loads
TX DATA Input	2 TTL Loads
TX Inhibit	1 TTL Load
Output Level (Direct Coupled)	30Vpp, nom across 140 $\Omega$ load
Rise/Fall Time (nsec)	100 min, 150 typ, 300 max
Output Noise	10mVpp, Diff, max
Output Offset Voltage	$\pm$ 90mVpp, max across 35 $\Omega$ load
Output Impedance (Non-Transmitting)	
Output Resistance – Diff	10K $\Omega$ , min
Output Capacitance – Diff	5pf, max
<b>POWER SUPPLY REQUIREMENTS</b>	
	Each channel +5V – 5% + 10%
Non-Transmitting – (typ/max)	29/49mA
Transmitting – 50% duty cycle (typ/max)	164/199.5mA
Transmitting – 100% duty cycle (typ/max)	299.5/349.5mA

**TABLE 1. BUS-63147 SPECIFICATIONS (Continued)**

<b>THERMAL</b>	
Operating Junction Temperature	–55°C to +160°C
Operating Case Temperature	–55°C to +125°C
Storage Temperature	–55°C to +160°C
Thermal Impedance – Junction to Case Case to Air (typ)	110°C/W (Hottest Die) 20°C/W
<b>POWER DISSIPATION</b>	
Single Channel	(Total Hybrid, one channel transmitting, other at idle)
Non-Transmitting – (typ/max)	0.29/0.49W
Transmitting – 50% duty cycle (typ/max)	1.25/1.80W
Transmitting – 100% duty cycle (typ/max)	2.49/3.10W
<b>POWER DISSIPATION</b>	
Hottest Die	(Each Channel)
Non-Transmitting – (typ/max)	0.0W
Transmitting – 50% duty cycle (typ/max)	0.13/0.16W
Transmitting – 100% duty cycle (typ/max)	0.27/0.32W
<b>MECHANICAL</b>	
Size	36 Pin DDIP
Dimensions	1.895" x 0.775" x 0.210"
Weight	.6 oz
* The Threshold Level, as referred to in this specification, is meant to be the maximum peak to peak voltage (measured on the Data Bus) that can be applied to the receivers' input without causing the output to change from the OFF state.	

## GENERAL

The BUS-63147 is a dual redundant transmitter and receiver packaged in a 36 pin DDIP. It is directly compatible to Harris 15530 encoder/decoder and has internal (factory preset) threshold levels. Requiring only a +5V power supply, the BUS-63147 is designed for use in any MIL-STD-1553 application.

Figure 2 illustrates the BUS-63147 connected to a MIL-STD-1553 Data Bus. Once transformer isolated, coupling to Data Bus can be either short stub (direct) or long stub (transformer). The recommended transformer for long stub and short stub coupling is DDC's BUS-41429.

## TRANSMIT OPERATING MODE

The transmitter section accepts encoded TTL data and converts it to phase-modulated bipolar form by means of a waveshaping network and driver circuitry. These driver outputs are coupled to a MIL-STD-1553 Data Bus via a transformer which is driven from the TX DATA OUT and TX  $\overline{\text{DATA}}$  OUT terminals. These output terminals can be put into a high impedance state when transmitting by enabling INHIBIT, or by placing both inputs at the same logic level following the Manchester II truth table. Table 2, Transmit Operating Mode, lists the functions for the output data and input data in reference to the state of INHIBIT. The transceivers are able to operate in a "wraparound" mode. This allows output data to be monitored by the receiver section

and returned to the decoder where it can be checked for errors. Reference DDC Protocol Monolithics (BUS-65600 or BUS-65112) for more information.

## RECEIVER OPERATING MODE

The receiver section accepts data from a MIL-STD-1553 Data Bus when properly coupled in either of the two possible configurations (long or short stub). This data is converted to bi-phase TTL and made available for decoding at the RX DATA and RX  $\overline{\text{DATA}}$  output terminals. Applying a logic "1" to the STROBE input allows data to pass through to the receiver output. Applying a logic "0" to the STROBE input, turns the receiver output OFF.

The BUS-63147 receiver outputs are both at a logic "0" when they are either strobed off, or no signal is being received. This is directly compatible with Harris type of encoder/decoder. Compatibility to Smiths type of encoder/decoder can be accomplished by swapping the RX DATA and RX  $\overline{\text{DATA}}$  outputs and then inverting them (see figure 3).

## BUS-63147 WAVEFORMS

Figure 4 illustrates the waveforms for the BUS-63147 with Harris type encoder/decoders. Note that DATA and  $\overline{\text{DATA}}$  inputs must be complementary waveforms of 50% duty cycle. Care must be taken that the Manchester bi-phase truth table is followed if other encoder/decoders are used.

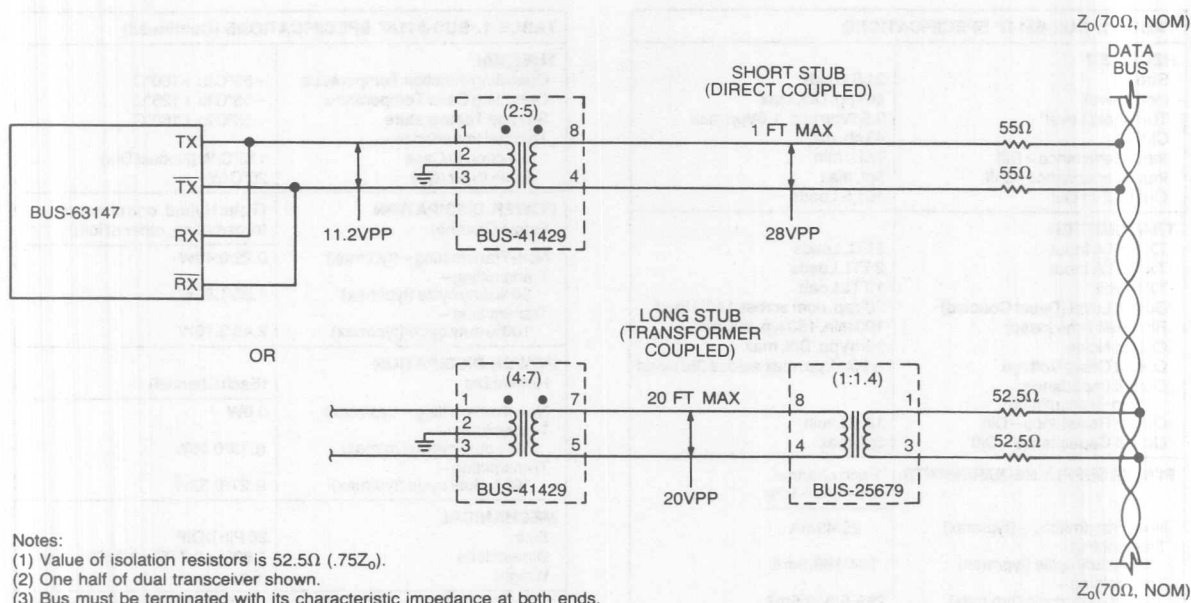


FIGURE 2. BUS-63147 CONNECTIONS TO DATA BUS

TABLE 2. TRANSMIT OPERATING MODE			
TX DATA IN	TX DATA IN	TX INHIBIT	DRIVER OUTPUT <sup>(2)</sup>
X <sup>(1)</sup>	X	H	OFF <sup>(3)</sup>
0	0	X	OFF
0	1	L	ON
1	0	L	ON
1	1	X	OFF

Notes:

- (1) X = Don't care.
- (2) DRIVER OUT = TX DATA OUT and TX DATA OUT
- (3) DRIVER OUTPUT terminals are in the high impedance mode during OFF time, independent of INHIBIT status.

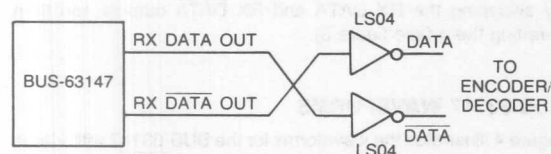
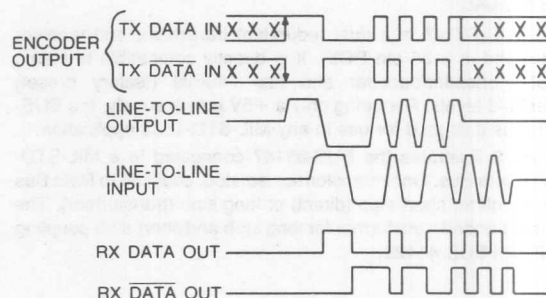


FIGURE 3. SMITHS ENCODER/DECODER COMPATIBILITY



Notes:

- (1) TX DATA IN and RX DATA OUT are TTL signals.
- (2) TX DATA IN inputs must be at opposite logic levels during transmission, and at the same logic level when not transmitting.
- (3) LINE-TO-LINE output voltage is measured between TX DATA OUT AND TX DATA OUT.
- (4) LINE-TO-LINE input voltage is measured on the Data Bus.

FIGURE 4. BUS-63147 WAVEFORMS

**TABLE 3. BUS-63147 PIN FUNCTIONS**

PIN	FUNCTION	PIN	FUNCTION
1	TX DATA OUT	* 19	NC
2	TX DATA OUT	* 20	RX DATA IN **
3	GND	* 21	RX DATA IN **
4	NC	* 22	GND **
5	RX DATA OUT	* 23	NC **
6	STROBE	* 24	+5V **
7	GND	* 25	INHIBIT **
8	RX DATA OUT	* 26	TX DATA IN **
9	GND (CASE)	* 27	TX DATA IN **
10	TX DATA OUT	** 28	NC
11	TX DATA OUT	** 29	RX DATA IN *
12	GND	** 30	RX DATA IN *
13	NC	** 31	GND *
14	RX DATA OUT	** 32	NC *
15	STROBE	** 33	+5V *
16	GND	** 34	INHIBIT *
17	RX DATA OUT	** 35	TX DATA IN *
18	NC	** 36	TX DATA IN *

\*Channel One

\*\*Channel Two

## ORDERING INFORMATION

BUS- 63147 - 883B

Reliability Grade:

883B = Fully compliant with  
MIL-STD-883

B = Screened to MIL-STD-883  
but without QCI testing

Blank = 0° to 70° C operation

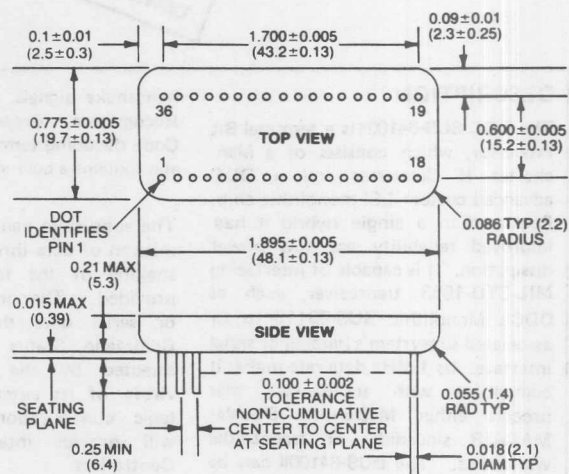
Decoder Compatibility:

7 = Standard Decoder

8 = DDC Bus-65612 PGA

Matching transformer BUS-41429.

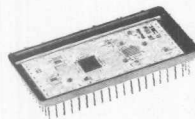
SMD Listing: DESC# 5962-89522-01XC



Dimensions in inches (millimeters).

**FIGURE 5. BUS-63147 MECHANICAL OUTLINE**

# MIL-STD-1553 TERMINAL BIT PROCESSOR



**IMPROVED  
CONTACT FACTORY**

## FEATURES

- 16 BIT OR 8 BIT BYTE PARALLEL OR SERIAL I/O
- PERFORMS MIL-STD-1553 FUNCTIONS:  
BROADCAST  
MODE CODE  
OWN ADDRESS  
TIME OUT
- ON/OFF LINE SELF-TEST
- DUAL RANK REGISTERS
- LOW POWER LSI DESIGN

## DESCRIPTION

The DDC BUS-64100II is a terminal Bit Processor, which consists of a Manchester II Converter and a DDC advanced custom LSI monolithic chip. Packaged in a single hybrid it has improved reliability and low power dissipation. It is capable of interfacing MIL-STD-1553 transceiver, such as DDC's Monolithic BUS-63115 to an associated subsystem's parallel or serial interface. Its 1 MHz data rate makes it compatible with transceivers that process either McDonnell Douglas MACAIR sinusoidal or trapezoidal waveforms. The BUS-64100II can be used as a common interface for remote terminals, bus monitors or bus controllers.

This unit functions as a decoder per MIL-STD-1553 by transferring all command, status and data words to the subsystem, together with error information, BIT status and necessary

handshake signals. It flags Address Recognition, Broadcast and Mode Code decoding terminal fail safe signal and contains a built-in Self-test Circuit.

The subsystem can control the transmission of data through positive handshaking of the logic control lines provided. The unit accepts parallel or serial data then transmits the Command, Status or Data words as directed by the subsystem. By virtue of its extensive input/output logic configuration the BUS-64100II will provide interfacing for BUS Controllers.

The BUS-64100II meets the full specifications of MIL-STD-1553 A & B and those of MACAIR A5690, A3818, A4905 and A5232. The hybrid operates over the temperature range of -55°C to +125°C. Military Processing is available (Contact Factory).

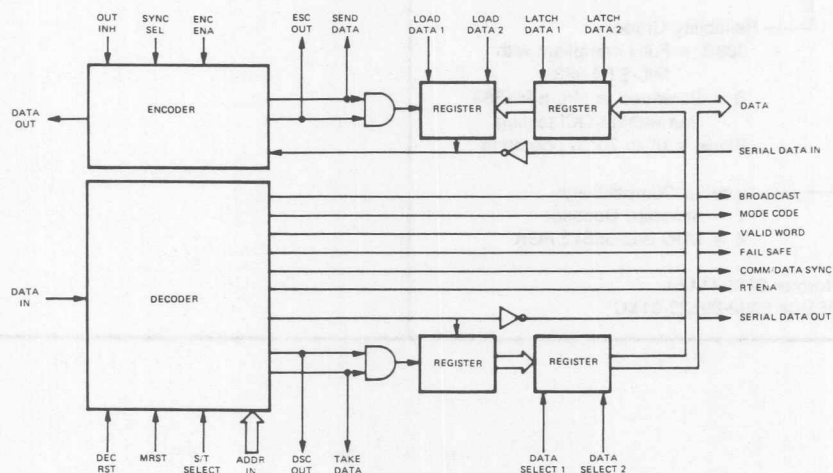
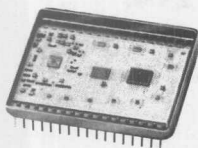


FIGURE 1. BUS-64100II BLOCK DIAGRAM

## MIL-STD-1553 DUMB RTU HYBRID



### DESCRIPTION

The BUS-65101II MIL-STD-1553 Dumb Remote Terminal Unit (RTU) consists of a transceiver, and encoder/decoder, control logic, dual rank I/O registers and internal clock oscillator packaged in a 1.6" x 1.9" hermetic hybrid. It provides all the functions required to interface between a MIL-STD-1553 serial MUX data bus and a subsystem parallel 3-state data highway. Utilizing several DDC custom monolithic ICs, the BUS-65101II provides sufficient handshaking, control and data lines to permit versatile operation as a remote terminal, a bus controller or a bus monitor, in either single or dual redundant data bus configurations.

As a transmitter, the BUS-65101II accepts 8 bit or 16 bit parallel data from the subsystem, and outputs serial Manchester II coded Command, Status or Data words, under subsys-

tem control. As a receiver, it accepts serial MIL-STD-1553 transmissions and transfers all Command, Status and Data words to the 8 bit or 16 bit data highway, under subsystem control. The BUS-65101II also provides flags to the subsystem when Broadcast, Mode Code, and Own Address (with parity) commands are decoded.

The BUS-65101II contains a terminal fail-safe timeout circuit which flags message lengths exceeding 768 microseconds, and terminates serial data transmission. Wraparound self-test is initiated by a control line which causes the encoder serial output to be connected to the decoder input. The BUS-65101II provides a serial output of decoded words, thus allowing Command Word lookahead, for the fastest terminal response.

### FEATURES

- **INCLUDES:**
  - TRANSCIVER
  - ENCODER/DECODER
  - DUAL RANK I/O REGISTERS
  - FAIL-SAFE TIMER
  - CLOCK OSCILLATOR
- **SMALL 1.6" x 1.9" HYBRID**
- **PROVIDES FLAGS FOR:**
  - OWN ADDRESS (WITH PARITY)
  - MODE CODE
  - BROADCAST
  - TIME OUT
  - VALID WORD
  - SYNC TYPE
- **16 BIT OR 8 BIT 3-STATE PARALLEL I/O AND SERIAL OUT**
- **WRAPAROUND BUILT-IN TEST**
- **SIMPLE CONTROLS FOR SINGLE OR DUAL REDUNDANT DATA BUS CONFIGURATIONS**

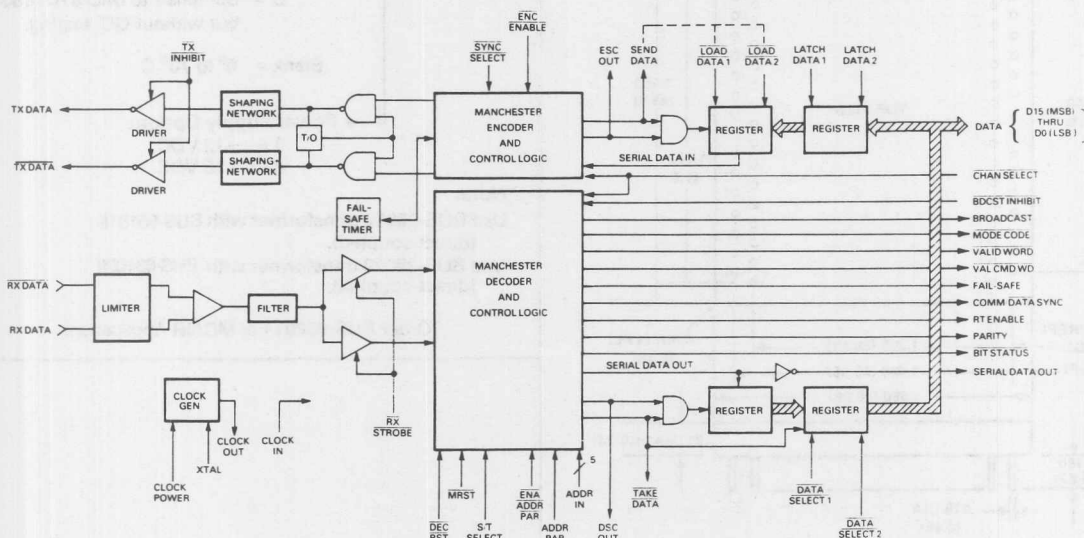


FIGURE 1. BUS-65101II BLOCK DIAGRAM



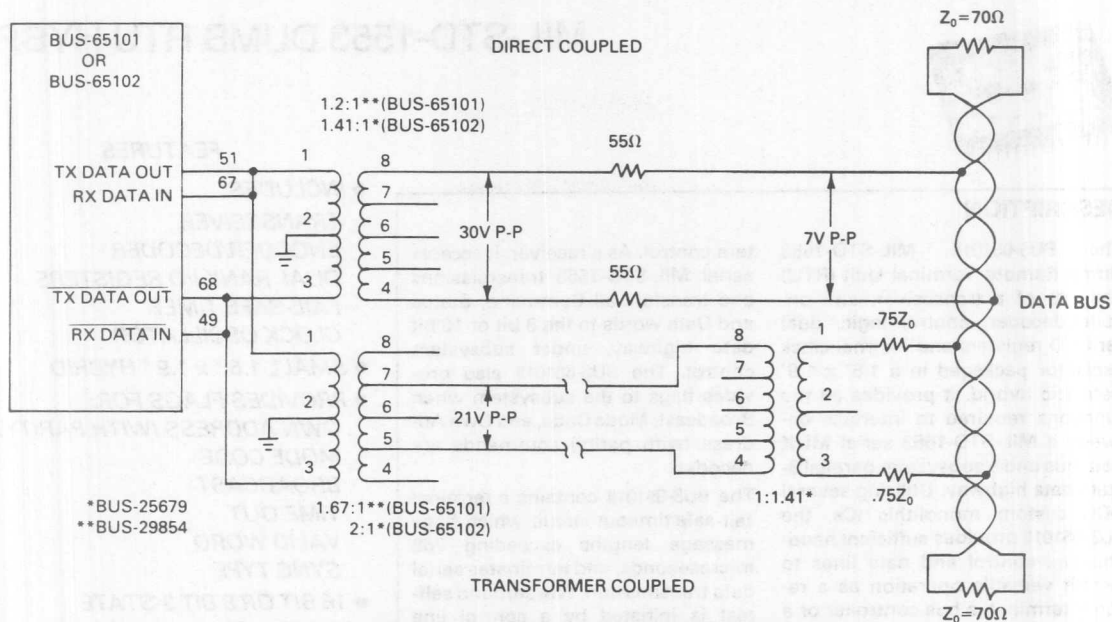
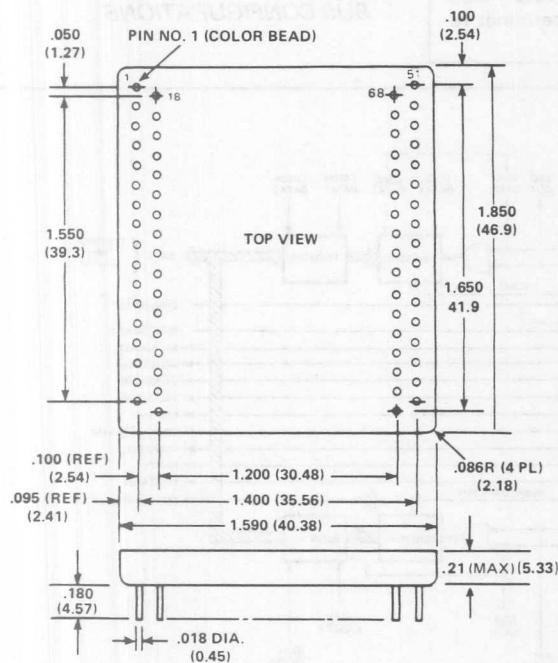


FIGURE 6. TYPICAL TRANSFORMER CONNECTIONS

## MECHANICAL OUTLINE



## ORDERING INFORMATION

BUS-65101II-883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883.

B = Screened to MIL-STD-883 but without QCI testing.

Blank = 0° to 70° C

Power Supply Option:

1 = -12 VDC  
2 = -15 VDC

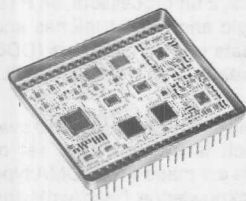
Note:

Use BUS-29854 transformer with BUS-65101II (direct-coupled).

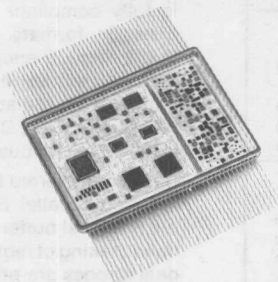
Use BUS-25679 transformer with BUS-65102II (direct-coupled).

Order BUS-65201 For MCAIR Applications.

## MIL-STD-1553 DUAL REDUNDANT REMOTE TERMINAL HYBRID



BUS-65112 DDIP



BUS-65117 FLATPACK

### DESCRIPTION

The BUS-65112 is a complete dual redundant MIL-STD-1553 Remote Terminal Unit (RTU) packaged in a small 1.9" x 2.1" hybrid. Based upon DDC custom ICs, it includes 2 transceivers, 2 encoder/decoders, 2 bit processors, RTU protocol, data buffers, and timing control logic. It supports all 13 mode codes for dual redundant operation, any combination of which can be illegalized.

Parallel data transfers are accomplished with a DMA type handshaking, compatible with most CPU types. Data transfers to/from memory are simplified by the latched command word and word count out-

puts. Error detection and recovery are enhanced by BUS-65112 special features. A 14 bit built-in-test word register stores RTU information, and sends it to the Bus Controller in response to the Mode Command Transmit Bit Word. The BUS-65112 performs continuous on-line wrap-around self-test, and provides 4 error flags to the host CPU. Inputs are provided for host CPU control of 6 bits of the RTU Status Word.

Its small hermetic package, -55°C to +125°C operating temperature range, and complete RTU operation make the BUS-65112 ideal for most MIL-STD-1553 applications.

### FEATURES

- SMALL SIZE & LOW POWER
- COMPLETE RTU PROTOCOL
- SUPPORTS 13 MODE CODES: ANY COMBINATIONS CAN BE ILLEGALIZED
- TRANSFERS DATA WITH DMA TYPE HANDSHAKING
- LATCHED OUTPUTS FOR COMMAND WORD AND WORD COUNT
- 14 BIT BUILT-IN-TEST WORD REGISTER
- 4 ERROR FLAG OUTPUTS
- CONTINUOUS ONLINE SELF-TEST
- PLUG-IN & FLATPACK PACKAGING

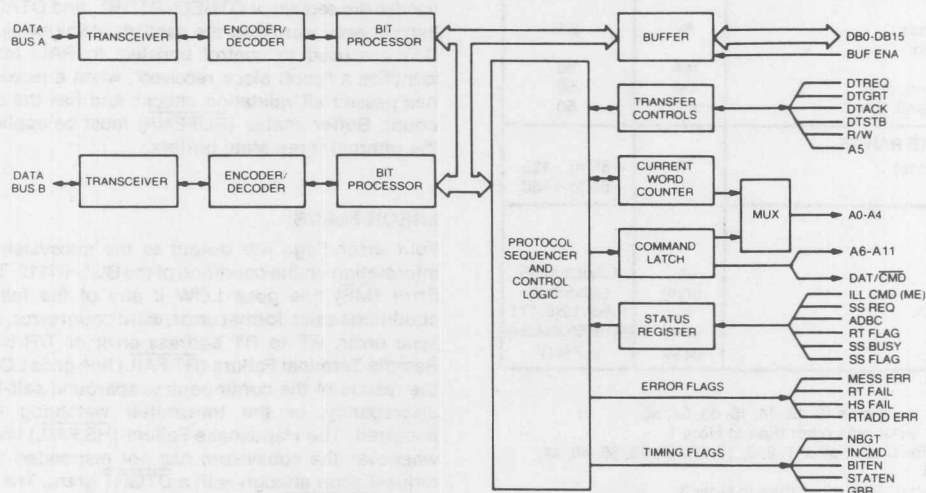


FIGURE 1. BUS-65112 BLOCK DIAGRAM

PARAMETER	UNITS	VALUE
<b>RECEIVER</b>		
Differential Input Impedance (DC to 1MHz)	K $\Omega$	4 min
Differential Input Voltage	V <sub>p-p</sub>	40 max
Input Threshold (Direct Coupled)	V <sub>p-p</sub>	1 typ
CMRR (DC to 2MHz)	dB	40 min
CMV (DC to 2MHz)	V	$\pm 10$ min
<b>TRANSMITTER</b>		
Differential Output Voltage	V <sub>p-p</sub>	30 typ
Direct Coupled (Across 145 $\Omega$ Load)	V <sub>p-p</sub>	21 typ
Transformer Coupled (at Stub)	V <sub>p-p</sub>	130 typ
Output Rise and Fall Times	ns	10 max
Output Noise	mV <sub>p-p</sub>	10 max
<b>LOGIC</b>		
V <sub>IH</sub>	V	2.4 min
V <sub>IL</sub>	V	0.7 max
I <sub>IH</sub> (Note 1) (V <sub>IH</sub> = 2.7V)	mA	-0.7 max
I <sub>IH</sub> (Note 2) (V <sub>IH</sub> $\geq$ 2.4V)	$\mu$ A	$\pm 20$ max
I <sub>IL</sub> (Note 1) (V <sub>IL</sub> = 0.4V)	mA	-1.6 max
I <sub>IL</sub> (Note 2) (V <sub>IL</sub> $\leq$ 0.7V)	$\mu$ A	$\pm 20$ max
V <sub>OH</sub> (Note 3) (I <sub>OH</sub> = 0.3 mA)	V	2.4 min
V <sub>OH</sub> (Note 4) (I <sub>OH</sub> = 3 mA)	V	2.4 min
V <sub>OH</sub> (Note 6) (I <sub>OH</sub> = -3 mA)	V	2.4 min
V <sub>OL</sub> (Note 3) (I <sub>OL</sub> = -1.6 mA)	V	0.4 max
V <sub>OL</sub> (Note 5) (I <sub>OL</sub> = -4 mA)	V	0.4 max
V <sub>OL</sub> (Note 6) (I <sub>OL</sub> = -6 mA)	V	0.4 max
C <sub>i</sub> (f = 1 MHz)	pF	50 typ
C <sub>io</sub> (Note 6) (f = 1 MHz)	pF	50 typ
<b>POWER SUPPLIES</b>		
+5VDC		
Tolerance, max	%	$\pm 10$
Current Drain, max	mA	160
+15VDC		
Tolerance, max	%	$\pm 5$
Current Drain, max		
Idle, max	mA	80
50% Transmit, max	mA	180
100% Transmit, max	mA	280
-15VDC		
Tolerance, max	%	$\pm 5$
Current Drain		
Idle, max	mA	60
50% Transmit, max	mA	60
100% Transmit, max	mA	60
<b>TEMPERATURE RANGE</b>		
Operating (Case)	$^{\circ}$ C	-55 to +125
Storage	$^{\circ}$ C	-65 to +150
<b>PHYSICAL</b>		
Size		
DDIP	in. (mm)	1.9x2.1x0.25 (48x53x6)
Flatpack	in. (mm)	1.6x2.19x0.171 (40.6x55.6x4.34)
Weight	oz (g)	1.7 (41)

**Notes:**

1. I<sub>IH</sub> and I<sub>IL</sub> for input pins 12, 13, 14, 15, 53, 54, 55.
2. I<sub>IH</sub> and I<sub>IL</sub> for input pins other than in Note 1.
3. V<sub>OH</sub> and V<sub>OL</sub> for output pins, 1, 2, 3, 16, 25, 27, 28, 35, 40, 41, 42, 65, 73, 78.
4. V<sub>OH</sub> for all output pins other than in Note 3.
5. V<sub>OL</sub> for output pins 21, 22, 24, 26, 29, 60, 61, 62, 63, 64.
6. V<sub>OL</sub> and C<sub>io</sub> for pins 43 thru 50 and 4 thru 11.

The BUS-65112 is a complete dual redundant Remote Terminal Unit (RTU) packaged in a small 1.9" x 2.1" hybrid. It is fully compliant with MIL-STD-1553B and supports all message formats. As shown in Figure 1, it includes 2 transceivers, 2 encoder/decoders, 2 bit processors, an RTU protocol sequencer, control logic and output latches and buffers. With the addition of 2 data bus transformers (DDC P/N BUS-25679), BUS-65112 is ready to connect to the MIL-STD-1553 data bus.

Data is transferred to and from the subsystem host CPU over a 16 bit parallel highway, which is isolated by a set of bidirectional buffers. All transfers are made with a DMA type handshaking of request, grant, acknowledge. Read/write and data strobes are provided to simplify interfacing to external RAM memory. Also simplifying the RAM interface, is the availability of latched command word and word counter. These signals may be used as an address to map the data directly to and from RAM.

BUS-65112 allows the subsystem host CPU to control 6 of the bits in the RTU status word. Of particular interest is the Illegal Command input which may be used to set the message error bit and illegalize any command word. Four error flags are provided to the subsystem host CPU by the BUS-65112, to aid in assessing its condition. In addition, a continuous online self-test is performed by the BUS-65112 on every transmission. Each transmitted message is wrapped around to the decoder and compared to the intended message. Any discrepancy is flagged as an error.

## TIMING

The subsystem host CPU interface to the BUS-65112 is simple and compatible with most microprocessors. Figures 3 and 4 illustrate typical MIL-STD-1553 messages of transmit data and receive data, and figures 5 and 6 show RT to RT transfers. In each case, NBGT identifies the start of the message, and INCMD identifies that a command is being processed. The handshake sequence DTREQ, DTGRT, and DTACK is used to transfer each word over the parallel data highway. DTSTR and R/W are used to control transfers to RAM memory. GBR identifies a "good block received", when a received message has passed all validation checks and has the correct word count. Buffer enable (BUFENA) must be applied to enable the internal three-state buffers.

## ERROR FLAGS

Four error flags are output to the subsystem to provide information on the condition of the BUS-65112. The Message Error (ME) line goes LOW if any of the following error conditions exist: format error, word count error, invalid word, sync error, RT to RT address error or T/R bit error. The Remote Terminal Failure (RT FAIL) line goes LOW whenever the results of the continuous wraparound self-test shows a discrepancy, or the transmitter watchdog timeout has occurred. The Handshake Failure (HS FAIL) line goes LOW whenever the subsystem has not responded to a DTREQ request soon enough with a DTGRT grant. The RT Address Error (RTAD ERR) line goes LOW whenever the sum of the 5 address lines and parity line shows a parity error.

## STATUS REGISTER

Six inputs to the BUS-65112 allow the subsystem host CPU to control bits in the RTU Status Word. The Illegal Command input may be used to set the Message Error bit in the Status Word. This line is particularly useful in illegalizing any combination of mode commands. An external PROM may be used to monitor the latched Command Word. This PROM would drive the Illegal Command input LOW when it identifies a mode command that is programmed to be illegal.

The Subsystem Request (SRQ) line is used to set the service request bit in the Status Word. The Accept Dynamic Bus Control (ADBC) line is used to set the Bus Control acceptance bit in the Status Word, if that mode command was sent. The Remote Terminal Flag (RTFLAG) line is used to set the terminal flag bit in the Status Word. The Subsystem Busy

(BUSY) line is used to set the busy bit in the Status Word, and to inhibit requests for data from the subsystem. The Subsystem Flag (SS FLAG) line is used to set subsystem flag (fault) bit in the Status Word.

### BUILT-IN-TEST WORD

The BUS-65112 contains a 14 bit Built-In-Test (BIT) word register which stores information about the condition of the Remote Terminal. When a Mode Command is received to transmit BIT word, the contents of this register are transmitted over the 1553 data bus. Figure 2 shows the meaning of each bit in the BIT register. Information is included regarding transmitter timeouts, loop test failures, transmitter shutdown, subsystem handshake failure, and the results of individual message validations.

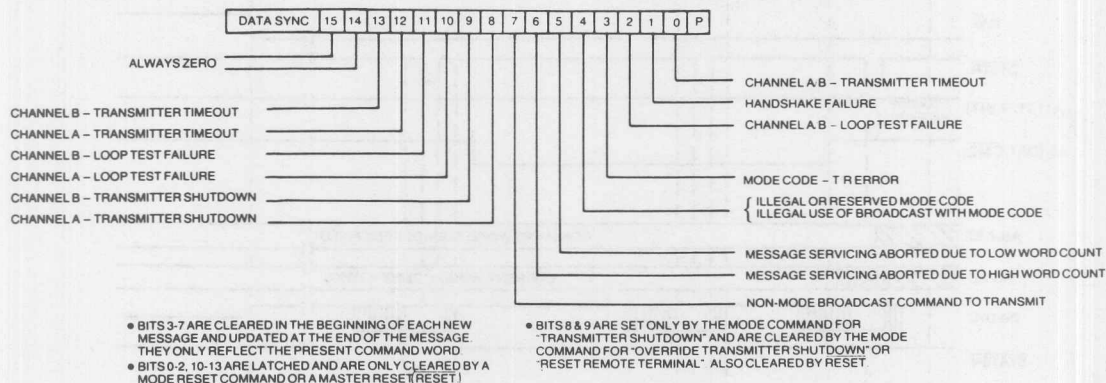


FIGURE 2. BUILT-IN-TEST (BIT) WORD REGISTER

### MODE CODES

The BUS-65112 recognizes all MIL-STD-1553 mode codes. The hybrids responses to the mode codes and error conditions are described below.

## DYNAMIC BUS CONTROL [00000]

message sequence = DBC \* STATUS

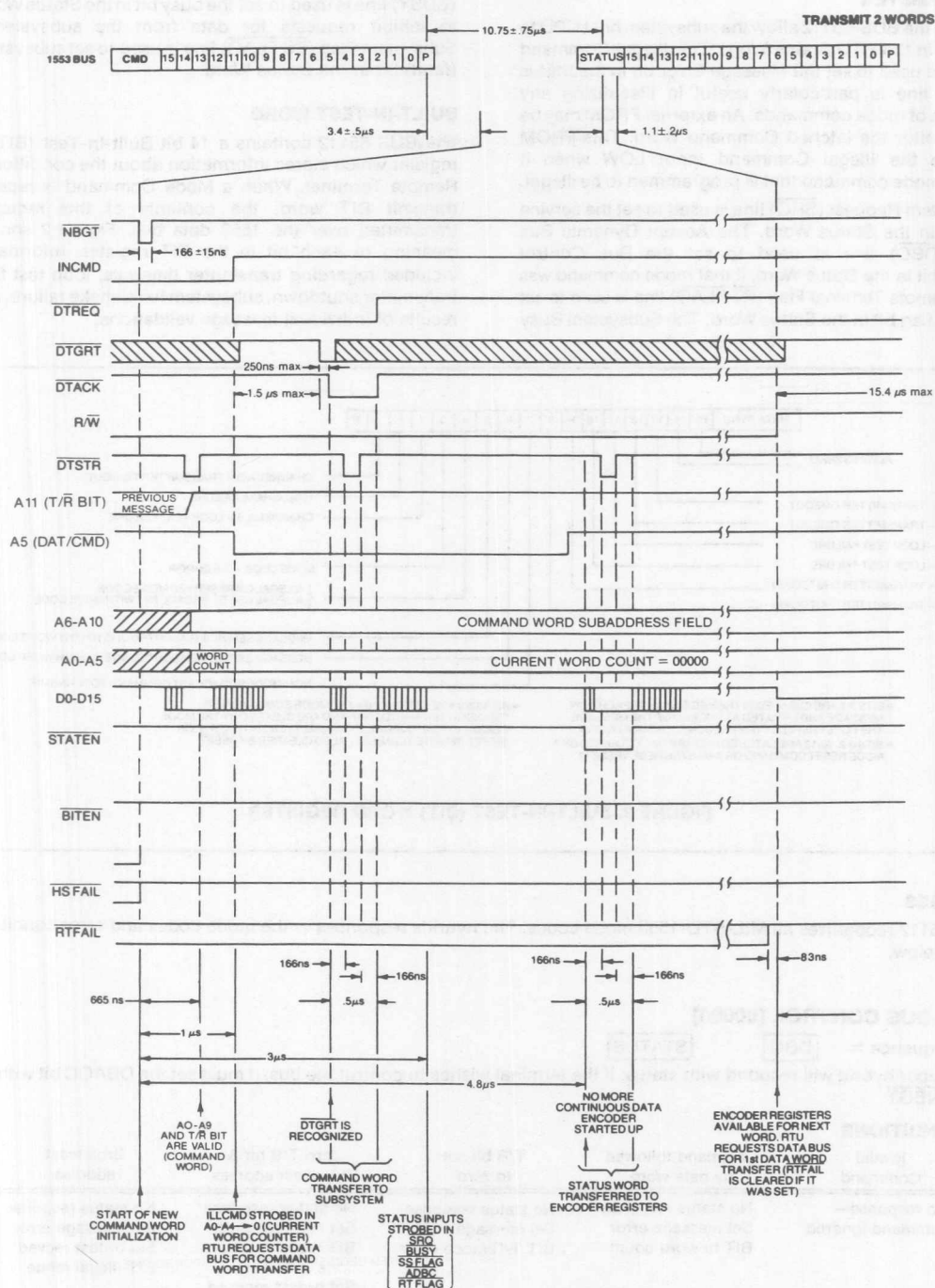
The super hybrid will respond with status; if the terminal wishes to control the bus, it must set the DBACC bit within 2.5 $\mu$ s after NBGT.

### ERROR CONDITIONS

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address	Broadcast address
No response—command ignored	No status response Set message error BIT hi word count	No status response Set message error BIT T/R mode error	No status response Set message error BIT illegal mode code & T/R error Set brdcst received	No status response Set message error Set brdcst rcvcd BIT illegal mode

(\* = status response time)

# BUS-65112 AND BUS-65117





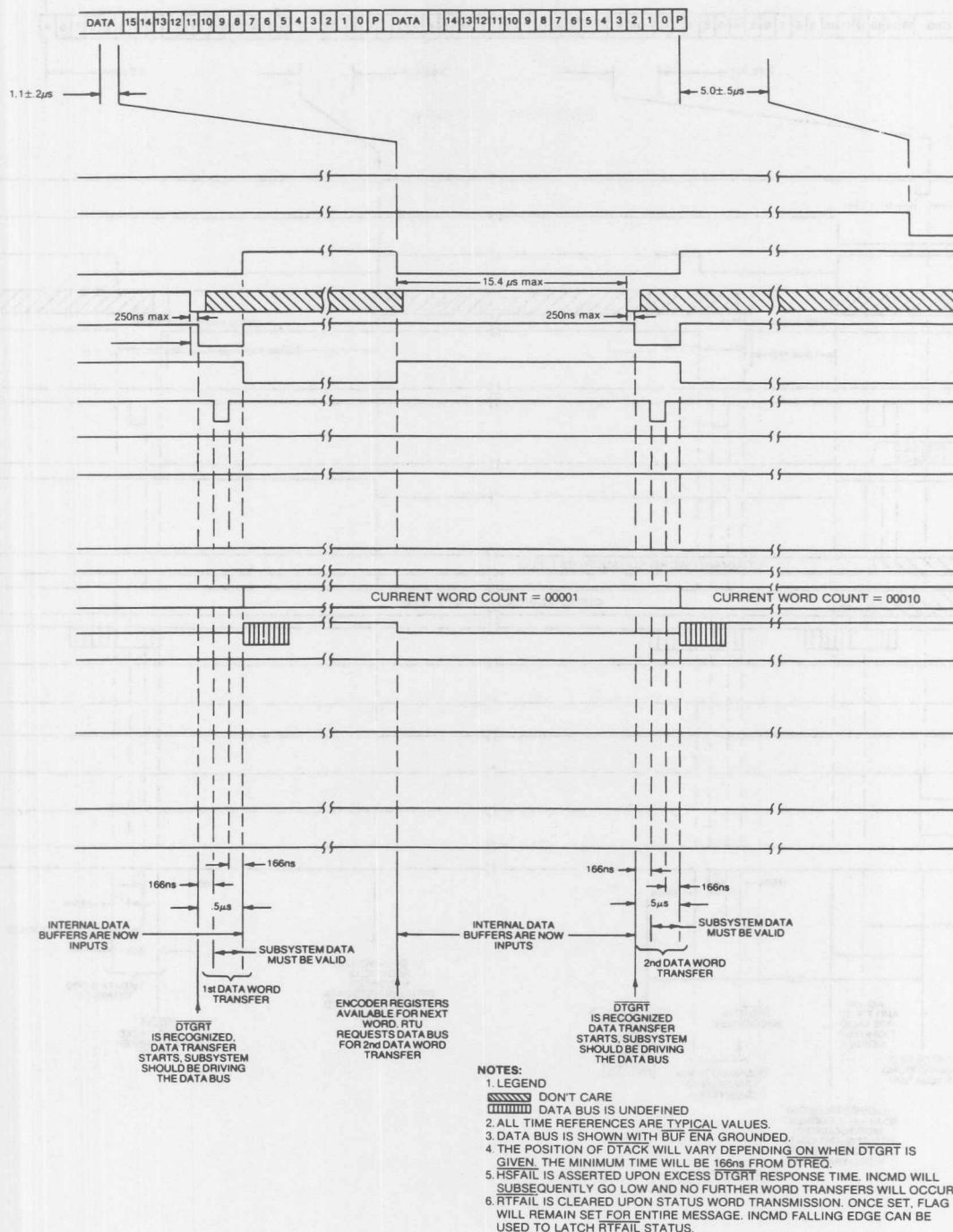
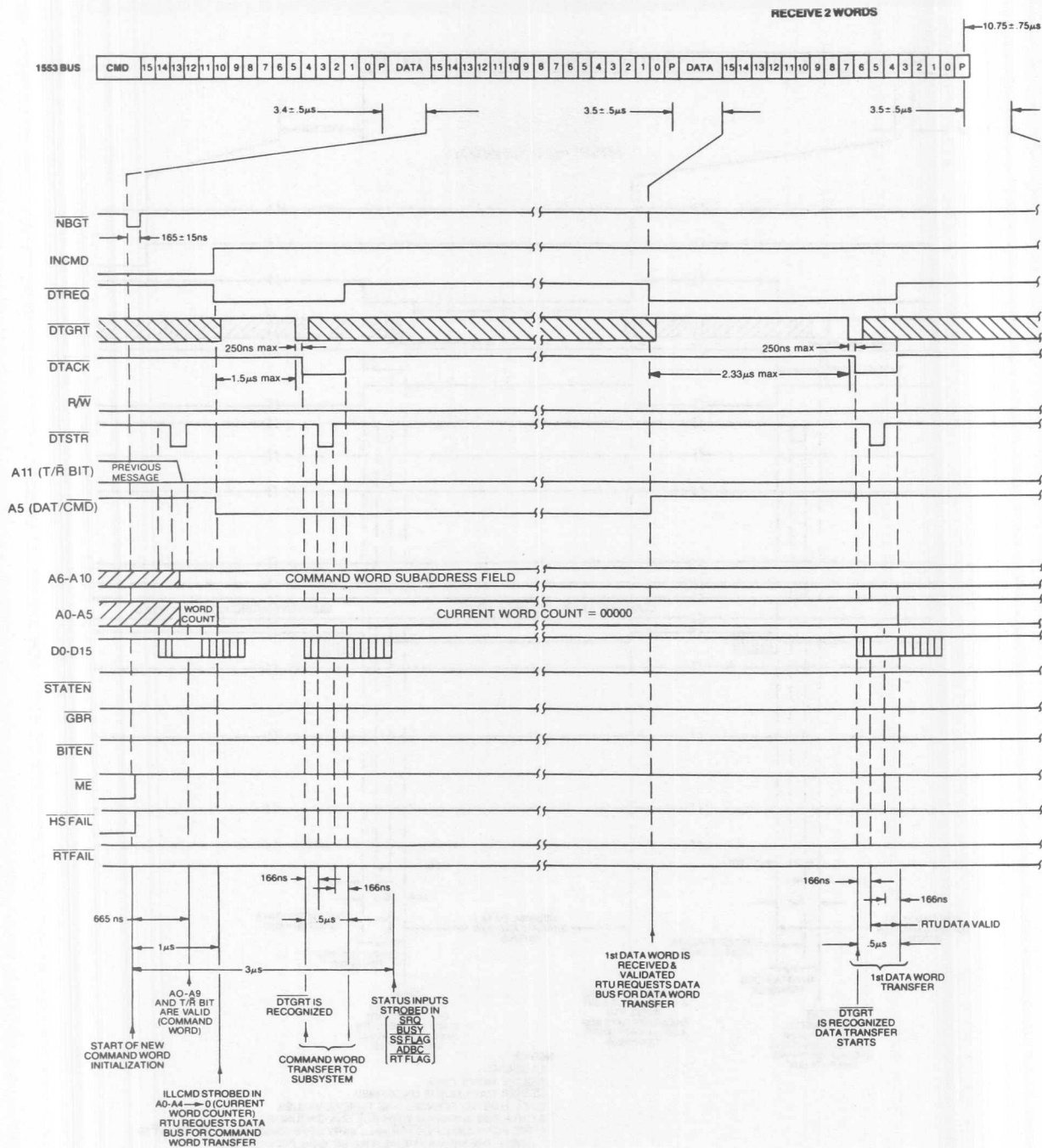
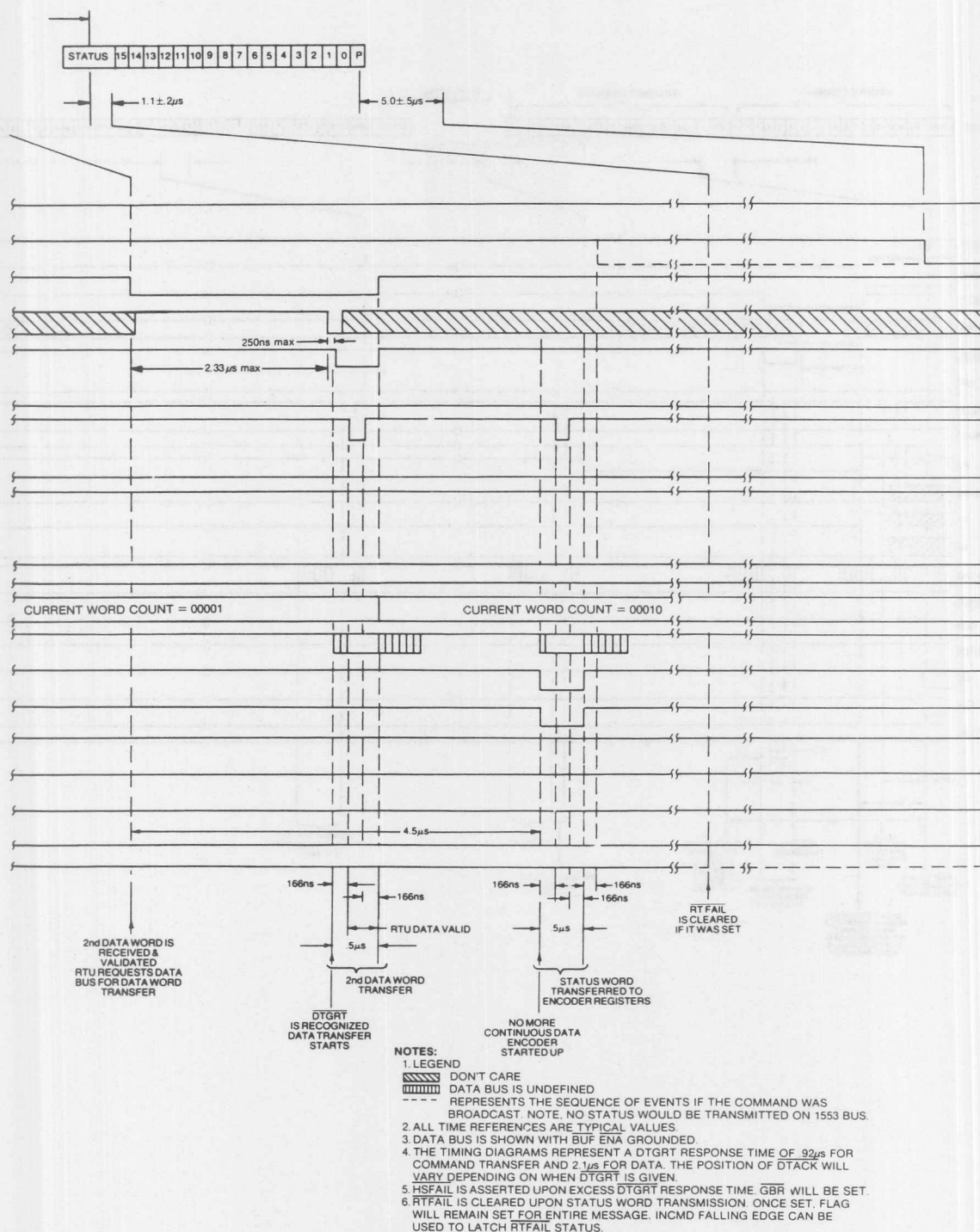
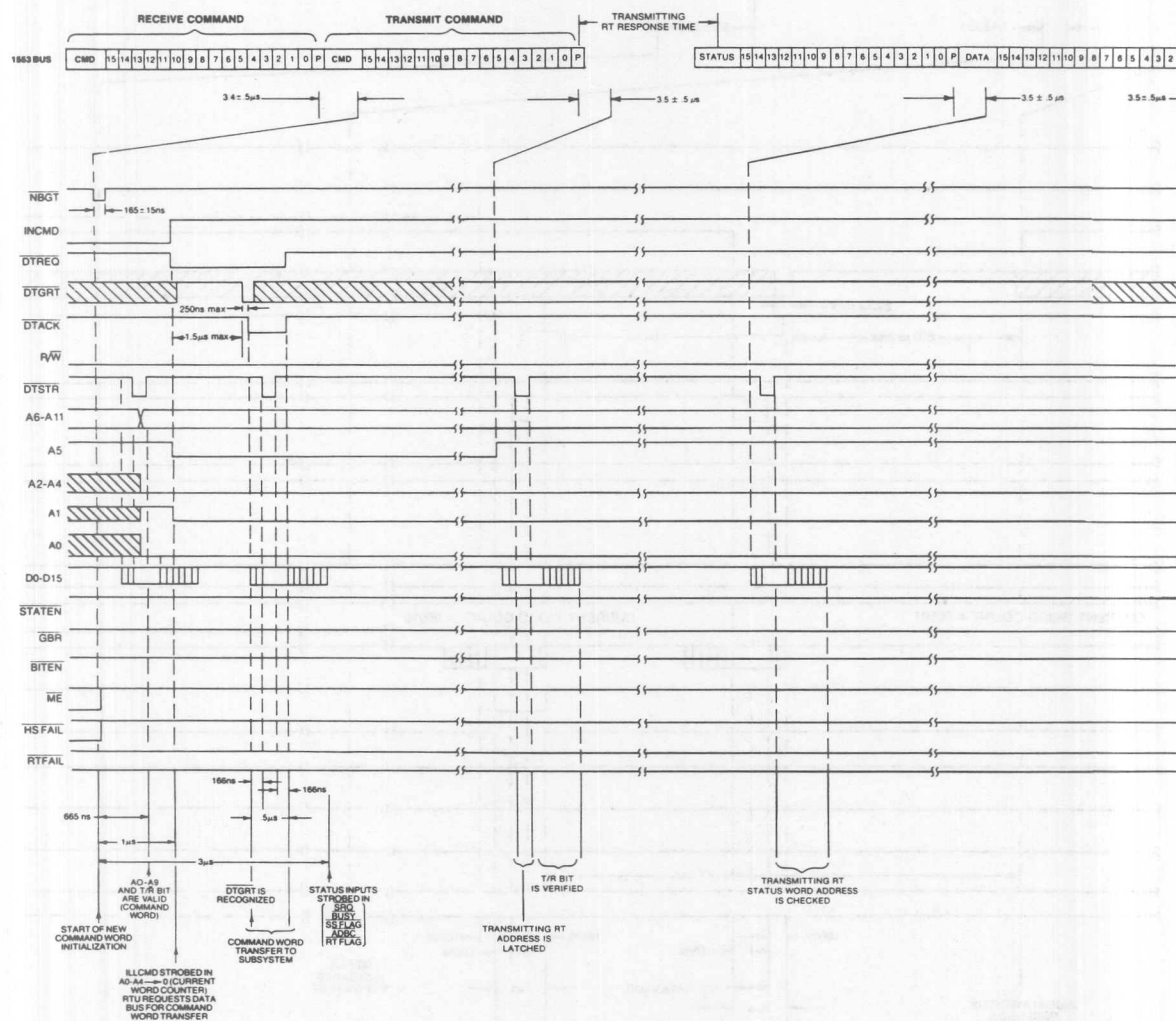


FIGURE 3. TRANSMIT TIMING DIAGRAM

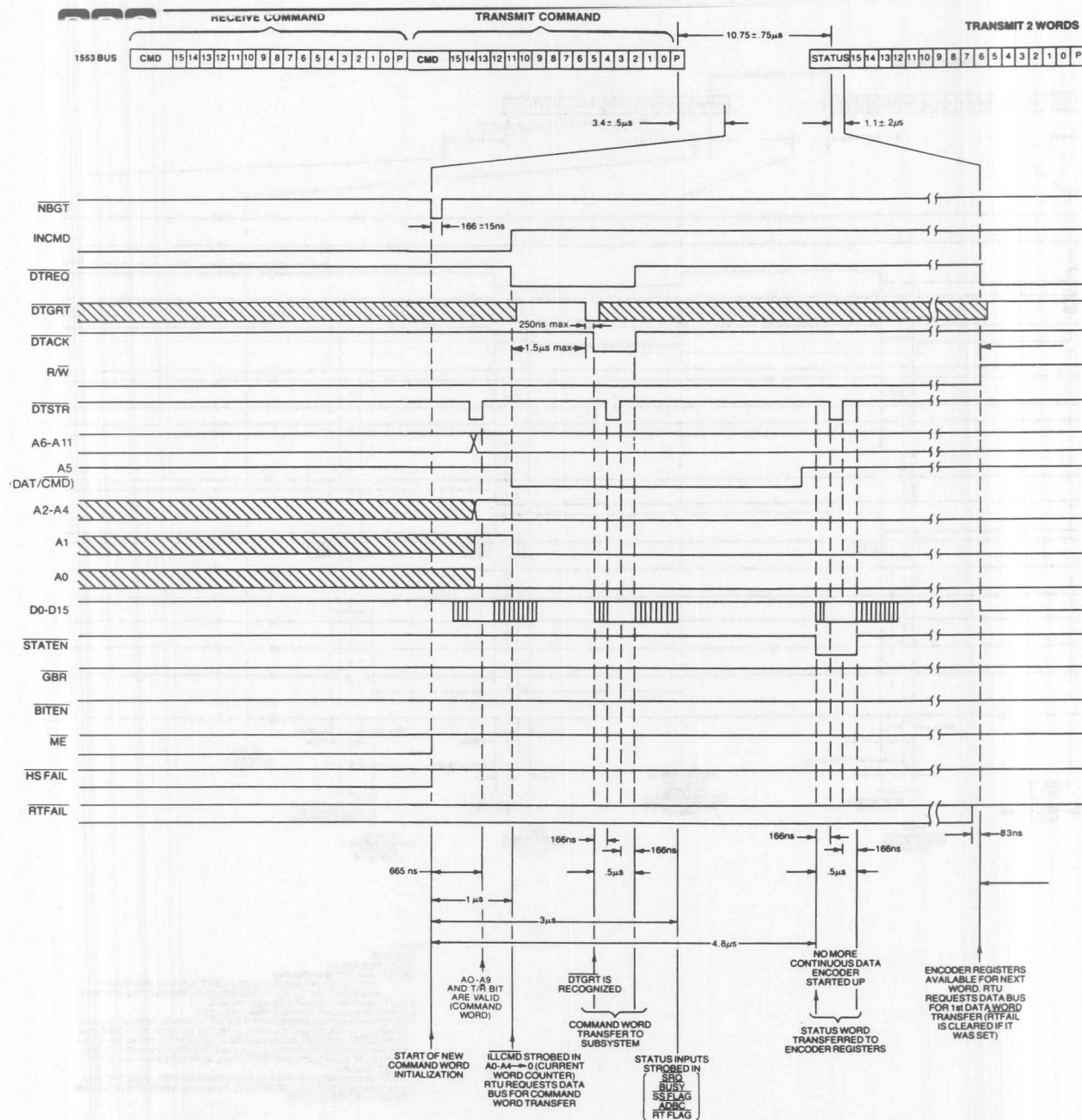












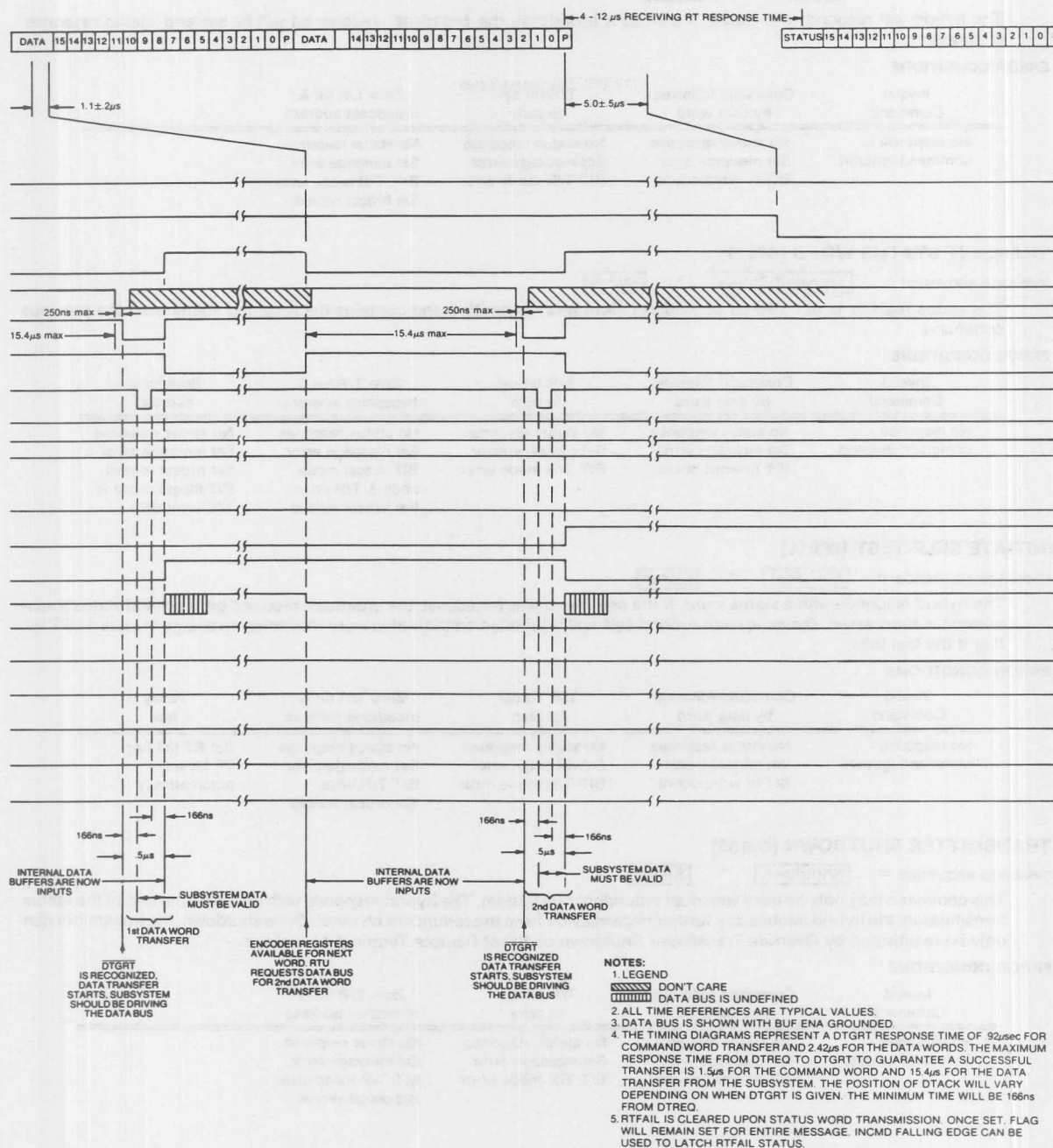


FIGURE 6. RT TO RT (TRANSMIT) TIMING DIAGRAM

## SYNCHRONIZE WITHOUT DATA WORD [00001]

message sequence = **SYNC** \* **STATUS**

The hybrid will respond with status. If sent as a broadcast, the broadcast receive bit will be set and status response suppressed.

### ERROR CONDITIONS

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address
No response - command ignored	No status response Set message error BIT hi word count	No status response Set message error BIT T/R mode error	No status response Set message error, BIT, T/R mode error Set brdcst recvd

## TRANSMIT STATUS WORD [00010]

message sequence = **Transmit Status** \* **Status**

The status register is not cleared or loaded before it is transmitted and contains the resulting status from the previous command.

### ERROR CONDITIONS

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address	Broadcast address
No response - command ignored	No status response Set message error BIT hi word count	No status response Set message error BIT T/R mode error	No status response Set message error BIT illegal mode code & T/R error Set brdcst recvd	No status response Set message error Set brdcst recvd BIT illegal mode & T/R error set

## INITIATE SELF-TEST [00011]

message sequence = **Self Test** \* **Status**

The hybrid responds with a status word. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed. Dynamic wrap-around self-test is initiated on the status word transmission and generates an RT fail flag if the test fails.

### ERROR CONDITIONS

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address	Faulty test
No response - command ignored	No status response Set message error BIT hi word count	No status response Set message error BIT T/R mode error	No status response Set message error BIT T/R error Set brdcst recvd	Set RT fail flag TF bit set automatically

## TRANSMITTER SHUTDOWN [00100]

message sequence = **Shutdown** \* **Status**

This command may only be used with dual redundant bus system. The hybrid responds with status, at the end of the status transmission, the hybrid inhibits any further transmission from the redundant channel. Once shutdown, the transmitter can only be reactivated by Override Transmitter Shutdown or Reset Remote Terminal commands.

### ERROR CONDITIONS

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address
No response - command ignored	No status response Set message error BIT hi word count	No status response Set message error BIT T/R mode error	No status response Set message error, BIT, T/R mode error Set brdcst recvd

## OVERRIDE TRANSMITTER SHUTDOWN [00101]

message sequence = **Override Shutdown** \* **Status**

This command may only be used with dual redundant bus systems. The hybrid will respond with status, at the end of the

# BUS-65112 AND BUS-65117

status transmission, the hybrid reenables the transmitter of the redundant bus. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

## ERROR CONDITIONS

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address
No response - command ignored	No status response Set message error BIT hi word count	No status response Set message error BIT T/R mode error	No status response Set message error, BIT, T/R mode error Set brdcast received

## INHIBIT TERMINAL FLAG BIT [00110]

message sequence = **Inhibit Terminal Flag** \* **Status**

The hybrid will respond with status and inhibit any further internal or external setting of the terminal flag bit in the status register. Once the terminal flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset Remote Terminal command. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

## ERROR CONDITIONS

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address
No response - command ignored	No status response Set message error BIT hi word count	No status response Set message error BIT T/R mode error	No status response Set message error BIT T/R mode error Set brdcast received

## OVERRIDE INHIBIT TERMINAL FLAG [00111]

message sequence = **Override Inhibit Terminal Flag** \* **Status**

The hybrid responds with status and reactivates the terminal flag bit in the status register. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

## ERROR CONDITIONS

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address
No response - command ignored	No status response Set message error BIT hi word count	No status response Set message error BIT T/R mode error	No status response Set message error BIT T/R mode error Set brdcast received

## RESET REMOTE TERMINAL [01000]

message sequence = **Reset Remote Terminal** \* **Status**

The hybrid responds with status and internally resets. Transmitter shutdown, mode commands and inhibit terminal flag commands will be reset. If the command was broadcast, the broadcast received bit is set and the status word is suppressed.

## ERROR CONDITIONS

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address
No response - command ignored	No status response Set message error BIT hi word count	No status response Set message error BIT T/R mode error	No status response Set message error BIT T/R mode error Set brdcast received

## RESERVED MODE CODES [01001 - 01111]

message sequence = **Reserved Mode Codes** \* **Status**

The hybrid responds with status. If the command is made illegal through an optional PROM, the message error bit is set and only the status word is transmitted.

**ERROR CONDITIONS**

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address
No response - command ignored	No status response Set message error BIT hi word count	No status response Set message error BIT illegal mode	No status response Set message error BIT illegal mode Set brdcst recvd

**TRANSMIT VECTOR WORD [10000]**

message sequence = Xmit Vector Word \* Status Vector Word

The hybrid will transmit a status word followed by the vector word. The contents of the vector word (from the subsystem) are enabled onto DB0-DB15 with the DTREQ after the command transfer (same as a data word in a normal transmit command).

**ERROR CONDITIONS**

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address	Broadcast address
No response - command ignored	No status response Set message error BIT hi word count	No status response Set message error BIT T/R mode & lo word count	No status response Set message error BIT illegal mode code, T/R error & lo word count Set brdcst received	No status response Set message error Set brdcst recvd BIT illegal mode

**SYNCHRONIZE WITH DATA WORD [10001]**

message sequence = Synchronize Data Word \* Status

The data word received following the command word is transferred to the subsystem. The status register is then enabled and then transferred onto the data highway and transmitted. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

**ERROR CONDITIONS**

Invalid Command	Cmdnd not followed by data word	Cmdnd followed by too many data words	Command T/R bit set to one	Cmdnd T/R bit set to one & brdcst address
No response - command ignored	No status response Set message error BIT lo word count	No status response Set message error BIT hi word count	No status response Set message error BIT hi word count & T/R error	No status response Set message error Set brdcst recvd BIT hi word count & T/R mode error

**TRANSMIT LAST COMMAND [10010]**

message sequence = Xmit Last Command \* Status Last Command

The status register is not cleared or loaded before transmission; it contains the status from the previous command. The data word transmitted contains the previous valid command (providing it was not another transmit last command).

**ERROR CONDITIONS**

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address	Broadcast address
No response - command ignored	No status response Set message error BIT high word count	No status response Set message error BIT T/R mode & lo word count	No status response Set message error BIT illegal mode code & T/R error	No status response Set message error Set brdcst recvd BIT illegal mode code

**TRANSMIT BIT WORD [10011]**

message sequence = Transmit BIT Word \* Status BIT word

The hybrid responds with status followed by the BIT word. BITEN when active will allow the subsystem to latch the BIT word on the parallel data bus.



PIN FUNCTION TABLE		
PIN	FUNCTION	DESCRIPTION
1	A10	Latched output of the most significant bit (MSB) in the subaddress field of the command word.
2	A8	Latched output of the third most significant bit in the subaddress field of the command word.
3	A6	Latched output of the least significant bit (LSB) in the subaddress field of the command word.
4	DB1	Bi-directional parallel data bus Bit 1
5	DB3	Bi-directional parallel data bus Bit 3
6	DB5	Bi-directional parallel data bus Bit 5
7	DB7	Bi-directional parallel data bus Bit 7
8	DB9	Bi-directional parallel data bus Bit 9
9	DB11	Bi-directional parallel data bus Bit 11
10	DB13	Bi-directional parallel data bus Bit 13
11	DB15	Bi-directional parallel data bus Bit 15 (MSB)
12	BRO ENA	Broadcast enable – when HIGH, this input allows recognition of an RT address of all ones in the command word as a broadcast message. When LOW, it prevents response to RT address 31 unless it was the assigned terminal address.
13	ADDRE	Input of the MSB of the assigned terminal address.
14	ADDRC	Input of the 3rd MSB of the assigned terminal address.
15	ADDRA	Input of the LSB of the assigned terminal address.
16	RTADERR	Output signal used to inform subsystem of an address parity error. If LOW, indicates parity error and the RT will not respond to any command address to a single terminal. It will respond to broadcast commands if BRO ENA is HIGH.
17	TXDATA B	LOW output to the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
18	+15VB	+15 volt input power supply connection for the B channel transceiver.
19	GND B	Power supply return connection for the B channel transceiver.
20	RXDATA B	Input from the HIGH side of the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
21	A3	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 2ns MSB of the current word counter.
22	A1	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd LSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter.

PIN FUNCTION TABLE		
PIN	FUNCTION	DESCRIPTION
23	DTGRT	Data transfer grant – active LOW input signal from the subsystem that informs the RT, when DTREQ is asserted, to start the transfer. Once transfer is started, DTGRT can be removed.
24	INCMD	In Command – HIGH level output signal used to inform the subsystem that the RT is presently servicing a command.
25	HSFAIL	Handshake Fail – output signal that goes LOW and stays LOW whenever the subsystem fails to supply DTGRT in time to do a successful transfer. Cleared by the next NBGT.
26	DTSTR	A LOW level output pulse (166ns) present in the middle of every data word transfer over the parallel data bus. Used to latch or strobe the data into memory, FIFOs, registers, etc. Recommend using the rising edge to clock data in.
27	(DAT/CMD) A5	Address line output that is LOW whenever the command word is being transferred to the subsystem over the parallel data bus, and is HIGH whenever data words are being transferred.
28	RTFAIL	Remote Terminal Failure – latched active LOW output signal to the subsystem to flag detection of a remote terminal continuous self-test failure. Cleared by the start of the next message transmission (status word) and set if problem is again detected.
29	DTREQ	Data Transfer Request – active LOW output signal to the subsystem indicating that the RT has data for or needs data from the subsystem and requests a data transfer over the parallel data bus. Will stay LOW until transfer is completed or transfer timeout has occurred.
30	ADBC	Accept Dynamic Bus Control – active LOW input signal from subsystem used to set the Dynamic Bus Control Acceptance bit in the status register if the command word was a valid, legal mode command for dynamic bus control.
31	TEST 2	Factory test point – DO NOT USE.
32	A11 (T/R)	Latched output of the T/R bit in the command word.
33	ILLCMD	Illegal Command – Active LOW input signal from the subsystem, strobed in on the rising edge of INCMD. Used to define the command word as illegal and to set the message error bit in the status register.
34	SRQ	Subsystem Service Request – Input from the subsystem used to control the Service Request Bit in the status register. If LOW when the status word is updated, the Service Request Bit will be set; if HIGH, it will be cleared.
35	BITEN	Built-in-Test Word Enable – LOW level output pulse (.5μsec), present when the built-in-test word is enabled on the parallel data bus.
36	RXDATA A	Input from the LOW side of the primary side of the coupling transformer that connects to the A Channel of the 1553 Bus.
37	+5VA	+5 volt input power supply connection for the A channel transceiver.

PIN FUNCTION TABLE		
PIN	FUNCTION	DESCRIPTION
38	-15VA	-15 volt input power supply connection for the A Channel transceiver.
39	TXDATA A	HIGH output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
40	NBGT	New Bus Grant - LOW level output pulse (166 ns) used to indicate the start of a new protocol sequence in response to the command word just received.
41	A9	Latched output of the 2nd MSB in the subaddress field of the command word.
42	A7	Latched output of the 2nd LSB in the subaddress field of the command word.
43	DB0	Bidirectional parallel data bus Bit 0 (LSB)
44	DB2	Bidirectional parallel data bus Bit 2
45	DB4	Bidirectional parallel data bus Bit 4
46	DB6	Bidirectional parallel data bus Bit 6
47	DB8	Bidirectional parallel data bus Bit 8
48	DB10	Bidirectional parallel data bus Bit 10
49	DB12	Bidirectional parallel data bus Bit 12
50	DB14	Bidirectional parallel data bus Bit 14
51	+5V	+5 Volt input power supply connection for RTU digital logic section.
52	GND	Power supply return for RTU digital logic section.
53	ADDRD	Input of the 2nd MSB of the assigned terminal address.
54	ADDRB	Input of the 2nd LSB of the assigned terminal address.
55	ADDRP	Input of Address Parity Bit. The combination of assigned terminal address and ADDR <sub>P</sub> must be odd parity for the RT to work.
56	TXDATA B	HIGH, output to the primary side of the coupling transformer that connects to the B Channel of the 1553 Bus.
57	-15VB	-15 volt input power supply connection for the B channel transceiver.
58	+5VB	+5 volt input power supply connection for the B channel transceiver.
59	RXDATA B	Input from the LOW side of the primary side of the coupling transformer that connects to the B Channel of the 1553 Bus.
60	A2	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the 3rd MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 3rd MSB of the current word counter.
61	A0	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the LSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the LSB of the current word counter.
62	DTACK	Data Transfer Acknowledge - active LOW output signal during data transfers to or from the subsystem indicating the RTU has received the DTGRT in response to DTREQ and is presently doing the transfer. Can be connected directly to pin 67 (BUF ENA) for control of tri-state data buffers; and to tri-state address buffer control lines, if they are used.

PIN FUNCTION TABLE		
PIN	FUNCTION	DESCRIPTION
63	A4	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the MSB of the current word counter.
64	R/W	Read/Write - output signal that controls the direction of the internal data bus buffers. Normally, the signal is LOW and the buffers drive the data bus. When data is needed from the subsystem, it goes HIGH to turn the buffers around and the RT now appears as an input. The signal is HIGH only when DTREQ is active (LOW).
65	GBR	Good Block Received - LOW level output pulse (5μsec) used to flag the subsystem that a valid, legal, non-mode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem.
66	12MHz IN	12MHz Clock Input - input for the master clock used to run RTU circuits.
67	BUF ENA	Buffer Enable - input used to enable or tri-state the internal data bus buffers when they are driving the bus. When LOW, the data bus buffers are enabled. Could be connected to DTACK (Pin 62) if RT is sharing the same data bus as the subsystem.
68	RESET	Input resets entire RT when LOW.
69	RTFLAG	Remote Terminal Flag - input signal used to control the terminal flag bit in the status register. If LOW when the status word is updated, the terminal flag bit would be set; if HIGH, it would be cleared. Normally connected to RTFAIL (Pin 28).
70	TEST 1	Factory test point - DO NOT USE.
71	BUSY	Subsystem Busy - input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set; if HIGH, it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands, data will still be transferred to subsystem.
72	SSFLAG	Subsystem Flag - input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated, the subsystem flag will be set; if HIGH, it will be cleared.
73	ME	Message Error - output signal that goes LOW and stays LOW whenever there is a format or word error with the received message over the 1553 Data Bus. Cleared by the next NBGT.
74	RXDATA A	Input from the HIGH side of the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
75	GND A	Power supply return connection for the A Channel transceiver.
76	+15VA	+15 volt input power supply connection for the A channel transceiver.
77	TXDATA A	LOW output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
78	STATEN	Status Word Enable - LOW level active output signal present when the status word is enabled on the parallel data bus.

## ERROR CONDITIONS

Invalid Command	Command followed by data word	T/R bit set to zero	Zero T/R bit & broadcast address	Broadcast address
No response - command ignored	No status response Set message error	No status response Set message error BIT T/R mode error & lo word count	No status response Set message error BIT illegal mode code, T/R error & lo word count	No status response Set message error Set brdcst rcvcd BIT illegal mode

## SELECTED TRANSMITTER SHUTDOWN [10100]

message sequence = Transmitter Shutdown Data \* Status

The data word received is transferred to the subsystem and then the status word is transmitted. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed. Intended for RTs with more than dual redundant channels.

## ERROR CONDITIONS

Invalid Command	Cmnd not followed by data word	Cmnd followed by too many data words	Cmnd T/R bit set to one	Cmnd T/R bit to one & broadcast address
No response - command ignored	No status response Set message error BIT lo word count & illegal mode	No status response Set message error BIT hi word count & illegal mode	No status response Set message error BIT illegal mode & hi word count	No status response Set message error Set brdcst rcvcd BIT illegal mode & hi word count

## OVERRIDE SELECTED TRANSMITTER SHUTDOWN [10101]

message sequence = Override Shutdown Data \* Status

The data word received after the command word is transferred to the subsystem. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

## ERROR CONDITIONS

Invalid Command	Cmnd not followed by data word	Cmnd followed by too many data words	Cmnd T/R bit set to one	Cmnd T/R set to one & broadcast address
No response - command ignored	No status response Set message error BIT lo word count & illegal mode	No status response Set message error BIT hi word count & illegal mode	No status response Set message error BIT illegal mode & hi word count	No status response Set message error Set brdcst rcvcd BIT illegal mode, hi word count & T/R mode

## RESERVED MODE CODES [10110 - 11111]

message sequence = Reserved Mode Code (T/R=1) \* Status  
Reserved Mode Code (T/R=0) \* Status

The hybrid responds with status. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

## ERROR CONDITIONS

T/R=1		T/R=0		
Invalid Command	Command followed by data word	Invalid Command	Cmnd not followed by contiguous data word	Cmnd followed by too many data words
No response - command ignored	No status response Set message error BIT hi word count & illegal mode	No response - command ignored	No status response Set message error BIT illegal mode & lo word count	No status response Set message error BIT hi word count & illegal mode

## Command Word Illegalizing

Any command, including mode codes, can be illegalized. When an illegalized command or mode code is received, the RTU will set the message error bit of the status register and transmit the status word. Data received with an illegal command will be passed on to the subsystem, and data to be transmitted will not be requested from the subsystem, only the status word with the message error bit set will be transmitted.

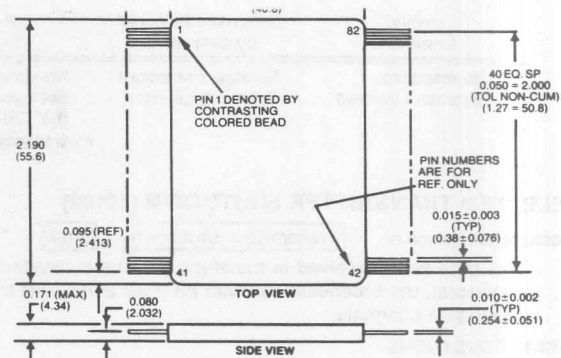
The BUS-65112 is capable of performing two internal tests.

**TEST 1, PIN 70.** A logic low on this pin will cause the last word of the next message to be repeated continuously until the built in Watch Dog Timeout circuit disables the transmitter. The transmitter will be re-enabled upon receipt of the next valid command to the BUS-65112 on that channel.

**TEST 2, PIN 31.** This pin indicates the result of the loop test comparison test. It is performed for every word transmitted to the 1553 bus.

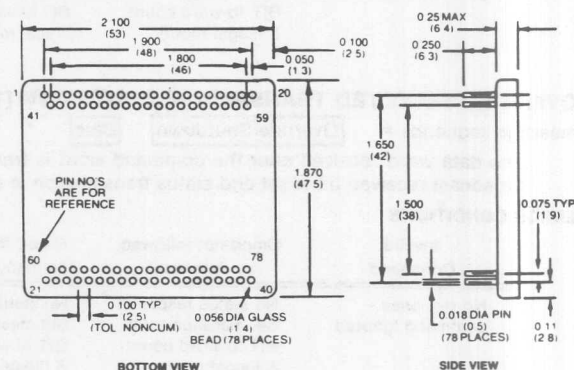
(1 = Pass, 0 = Fail) The result is reset upon transmission of the next word over the bus.

BUS-65117 FLATPACK PIN FUNCTIONS			
PIN	FUNCTION	PIN	FUNCTION
1	NC	42	NC
2	A10	43	NBGT
3	A9	44	STATEN
4	A8	45	TXDATA OUT A
5	A7	46	TXDATA OUT A
6	A6	47	-15VA
7	DB0	48	+15VA
8	DB1	49	+5VA
9	DB2	50	GND A
10	DB3	51	RXDATA IN A
11	DB4	52	RXDATA IN A
12	DB5	53	BITEN
13	DB6	54	ME
14	DB7	55	SRQ
15	DB8	56	SSFLAG
16	DB9	57	ILLCMD
17	DB10	58	BUSY
18	DB11	59	A11
19	DB12	60	TEST 1
20	DB13	61	TEST 2
21	DB14	62	RTFLAG
22	DB15	63	ABDC
23	-5V	64	RESET
24	BRO ENA	65	DTREQ
25	GROUND	66	BUFENA
26	ADDRE	67	RTFAIL
27	ADDRD	68	12 MHz IN
28	ADDRC	69	A5
29	ADDRB	70	GBR
30	ADDR A	71	DTSTR
31	ADDRP	72	R/W
32	RTADERR	73	HSFAIL
33	TXDATA OUT B	74	A4
34	TXDATA OUT B	75	INCMD
35	-15VB	76	DTACK
36	+15VB	77	DTGRT
37	+5VB	78	A0
38	GND B	79	A1
39	RXDATA IN B	80	A2
40	RXDATA IN B	81	A3
41	NC	82	NC



Note: Dimensions are in inches (millimeters).

FIGURE 7. BUS-65117 MECHANICAL OUTLINE (FLATPACK)



Note: Dimensions are in inches (millimeters).

FIGURE 8. BUS-65112 MECHANICAL OUTLINE (DDIP)

## ORDERING INFORMATION

BUS-65112 - 883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883.

B = Screened to MIL-STD-883 but without QCI testing.

Blank = 0° to 70°C operation

Power Supply and Packaging

2 = ±15VDC, DDIP

3 = ±12VDC, DDIP

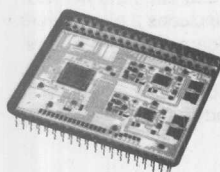
7 = ±15VDC, Flatpack

8 = ±12VDC, Flatpack



# BUS-65142 AND BUS-65144

## MIL-STD-1553 DUAL REDUNDANT REMOTE TERMINAL HYBRID



### DESCRIPTION

The BUS-65142 is a complete dual redundant MIL-STD-1553 Remote Terminal Unit (RTU) packaged in a small 1.9" x 2.1" hybrid. The device is based upon two DDC custom ICs, which includes two monolithic low power Mark II transceivers and one CMOS-SOS RTU protocol containing data buffers and timing control logic. It supports all 13 mode codes for dual redundant operation, any combination of which can be illegalized. Parallel data transfers are accomplished with a DMA type handshaking, compatible with most CPU types. Data transfers to/from memory are simplified by the latched command word and word count outputs. Error detection and recovery

are enhanced by BUS-65142 special features. A 14 bit built-in-test word register stores RTU information, and sends it to the Bus Controller in response to the Mode Command Transmit Bit Word. The BUS-65142 performs continuous on-line wrap-around self-test, and provides 4 error flags to the host CPU. Inputs are provided for host CPU control of 6 bits of the RTU Status Word.

Its small hermetic package, -55°C to +125°C operating temperature range, and complete RTU operation make the BUS-65142 ideal for most MIL-STD-1553 applications requiring hardware or microprocessor subsystems.

### FEATURES

- LOW POWER & LOW COST
- HIGH RELIABILITY
- SOS & BIPOLAR
- SUPPORTS ALL 13 MODE CODES
- MODE CODE/CMD WORD ILLEGALIZATION
- DMA TRANSFERS
- CONTINUOUS SELF-TEST
- SEAFAC TESTED COMPONENTS
- BUILT-IN-TEST WORD REGISTER
- 16MHz DECODERS OFFER IMPROVED NOISE REJECTION & ZERO CROSSING DETECTION

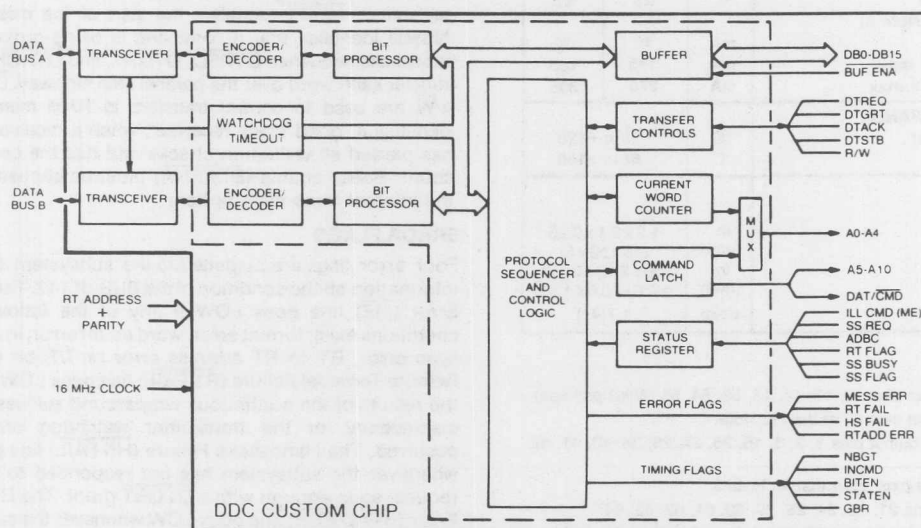


FIGURE 1. BUS-65142 BLOCK DIAGRAM



SPECIFICATIONS			
PARAMETER		UNITS	VALUE
<b>RECEIVER</b>			
Differential Input Impedance (DC to 1 MHz)	kΩ		4 min
Differential Input Voltage	V <sub>p-p</sub>		40 max
Input Threshold (Direct Coupled)	V <sub>p-p</sub>		0.70 min, 1.20 max
CMRR (DC to 2 MHz)	dB		40 min
CMV (DC to 2 MHz)	V		± 10 min
<b>TRANSMITTER</b>			
Differential Output Voltage			
Direct Coupled (Across 145Ω Load)	V <sub>p-p</sub>		30 typ
Transformer Coupled (at Stub)	V <sub>p-p</sub>		21 typ
Output Rise and Fall Times (Note 7)	ns		160 typ
Output Noise	mV <sub>p-p</sub>		10 max
<b>LOGIC</b>			
V <sub>IH</sub>	V		2.4 min
V <sub>IL</sub>	V		0.7 max
I <sub>IH</sub> (Note 1 & 6) (V <sub>IH</sub> = 2.7V)	mA		0.04 min, 0.2 max
I <sub>IH</sub> (Note 2) (V <sub>IH</sub> ≥ 2.4V)	μA		± 20 max
I <sub>IL</sub> (Note 1 & 6) (V <sub>IL</sub> = 0.4V)	mA		- 0.4 max
I <sub>IL</sub> (Note 2) (V <sub>IL</sub> ≥ 0.7V)	μA		± 20 max
V <sub>OH</sub> (Note 3) (I <sub>OH</sub> = - 0.4mA)	V		2.4 min
V <sub>OH</sub> (Note 4) (I <sub>OH</sub> = - 0.4mA)	V		2.4 min
V <sub>OH</sub> (Note 6) (I <sub>OH</sub> = - 0.4mA)	V		2.4 min
V <sub>OL</sub> (Note 3) (I <sub>OL</sub> = - 2mA)	V		0.4 max
V <sub>OL</sub> (Note 5) (I <sub>OL</sub> = - 2mA)	V		0.4 max
V <sub>OL</sub> (Note 6) (I <sub>OL</sub> = - 4mA)	V		0.4 max
C <sub>i</sub> (f = 1 MHz)	pF		50 max
C <sub>o</sub> (f = 1 MHz)	pF		10 typ
C <sub>IO</sub> (Note 6) (f = 1 MHz)	pF		50 max
<b>POWER SUPPLIES (TOTAL HYBRID)</b>			
+5VDC		<b>65142</b>	<b>65143</b>
Tolerance, max	%	± 10	± 10
Current Drain, max	mA	115	115
- 15VDC or - 12VDC			
Tolerance, max	%	± 5	± 5
Current Drain (Note 8)			
Idle, max	mA	70	70
50% Transmit, max	mA	175	185
100% Transmit, max	mA	270	305
<b>TEMPERATURE RANGE</b>			
Operating (Case)	°C	- 55 to + 125	
Storage	°C	- 65 to + 150	
<b>PHYSICAL</b>			
Size			
DDIP	in. (mm)	1.9 x 2.1 x 0.25 (48 x 53 x 6)	
Flatpack	in. (mm)	1.6 x 2.19 x 0.171 (40.6 x 55.6 x 4.34)	
Weight	oz(g)	1.7(41)	

**Notes:**

1. I<sub>IH</sub> and I<sub>IL</sub> for input pins 12, 13, 14, 15, 53, 54, 55 (30k $\Omega$  pull-ups).
2. I<sub>IH</sub> and I<sub>IL</sub> for input pins other than in Note 1.
3. V<sub>OH</sub> and V<sub>OL</sub> for output pins 1, 2, 3, 16, 25, 27, 28, 35, 40, 41, 42, 65, 73, 78.
4. V<sub>OH</sub> for all output pins other than in Note 3.
5. V<sub>OL</sub> for output pins 21, 22, 24, 26, 29, 60, 61, 62, 63, 64.
6. V<sub>OL</sub> and C<sub>IO</sub> for pins 43 thru 50 and 4 thru 11 (45k $\Omega$  pull-ups).
7. 120ns min, 200ns max
8. Measured at 5.5V; -15.75V

**GENERAL**

The BUS-65142 is a complete dual redundant Remote Terminal Unit (RTU) packaged in a small 1.9"x2.1" hybrid. It is fully compliant with MIL-STD-1553B and supports all message formats. As shown in Figure 1, it includes 2 transceivers and a custom chip containing 2 encoders, 2 bit processors, an RTU protocol sequencer and control logic, output latches, and buffers. With the addition of 2 data bus transformers (DDC P/N BUS-25679), BUS-65142 is ready to connect to the MIL-STD-1553 data bus.

Data is transferred to and from the subsystem host CPU over a 16 bit parallel highway, which is isolated by a set of bi-directional buffers. All transfers are made with a DMA type handshaking of request, grant, and acknowledgment. Read/write and data strobes are provided to simplify interfacing to external RAM. Also simplifying the RAM interface is the availability of latched command word and an auto-incrementing word counter. These signals may be used as an address to map the data directly to and from RAM.

BUS-65142 allows the subsystem host CPU to control 6 of the bits in the RTU status word. Of particular interest is the Illegal Command input which may be used to set the message error bit and illegalize any command word. Four error flags are provided to the subsystem host CPU by the BUS-65142, to aid in assessing its condition. In addition, a continuous on-line self-test is performed by the BUS-65142 on every transmission. The last Transmitted Word of each message is wrapped around the decoder and compared against the Actual Word. Any discrepancy is flagged as an error.

**TIMING**

The subsystem host CPU interface to the BUS-65142 is simple and compatible with most microprocessors. Figures 3 and 4 illustrate typical MIL-STD-1553 messages of transmit data and receive data, and figures 5 and 6 show RT to RT transfers. In each case, NBGT identifies the start of the message, and INCMD identifies that a command is being processed. The handshake sequence DTREQ, DTGRT, and DTACK is used to transfer each word over the parallel data highway. DTSTR and R/W are used to control transfers to RAM memory. GBR identifies a "good block received", when a received message has passed all validation checks and has the correct word count. Buffer enable (BUFENA) must be applied to enable the internal three-state buffers.

**ERROR FLAGS**

Four error flags are outputted to the subsystem to provide information on the condition of the BUS-65142. The Message Error (ME) line goes LOW if any of the following error conditions exist: format error, word count error, invalid word, sync error, RT to RT address error or T/R bit error. The Remote Terminal Failure (RT FAIL) line goes LOW whenever the results of the continuous wraparound self-test shows a discrepancy, or the transmitter watchdog timeout has occurred. The Handshake Failure (HS FAIL) line goes LOW whenever the subsystem has not responded to a DTREQ request soon enough with a DTGRT grant. The RT Address Error (RTAD ERR) line goes LOW whenever the sum of the 5 address lines and parity lines show a parity error (the terminal will not respond to commands while this error condition exists).

## STATUS REGISTER

Six inputs to the BUS-65142 allow the subsystem host CPU to control bits in the RTU Status Word. The Illegal Command input may be used to set the Message Error bit in the Status Word and suppress the transmission of data to the bus controller. This line is particularly useful in illegalizing any combination of commands. The latched Command Word may be connected to the address pins which lead to an optional external PROM, that would drive the Illegal Command input LOW when it identifies a command that is programmed to be illegal.

The Subsystem Request ( $\overline{SRQ}$ ) line is used to set the service request bit in the Status Word. The Accept Dynamic Bus Control ( $\overline{ADBC}$ ) line is used to set the Bus Control acceptance bit in the Status Word, if that mode command was sent. The Remote Terminal Flag (RT FLAG) line is used to set the terminal flag bit in the Status Word. The Subsystem Busy ( $\overline{BUSY}$ ) line is used to set the busy bit in the Status Word, and to inhibit requests for data from the subsystem. The Subsystem Flag ( $\overline{SS FLAG}$ ) line is used to set subsystem flag (fault) bit in the Status Word.

## BUILT-IN-TEST WORD

The BUS-65142 contains a 14 bit Built-In-Test (BIT) word register which stores information about the condition of the Remote Terminal. When a Mode Command is received to transmit BIT word, the contents of this register are transmitted over the 1553 data bus. Figure 2 shows the meaning of each bit in the BIT register. Information is included regarding transmitter timeouts, loop test failures, transmitter shutdown, subsystem handshake failure, and the results of individual message validations.

## MODE CODES

The BUS-65142 implements all mode codes applicable to dual-redundant systems. Mode codes can also be illegalized using the appropriate I/O signals. Mode command illegalization and handling are detailed in the RTU Operation section and listed in table 2.

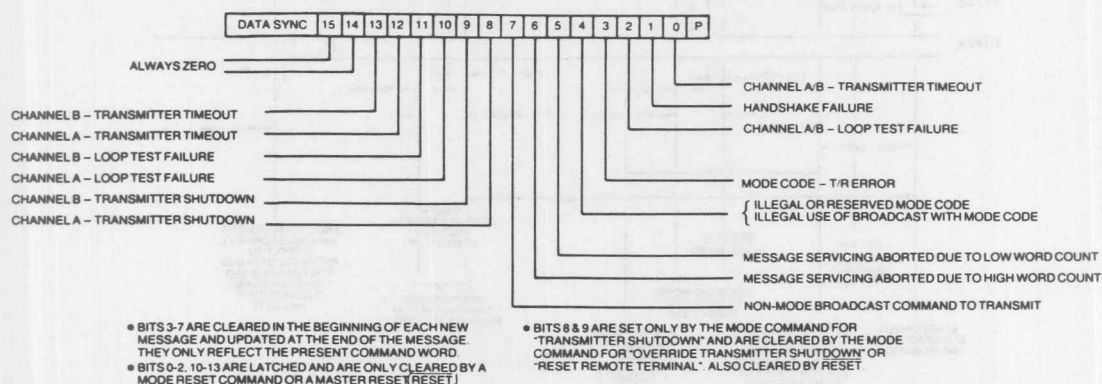
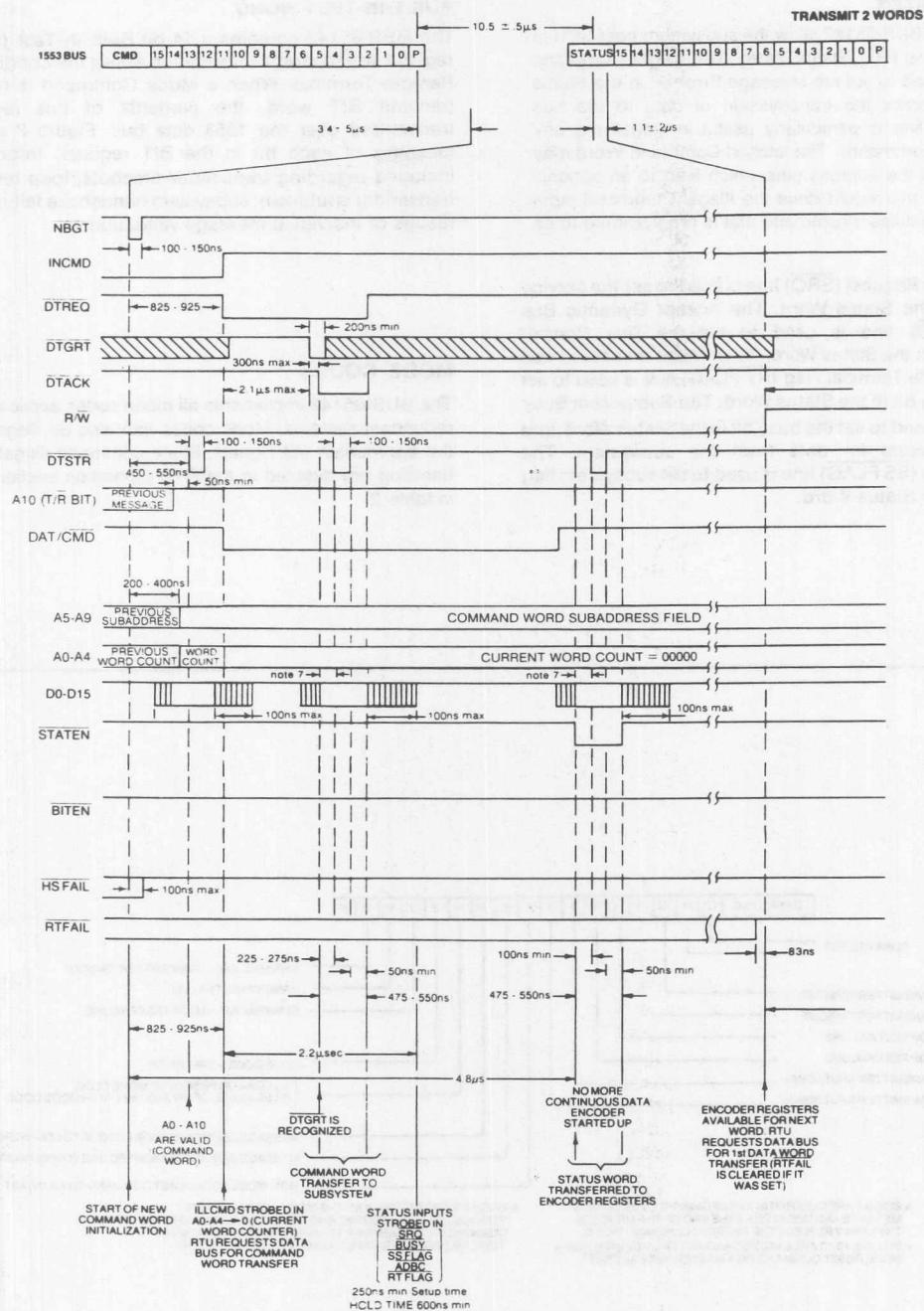


FIGURE 2. BUILT-IN-TEST (BIT) WORD REGISTER



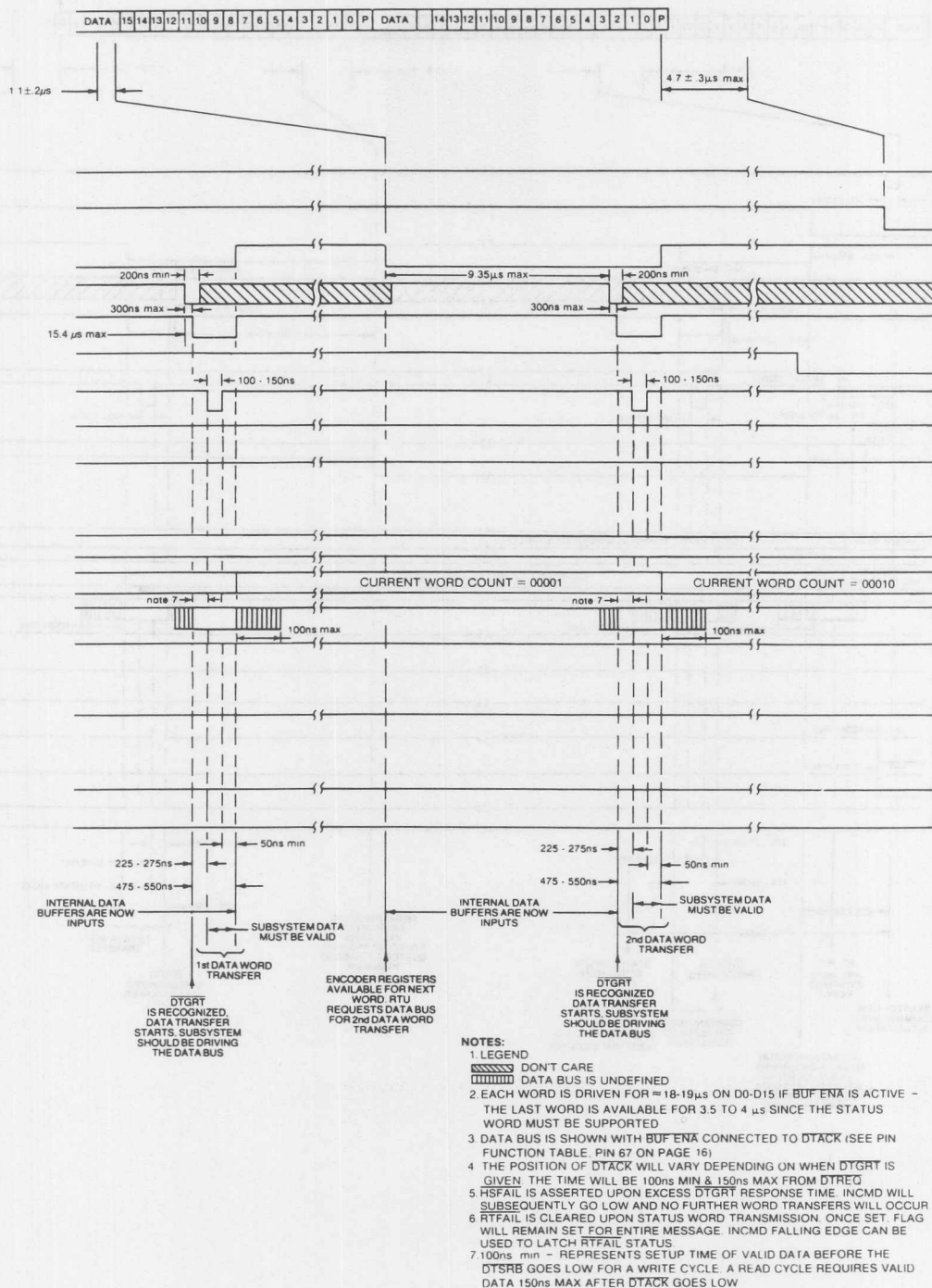
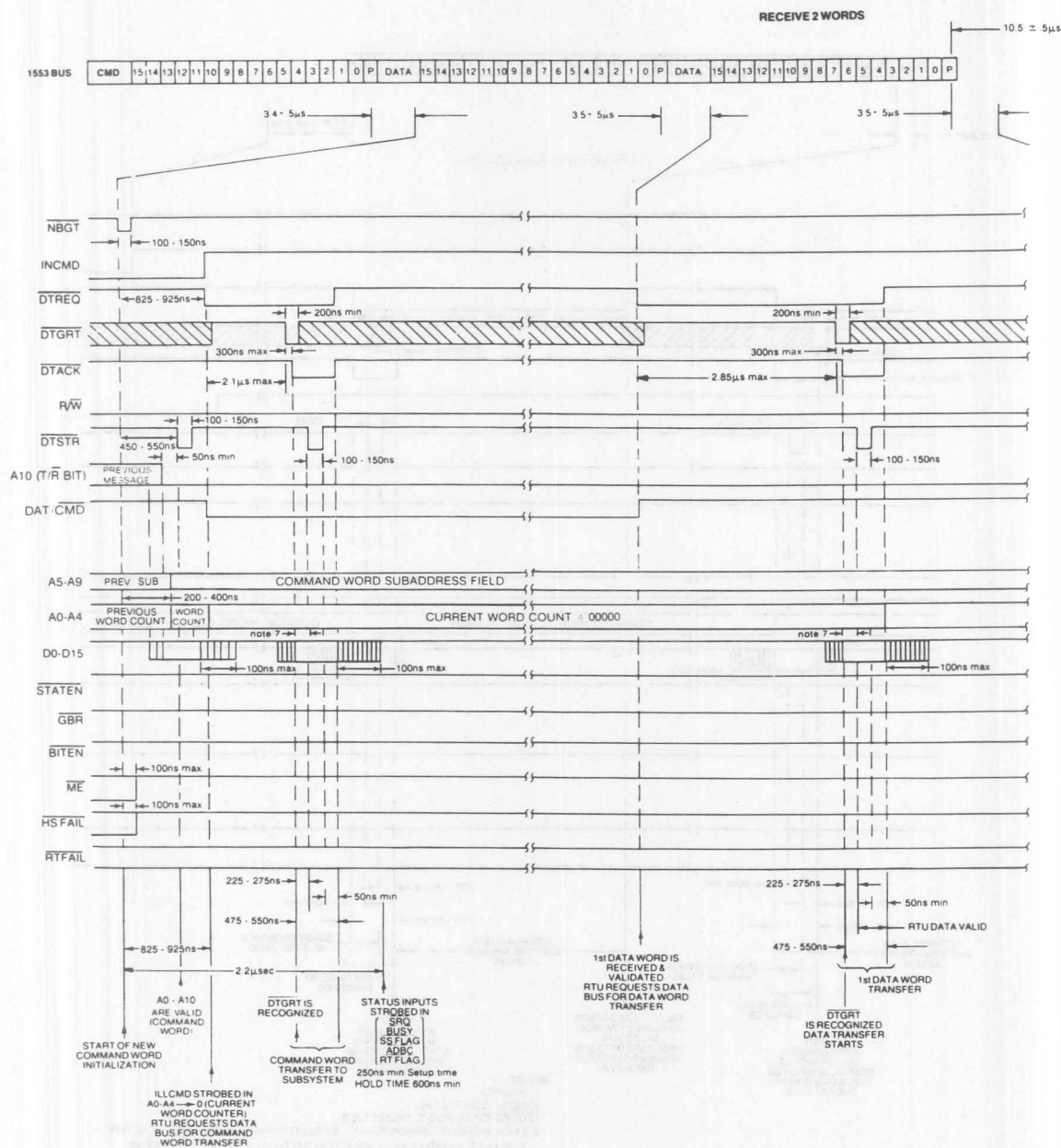
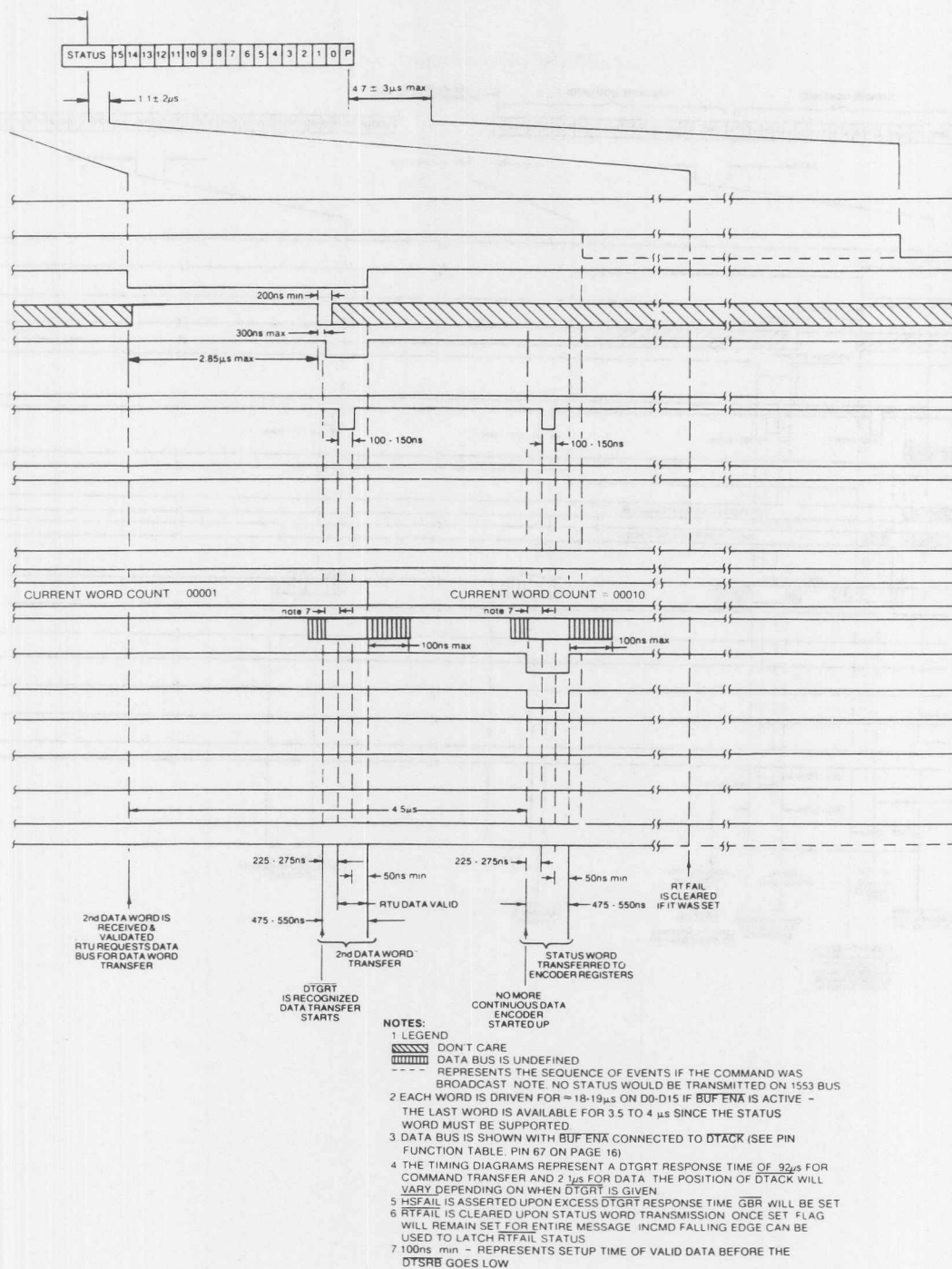


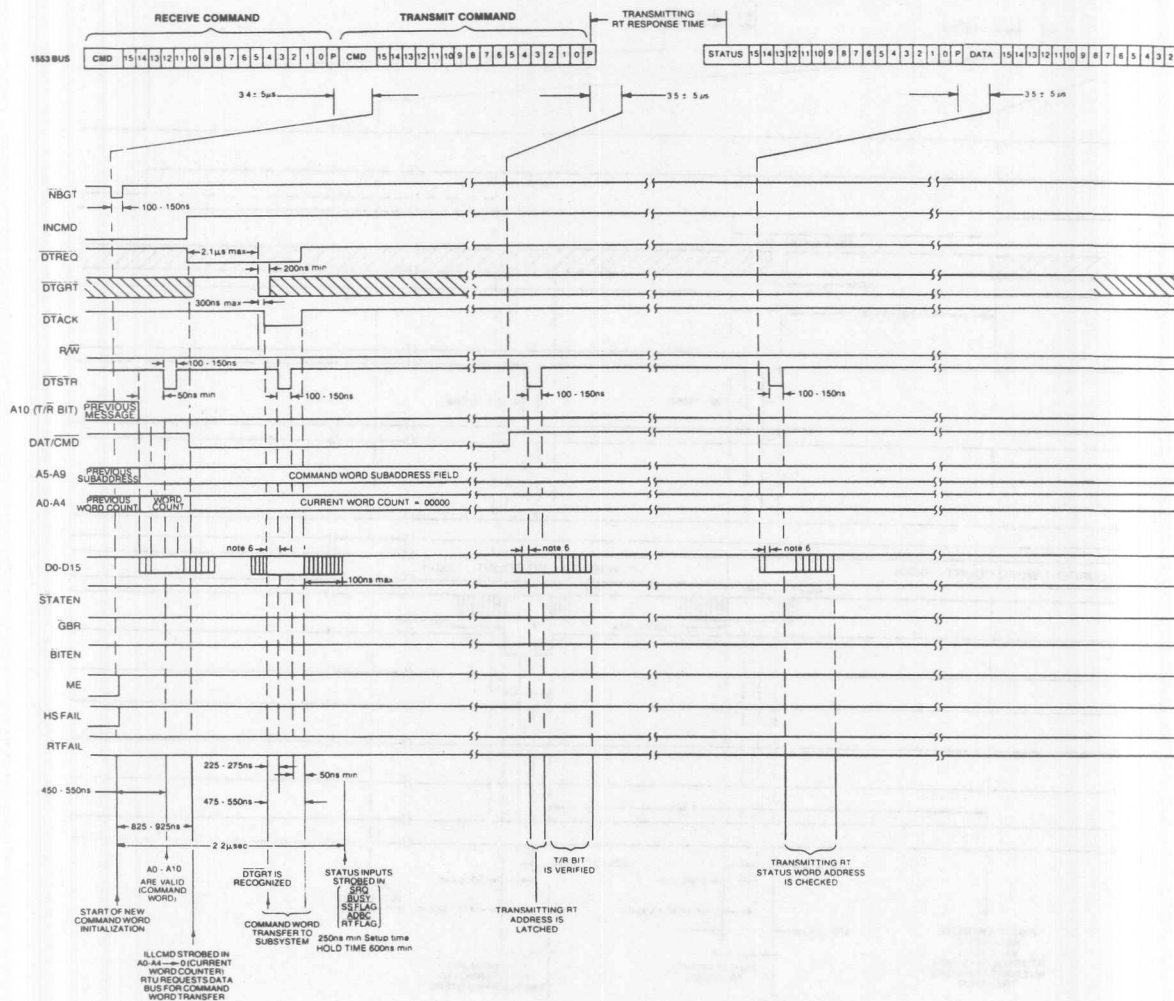
FIGURE 3. TRANSMIT TIMING DIAGRAM

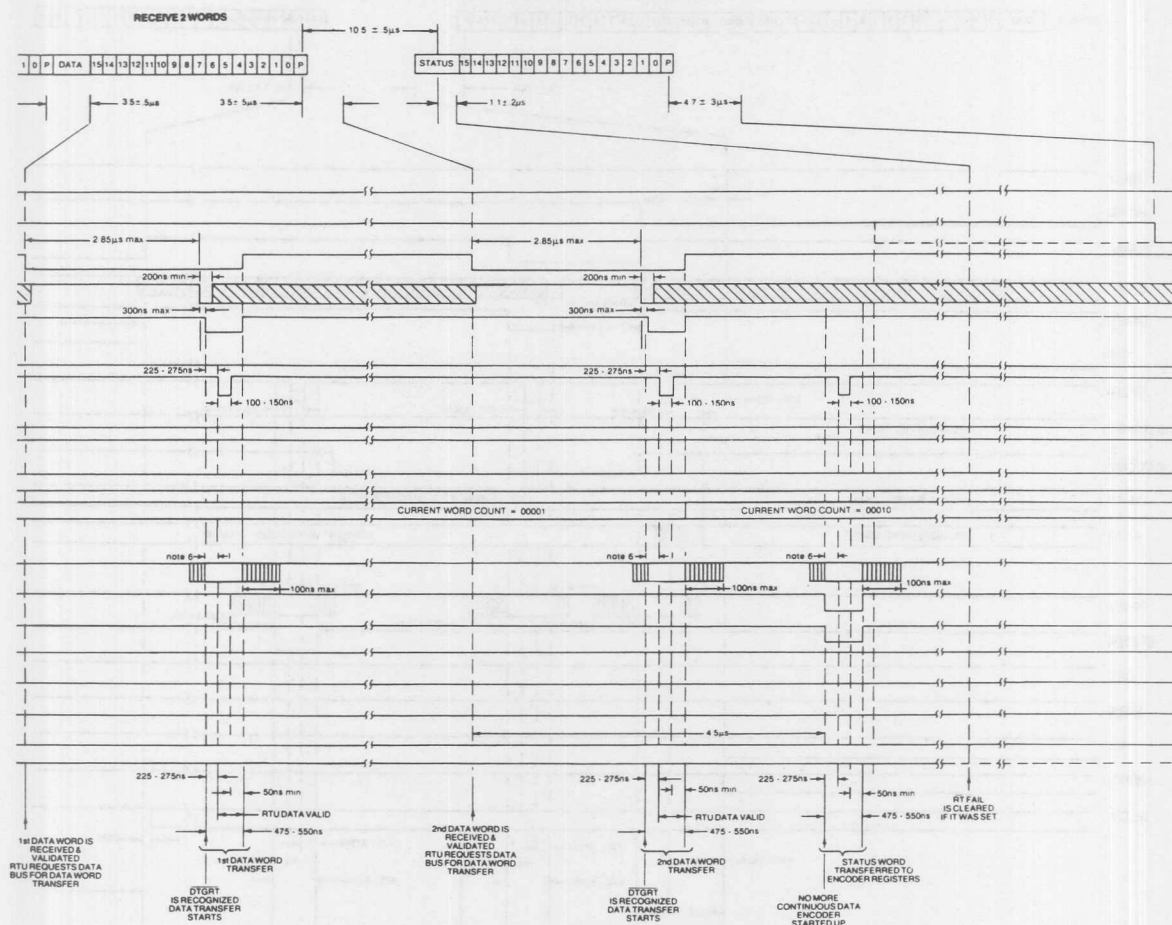






**FIGURE 4. RECEIVE TIMING DIAGRAM**

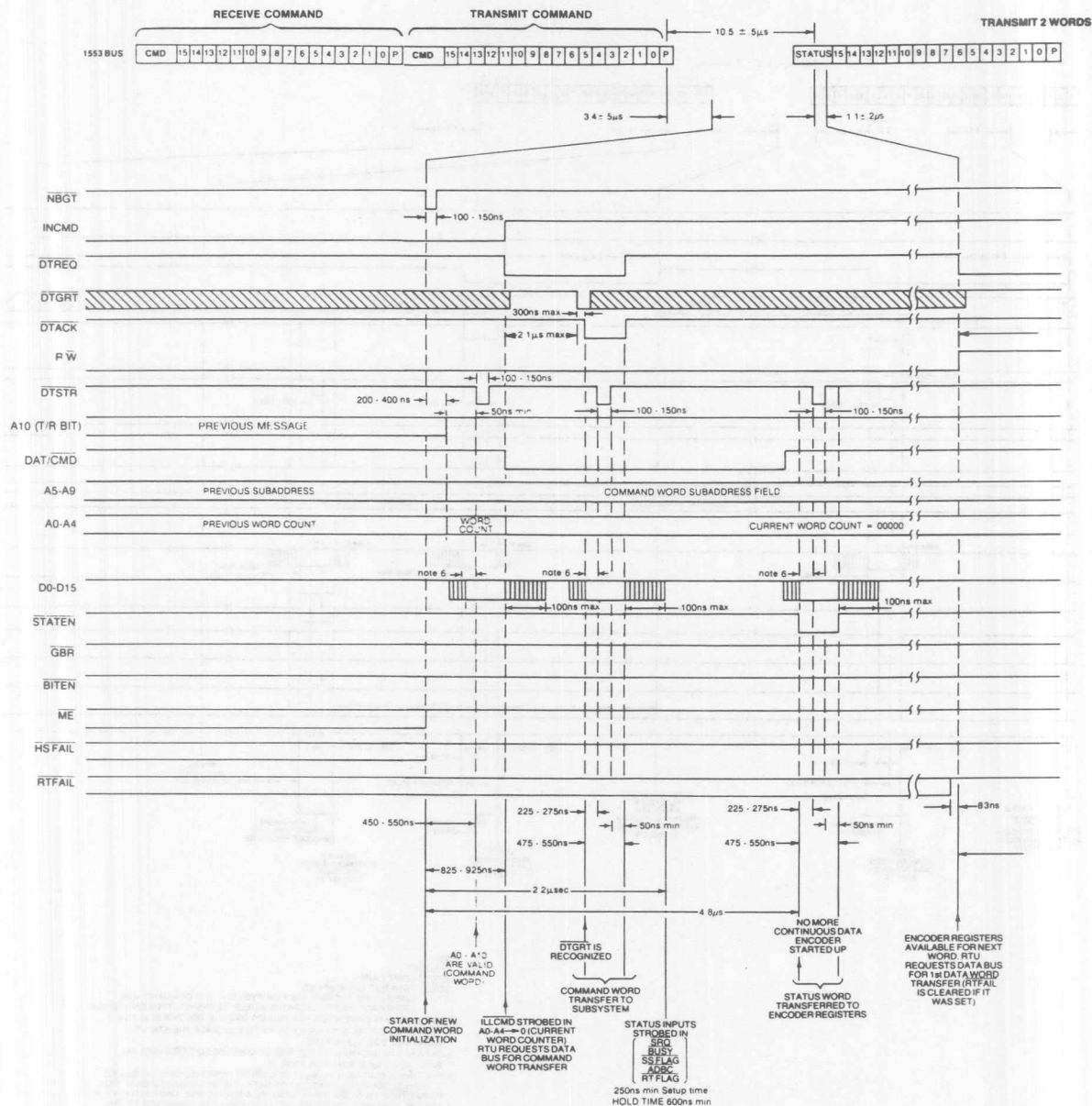




- NOTES:**
- LEGEND
    - DON'T CARE
    - DATA BUS IS UNDEFINED
    - REPRESENTS THE SEQUENCE OF EVENTS IF THE COMMAND WAS BROADCAST. NOTE: NO STATUS WOULD BE TRANSMITTED ON 1553 BUS
  - EACH WORD IS DRIVEN FOR 18-19 μs ON 00-015 IF BUF ENK IS ACTIVE - THE LAST WORD IS AVAILABLE FOR 3.5 TO 4 μs SINCE THE STATUS WORD MUST BE SUPPORTED
  - DATA BUS IS SHOWN WITH BUF ENK CONNECTED TO DTACK (SEE PIN FUNCTION TABLE, PIN 67 ON PAGE 16)
  - THE TIMING DIAGRAMS REPRESENT A DTGRY RESPONSE TIME OF 92 μs FOR COMMAND TRANSFER AND 2 μs FOR DATA. THE MAXIMUM RESPONSE TIME FROM DTRED TO DTGRY TO GUARANTEE A SUCCESSFUL TRANSFER IS 1 μs FOR THE COMMAND TRANSFER AND 2.3 μs FOR DATA TRANSFERS TO THE SUBSYSTEM. THE POSITION OF DTACK WILL VARY DEPENDING ON WHEN DTGRY IS GIVEN
  - RT FAIL IS CLEARED UPON STATUS WORD TRANSMISSION. ONCE SET, FLAG WILL REMAIN SET FOR ENTIRE MESSAGE. IN CMD FALLING EDGE CAN BE USED TO LATCH RT FAIL STATUS
  - 100ns min - REPRESENTS SETUP TIME OF VALID DATA BEFORE THE DTSRB GOES LOW

FIGURE 5. RT TO RT (RECEIVE) TIMING DIAGRAM

# BUS-65142 AND BUS-65144



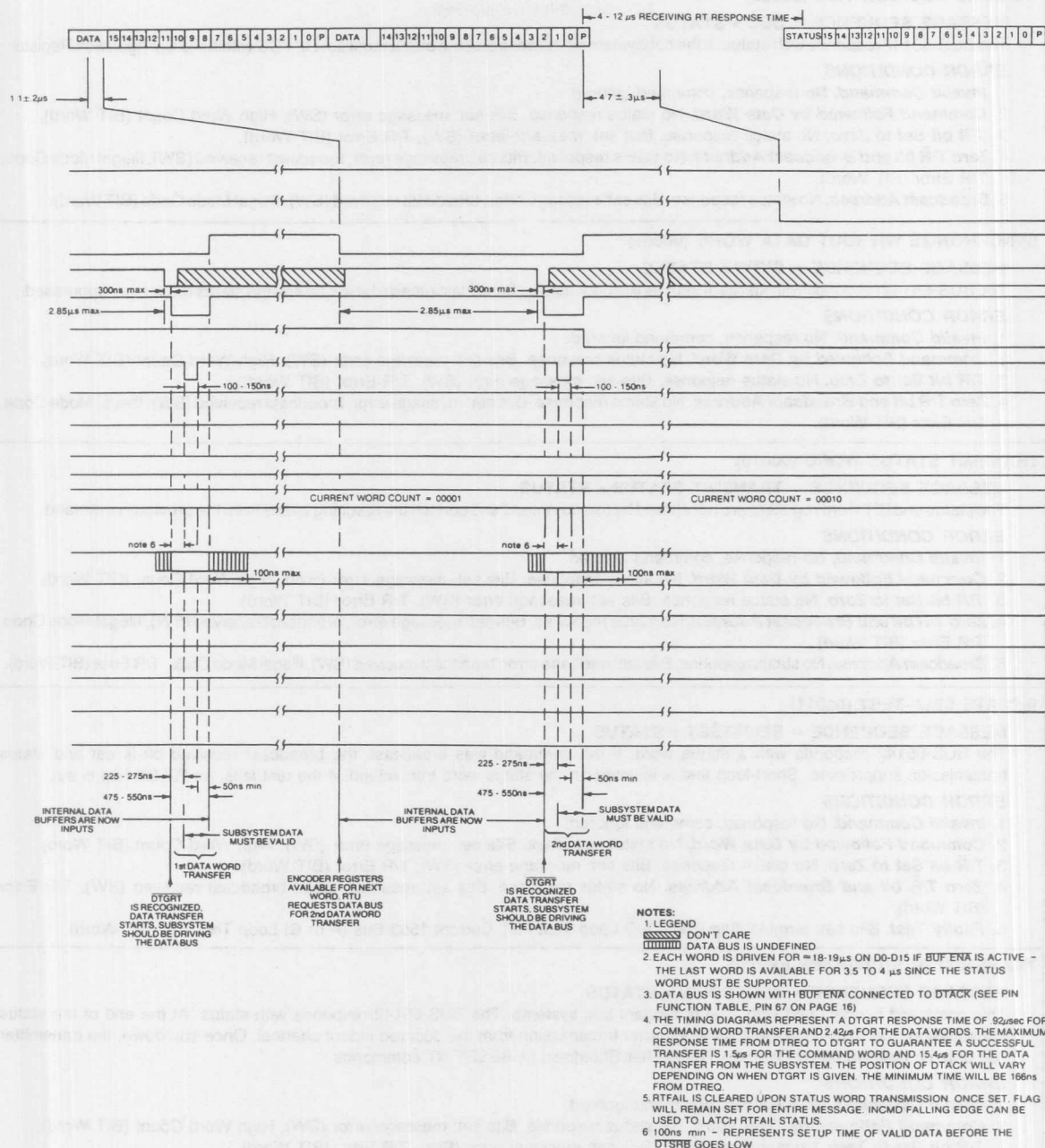


FIGURE 6. RT TO RT (TRANSMIT) TIMING DIAGRAM



TABLE 2. MODE CODES

**DYNAMIC BUS CONTROL (00000)****MESSAGE SEQUENCE = DBC \* STATUS**

The BUS-65142 responds with status. If the subsystem wants control of the bus, it must set DBACC within the Configuration Register.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

**SYNCHRONIZE WITHOUT DATA WORD (00001)****MESSAGE SEQUENCE = SYNC \* STATUS**

The BUS-65142 responds with status. If sent as a broadcast, the broadcast receive bit will be set and status response suppressed.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

**TRANSMIT STATUS WORD (00010)****MESSAGE SEQUENCE = TRANSMIT STATUS \* STATUS**

The status and BIT word registers are not altered by this command and contain the resulting status from the previous command.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

**INITIATE SELF-TEST (00011)****MESSAGE SEQUENCE = SELF-TEST \* STATUS**

The BUS-65142 responds with a status word. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Short-loop test is initiated on the status word transmitted. If the test fails, an RT fail flag is set.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).
5. **Faulty Test.** Bits set: terminal flag (SW), A/B Loop Test Fail, Current 1553 Bus (A or B) Loop Test Fail (BIT Word).

**TRANSMITTER SHUTDOWN (00100)****MESSAGE SEQUENCE = SHUTDOWN \* STATUS**

This command is only used with dual redundant bus systems. The BUS-65142 responds with status. At the end of the status transmission, the BUS-65142 inhibits any further transmission from the dual redundant channel. Once shutdown, the transmitter can only be reactivated by Override Transmitter Shutdown or RESET RT commands.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

\* = Status response time

TABLE 2. MODE CODES (CONTINUED)

## VERRIDE TRANSMITTER SHUTDOWN (00101)

### MESSAGE SEQUENCE = OVERRIDE SHUTDOWN \* STATUS

This command is only used with dual redundant bus systems. The BUS-65142 responds with status. At the end of the status transmission, the BUS-65142 re-enables the transmitter of the redundant bus. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

## INHIBIT TERMINAL FLAG BIT (00110)

### MESSAGE SEQUENCE = INHIBIT TERMINAL FLAG \* STATUS

The BUS-65142 responds with status and inhibits further internal or external setting of the terminal flag bit in the status register. Once the terminal flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT command. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

## VERRIDE INHIBIT TERMINAL FLAG BIT (00111)

### MESSAGE SEQUENCE = OVERRIDE INHIBIT TERMINAL FLAG \* STATUS

The RTU responds with status and reactivates the terminal flag bit in the status register. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

## RESET REMOTE TERMINAL (01000)

### MESSAGE SEQUENCE = RESET REMOTE TERMINAL \* STATUS

The BUS-65142 responds with status and internally resets. Transmitter shutdown, mode commands, BIT Word, and inhibit terminal flag commands will be reset. If the command was broadcast, the broadcast received bit is set and the status word is suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

## RESERVED MODE CODES (01001-01111)

### MESSAGE SEQUENCE = RESERVED MODE CODES \* STATUS

The BUS-65142 responds with clear status and no data. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), Illegal Mode Code (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

\* = Status response time

TABLE 2. MODE CODES (CONTINUED)

## TRANSMIT VECTOR WORD (10000)

**MESSAGE SEQUENCE = TRANSMIT VECTOR WORD \* STATUS VECTOR WORD**

The BUS-65142 transmits a status word followed by a vector word.

### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, (BIT Word).

## SYNCHRONIZE WITH DATA WORD (10001)

**MESSAGE SEQUENCE = SYNCHRONIZE DATA WORD \* STATUS**

The data word received following the command word is transferred to the RAM. The status word is then transmitted. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), Low Word Count (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), T/R Error, High Word Count (BIT Word).
5. **Command T/R bit Set to Zero and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), High Word Count, T/R Error (BIT Word).

## TRANSMIT LAST COMMAND (10010)

**MESSAGE SEQUENCE = TRANSMIT LAST COMMAND \* STATUS LAST COMMAND**

The status and BIT word registers are not altered by this command. The SW contains the status from the previous command. The data word transmitted contains the previous valid command (providing it was not another TRANSMIT LAST COMMAND).

### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

## TRANSMIT BIT WORD (10011)

**MESSAGE SEQUENCE = TRANSMIT BIT WORD \* STATUS BIT WORD**

The BUS-65142 responds with status followed by the BIT word. The BIT word is not altered by this command; however, the next SW will reflect errors in this transmission.

### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bit set: message error (SW).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

\* = Status response time

PIN FUNCTION TABLE		
PIN	FUNCTION	DESCRIPTION
1	A9	Latched output of the most significant bit (MSB) in the subaddress field of the command word.
2	A7	Latched output of the third most significant bit in the subaddress field of the command word.
3	A5	Latched output of the least significant bit (LSB) in the subaddress field of the command word.
4	DB1	Bi-directional parallel data bus Bit 1
5	DB3	Bi-directional parallel data bus Bit 3
6	DB5	Bi-directional parallel data bus Bit 5
7	DB7	Bi-directional parallel data bus Bit 7
8	DB9	Bi-directional parallel data bus Bit 9
9	DB11	Bi-directional parallel data bus Bit 11
10	DB13	Bi-directional parallel data bus Bit 13
11	DB15	Bi-directional parallel data bus Bit 15 (MSB)
12	BRO ENA	Broadcast enable – when HIGH, this input allows recognition of an RT address of all ones in the command word as a broadcast message. When LOW, it prevents response to RT address 31 unless it was the assigned terminal address.
13	ADDRE	Input of the MSB of the assigned terminal address.
14	ADDRC	Input of the 3rd MSB of the assigned terminal address.
15	ADDRA	Input of the LSB of the assigned terminal address.
16	RTADERR	Output signal used to inform subsystem of an address parity error. If LOW, indicates parity error and the RT will not respond to any command address to a single terminal. It will respond to broadcast commands if BRO ENA is HIGH.
17	TXDATA B	LOW output to the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
18	NC	
19	GND B	Power supply return connection for the B channel transceiver.
20	RXDATA B	Input from the HIGH side of the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
21	A3	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 2nd MSB of the current word counter.
22	A1	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd LSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter.

PIN FUNCTION TABLE		
PIN	FUNCTION	DESCRIPTION
23	DTGRT	Data transfer grant – active LOW input signal from the subsystem that informs the RT, when DTREQ is asserted, to start the transfer. Once transfer is started, DTGRT can be removed.
24	INCMD	In Command – HIGH level output signal used to inform the subsystem that the RT is presently servicing a command.
25	HSFAIL	Handshake Fail – output signal that goes LOW and stays LOW whenever the subsystem fails to supply DTGRT in time to do a successful transfer. Cleared by the next NBGT.
26	DTSTR	A LOW level output pulse (166ns) present in the middle of every data word transfer over the parallel data bus. Used to latch or strobe the data into memory, FIFOs, registers, etc. Recommend using the rising edge to clock data in.
27	(DAT/CMD)	Address line output that is LOW whenever the command word is being transferred to the subsystem over the parallel data bus, and is HIGH whenever data words are being transferred.
28	RTFAIL	Remote Terminal Failure — latched active LOW output signal to the subsystem to flag detection of a remote terminal continuous self-test failure. Also set if The Watchdog Timeout circuit is activated. Cleared by the start of the next message transmission (status word) and set if problem is again detected.
29	DTREQ	Data Transfer Request – active LOW output signal to the subsystem indicating that the RT has data for or needs data from the subsystem and requests a data transfer over the parallel data bus. Will stay LOW until transfer is completed or transfer timeout has occurred.
30	ADBC	Accept Dynamic Bus Control – active LOW input signal from subsystem used to set the Dynamic Bus Control Acceptance bit in the status register if the command word was a valid, legal mode command for dynamic bus control.
31	TEST 2	Factory test point output – DO NOT USE. (see note 1)*
32	A10 (T/R)	Latched output of the T/R bit in the command word.
33	ILLCMD	Illegal Command – Active LOW input signal from the subsystem, strobed in on the rising edge of INCMD. Used to define the command word as illegal and to set the message error bit in the status register.
34	SRQ	Subsystem Service Request – Input from the subsystem used to control the Service Request Bit in the status register. If LOW when the status word is updated, the Service Request Bit will be set; if HIGH, it will be cleared.
35	BITEN	Built-in-Test Word Enable – LOW level output pulse (.5μsec), present when the built-in-test word is enabled on the parallel data bus.
36	RXDATA A	Input from the LOW side of the primary side of the coupling transformer that connects to the A Channel of the 1553 Bus.
37	+5VA	+5 volt input power supply connection for the A channel transceiver.

\* See notes at end of table.



PIN	FUNCTION	DESCRIPTION
38	-15VA	-15 volt input power supply connection for the A Channel transceiver.
39	TXDATA A	HIGH output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
40	NBGT	New Bus Grant - LOW level output pulse (166 ns) used to indicate the start of a new protocol sequence in response to the command word just received.
41	A8	Latched output of the 2nd MSB in the subaddress field of the command word.
42	A6	Latched output of the 2nd LSB in the subaddress field of the command word.
43	DB0	Bidirectional parallel data bus Bit 0 (LSB)
44	DB2	Bidirectional parallel data bus Bit 2
45	DB4	Bidirectional parallel data bus Bit 4
46	DB6	Bidirectional parallel data bus Bit 6
47	DB8	Bidirectional parallel data bus Bit 8
48	DB10	Bidirectional parallel data bus Bit 10
49	DB12	Bidirectional parallel data bus Bit 12
50	DB14	Bidirectional parallel data bus Bit 14
51	+5V	+5 Volt input power supply connection for RTU digital logic section.
52	GND	Power supply return for RTU digital logic section.
53	ADDRD	Input of the 2nd MSB of the assigned terminal address.
54	ADDRB	Input of the 2nd LSB of the assigned terminal address.
55	ADDRP	Input of Address Parity Bit. The combination of assigned terminal address and ADDR P must be odd parity for the RT to work.
56	TXDATA B	HIGH, output to the primary side of the coupling transformer that connects to the B Channel of the 1553 Bus.
57	-15VB	-15 volt input power supply connection for the B channel transceiver.
58	+5VB	+5 volt input power supply connection for the B channel transceiver.
59	RXDATA B	Input from the LOW side of the primary side of the primary side of the coupling transformer that connects to the B Channel of the 1553 Bus.
60	A2	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the 3rd MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 3rd MSB of the current word counter.
61	A0	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the LSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the LSB of the current word counter.
62	DTACK	Data Transfer Acknowledge - active LOW output signal during data transfers to or from the subsystem indicating the RTU has received the DTGRT in response to DTREQ and is presently doing the transfer. Can be connected directly to pin 67 (BUF ENA) for control of tri-state data buffers; and to tri-state address buffer control lines, if they are used.

PIN	FUNCTION	DESCRIPTION
63	A4	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the MSB of the current word counter.
64	R/W	Read/Write - output signal that controls the direction of the internal data bus buffers. Normally, the signal is LOW and the buffers drive the data bus. When data is needed from the subsystem, it goes HIGH to turn the buffers around and the RT now appears as an input. The signal is HIGH only when DTREQ is active (LOW).
65	GBR	Good Block Received - LOW level output pulse (.5μsec) used to flag the subsystem that a valid, legal, non-mode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem.
66	16MHz IN	16MHz Clock Input - input for the master clock used to run RTU circuits.
67	BUF ENA	Buffer Enable - input used to enable or tri-state the internal data bus buffers when they are driving the bus. When LOW, the data bus buffers are enabled. Could be connected to DTACK (Pin 62) if RT is sharing the same data bus as the subsystem. (see note 2)*
68	RESET	Input resets entire RT when LOW.
69	RTFLAG	Remote Terminal Flag - input signal used to control the terminal flag bit in the status register. If LOW when the status word is updated, the terminal flag bit would be set; if HIGH, it would be cleared. Normally connected to RTFAIL (Pin 28).
70	TEST 1	Watchdog Timeout test point - DO NOT USE. (see note 3)* (input)
71	BUSY	Subsystem Busy - input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set; if HIGH, it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands, data will still be transferred to subsystem.
72	SSFLAG	Subsystem Flag - input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated, the subsystem flag will be set; if HIGH, it will be cleared.
73	ME	Message Error - output signal that goes LOW and stays LOW whenever there is a format or word error with the received message over the 1553 Data Bus. Cleared by the next NBGT.
74	RXDATA A	Input from the HIGH side of the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
75	GNDA	Power supply return connection for the A Channel transceiver.
76	NC	
77	TXDATA A	LOW output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
78	STATEN	Status Word Enable - LOW level active output signal present when the status word is enabled on the parallel data bus.

\* See notes at end of table.



TABLE 2. MODE CODES (CONTINUED)

## SELECTED TRANSMITTER SHUTDOWN (10100)

### MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA \* STATUS

The data word received is transferred to the subsystem and status is transmitted. No other action is taken by the BUS-65142. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Intended for use with RTs with more than one dual redundant channel.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count (BIT Word).

## OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101)

### MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA \* STATUS

The data word received after the command word is transferred to the subsystem. No other action is taken by the BUS-65142. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count, T/R Error (BIT Word).

## RESERVED MODE CODES (10110 - 11111)

### MESSAGE SEQUENCE = RESERVED MODE CODE (T/R = 1) \* STATUS

### RESERVED MODE CODE (T/R = 0) \* STATUS

#### If Valid (T/R = 0)

The BUS-65142 responds with status. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.

#### If Invalid (T/R = 1)

Respond with status and 1 data word.

#### ERROR CONDITIONS (T/R = 1)

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

#### ERROR CONDITIONS (T/R = 0)

1. **Invalid Command.** No response, command ignored.
2. **Command not Followed by Contiguous Data Word.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

## UNDEFINED MODE CODES

(T/R = 0, MODE CODE 00000 TO 01111)

No Response, set message error bit.

\* = Status response time

## PIN FUNCTION TABLE NOTES:

### 1: PIN 31 — FACTORY TEST POINT OUTPUT

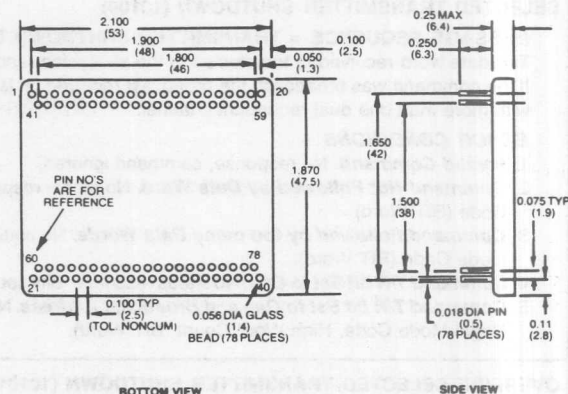
This pin provides the output of the BUS-65142 BIT Comparison output. It indicates the loop test results for every word transmitted by the BUS-65142. A test can be performed by actioning the RTU to transmit while the test fixture opens the receiver lines to force an error condition. A logic 1 (high) indicates the loop test passed. Normally this pin is left open.

### 2: PIN 67 — $\overline{\text{BUF ENA}}$

This pin is typically tied to  $\overline{\text{DTACK}}$ , causing the BUS-65142 to drive the shared data bus only while  $\overline{\text{DTACK}}$  is active. If desired,  $\overline{\text{BUF ENA}}$  can be grounded. The data will remain latched on the data bus pins for 18 $\mu\text{s}$  from  $\overline{\text{DTSRB}}$  and 3.5 $\mu\text{s}$  for the last word of a message as the device's status word or BIT word is transferred to the BC ( $\overline{\text{STATEN}}$  or  $\overline{\text{BITEN}}$  low). Once the STATUS or BIT Word transfer is complete, the data bus will automatically again contain the last data word. The BUS-65142 will automatically switch the direction of the internal buffers during a transmit operation.

### 3: PIN 70 — TEST 1

This test allows the user to force the active channel to transmit indefinitely, in order to test the built-in Watchdog Timer feature of the BUS-65142. When this pin is grounded and the active channel is stimulated with a valid transmit command, the BUS-65142 will respond with a status word and contiguous data (last data word loaded or STATUS WORD if none is loaded) until the built-in time-out occurs. Normally this pin is left open or an optional pull-up can be used.



Note: Dimensions are in inches (millimeters).

FIGURE 7. BUS-65142 MECHANICAL OUTLINE (DDIP)

## ORDERING INFORMATION

### BUS-65142-883

#### Reliability Grade:

883B = Fully compliant with MIL-STD-883.

B = Screened to MIL-STD-883 but without QCI testing.

#### Power Supply Option & Packaging

2 = -15VDC DDIP

3 = -12VDC DDIP

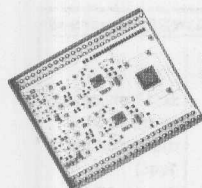
4 = -15VDC Flatpack

5 = -12VDC Flatpack

#### Mating Data Bus Transformers:

for BUS-65142 use DDC BUS-25679

for BUS-65143 use DDC BUS-29854



## MIL-STD-1553A/B & McAIR UNIVERSAL MULTI-PROTOCOL REMOTE TERMINAL

### DESCRIPTION

The BUS-65149 is the world's first dual redundant universal MIL-STD-1553 Remote Terminal (RT) hybrid. The BUS-65149 features a universal sinusoidal transceiver and pin selectable options providing for support of MIL-STD-1553A; MIL-STD-1553B; McAIR A3818, A5232, and A5690; the various G.D. F16 protocols; and GRUMMAN SPG151A.

The BUS-65149 provides all of the functions required to interface between a MIL-STD-1553 dual redundant serial data bus and a subsystem parallel three-state data bus. A pair of BUS-27765 transformers are required to interface between the BUS-65149 and the 1553 bus. See Figure 1, block diagram.

The BUS-65149 is compatible with all microprocessors, supporting both DMA and shared RAM interfaces. In addition, the 8/16-bit direct memory interface (DMA) handshake

and three-state parallel data and address buses facilitate the interface to simple systems without a microprocessor.

The BUS-65149 implements all MIL-STD-1553 message formats. Complete error detection capability is provided. This includes sync, encoding, parity, bit and word count, undefined commands, and RT-to-RT transfer errors.

The BUS-65149 features the capability for implementing all dual redundant MIL-STD-1553B mode codes. In addition, any command may (optionally) be illegalized through the use of an external PROM, PAL, or RAM device.

The device is available screened to MIL-STD-883B in a MIL-STD-1772 certified facility and operates over the full military temperature range of -55°C to +125°C.

### FEATURES

- **SUPPORTS:**
  - MIL-STD-1553A/B
  - McAIR A3818, A5232, AND A5690
  - GENERAL DYNAMICS 16PP303 (F16)
  - GRUMMAN SPG151A
- **DUAL UNIVERSAL TRANSCEIVER SATISFIES McAIR AND 1553A/B**
- **SUPPORTS 1553A/B MODE CODES**
- **INTERNAL AND EXTERNAL OPTIONS FOR STATUS AND BIT WORDS**
- **INTERFACE FLEXIBILITY**
  - SIMPLE SYSTEMS
  - 8/16-BIT DMA OR SHARED RAM
- **SUPPORTS COMMAND ILLEGALIZATION**
- **CONTINUOUS ON-LINE, BUILT-IN-TEST**
- **12 OR 16 MHZ CLOCK OPERATION**

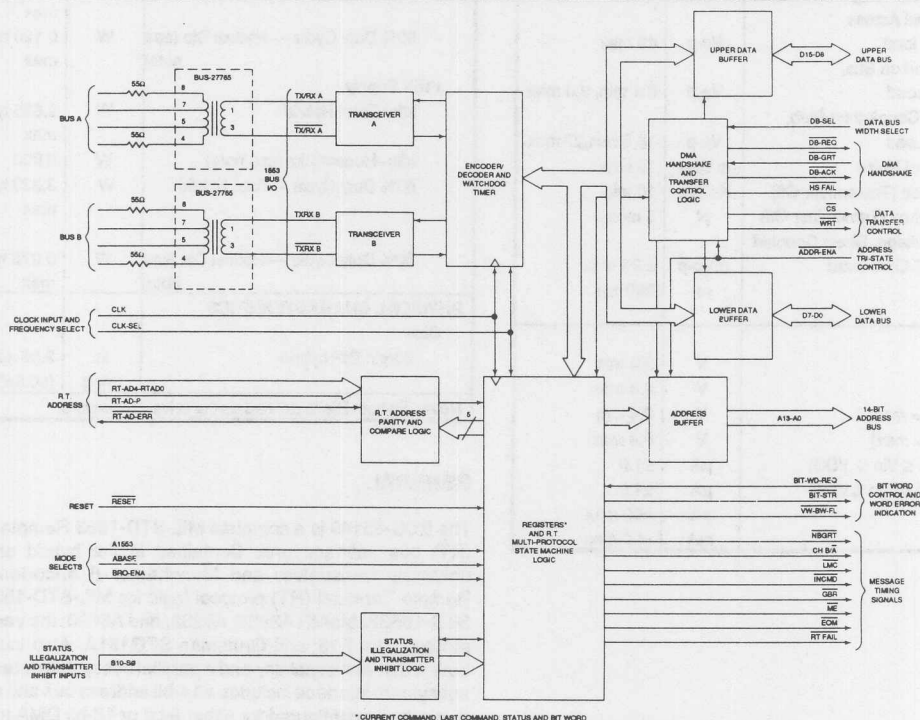


FIGURE 1. BUS-65149 BLOCK DIAGRAM

TABLE 1. BUS-65149 PRELIMINARY SPECIFICATIONS

Specifications are applicable over the full range of temperature and power supply voltage.

PARAMETER	UNITS	VALUE
<b>ABSOLUTE MAXIMUM RATINGS</b>		
Supply Voltage		-0.5 to 7.0
+5	V	
+12/15	V	-0.3 to +18.0
-12/-15	V	+0.3 to -18.0
Input Voltage Range	V	-.5 to V <sub>dd</sub> + .5
Operating Temperature Range	°C	-55 to 125
Storage Temperature Range	°C	-65 to 150
<b>RECOMMENDED OPERATING CONDITIONS</b>		
Supply Voltage +5	V	4.5 to 5.5
+12/15	V	+11.4 to +15.75
-12/15	V	-11.4 to -15.75
Input Voltage Range	V	0 to V <sub>dd</sub>
<b>RECEIVER</b>		
Differential Input Voltage	V <sub>p-p</sub>	40 max
Differential Input Resistance (DC to 1.0 MHz)	K Ohm	7 min
Differential Input Capacitance	pf	5 max
Threshold Voltage (Direct Coupled)	V <sub>p-p</sub>	0.5min, 1.0 max
CMRR (through BUS-27765 transformer)	dB	45 min
<b>TRANSMITTER</b>		
Differential Output Voltage		
Direct Coupled Across 140 Ohm load	V <sub>p-p</sub>	40 max
Direct Coupled on Bus, 35 Ohm Load	V <sub>p-p</sub>	6.4 min, 9.0 max
Transformer Coupled on Stub, 70 Ohm Load	V <sub>p-p</sub>	18.5 min, 27 max
Differential Output Noise	mV <sub>p-p</sub>	10 max
Output Resistance (Transmitter Off)	K Ohm	10 min
Output Capacitance (Transmitter Off)	pf	5 max
Output Offset Voltage, Direct Coupled, Across 35 Ohm Load	mV <sub>p-p</sub>	± 90 max
Rise/Fall Time	ns	280 typ
<b>LOGIC</b>		
V(IH)	V	2.0 min
V(IL)	V	0.8 max
V(OH) (IOH = max)	V	2.4 min
V(OL) (IOL = max)	V	0.4 max
I(IH) (GND ≤ V <sub>in</sub> ≤ V <sub>DD</sub> )	μA	±1.0
I(IL) (GND ≤ V <sub>in</sub> ≤ V <sub>DD</sub> )	μA	±1.0
I(OH)	μA	400 max
I(OL)	mA	-4.0 max

TABLE 1. BUS-65149 PRELIMINARY SPECIFICATIONS (continued)

<b>CLOCK INPUT</b>		
<b>16 MHz</b>		
Frequency Tolerance	%	±0.1%max (long term); ±0.01% max (short term 1sec)
Duty Cycle	%	33 min, 67 max
<b>12 MHz</b>		
Frequency Tolerance	%	± 0.1%max (long term); ±0.01% (short term, 1 sec)
Duty Cycle	%	40 min, 60 max
<b>CURRENT DRAIN</b>		
+5V	mA	75 typ, 115 max
+12/15V		
Idle	mA	48 typ, 60 max
50% Duty Cycle	mA	106 typ, 134 max
-12/15V		
Idle	mA	102 typ, 130 max
50% Duty Cycle	mA	164 typ, 195 max
<b>POWER DISSIPATION</b>		
±12V Supply		
Idle—Total Hybrid	W	2.175 typ, 2.865 max
Idle—Hottest Die (see note)	W	0.000
50% Duty Cycle —Total Hybrid	W	2.890 typ, 3.820 max
50% Duty Cycle — Hottest Die (see note)	W	0.120 typ, 0.145 max
±15V Supply		
Idle—Total Hybrid	W	2.635 typ, 3.285 max
Idle—Hottest Die (see note)	W	0.000
50% Duty Cycle —Total Hybrid	W	3.220 typ, 4.085 max
50% Duty Cycle — Hottest Die (see note)	W	0.075 typ, 0.090 max
<b>PHYSICAL CHARACTERISTICS</b>		
Size		
90-pin DIP hybrid	in (mm)	2.38 x 2.0 x 0.25 (60.3x50.8x6.34)

Note: Hottest Die is defined as the driver transistors.

## GENERAL

The BUS-65149 is a complete MIL-STD-1553 Remote Terminal (RT) bus interface unit. Contained in the hybrid are a dual universal transceiver and Manchester II encoder/decoder, Remote Terminal (RT) protocol logic for MIL-STD-1553A, MIL-STD-1553B; McAIR A3838, A5232, and A5690; the various G.D. protocols for F16; and Grumman SPG151A. Also included are built in self-test capability and a parallel subsystem interface. The subsystem interface includes a 14-bit address bus and a data bus that may be configured for either 8-bit or 16-bit DMA transfers.



The analog front end of the BUS-65149 consists of a dual redundant universal transceiver. The universal transceiver may be powered from a supply voltage in the range of  $\pm 12$  to  $\pm 15$  volts. The dual receiver is based on DDC's latest low-power bipolar transceiver monolithic. The dual transmitter provides sinusoidal complimentary voltage source outputs. The transmitters' nominal rise/fall time of 280 ns satisfies various McAIR standards as well as MIL-STD-1553A/B.

The BUS-65149 meets the MIL-STD-1553A response time requirement of 2 to 5  $\mu$ s of dead time on the 1553 bus.

The BUS-65149 implements all MIL-STD-1553 message formats, including all 13 of the 1553B dual redundant mode codes. Any subset of the possible 1553 commands (broadcast, T/R bit, subaddress, word count/mode code) may be optionally illegalized by means of an external PROM, PAL or RAM device. An extensive amount of message validation is performed for each message received. Each word received is validated for correct sync type and sync encoding, Manchester II encoding, parity and bit count. All messages are verified to contain a legal, defined Command Word and correct word count. If the BUS-65149 is the receiving RT in an RT-to-RT transfer, it verifies that the T/R bit of the transmit Command Word is a one and that the transmitting RT responds in time and contains the correct RT address in its Status Word.

The BUS-65149 offers a great deal of flexibility to fulfill a wide variety of 1553A/B/McAIR applications. It may be programmed for either of three operating modes: 1553B, BASIC 1553A or MODIFIED 1553A. There are programmable options regarding mode codes, command illegalizing, Status and BIT Word handling, and error responses.

One pin programmable option allows the BUS-65149 to respond to a receive command containing a Manchester II or parity error in the data portion of a message. In the BASIC 1553A mode, the BUS-65149 will respond with its Status Word with the Message Error bit set. If this option is not selected, (MODIFIED 1553A mode), the BUS-65149 will suppress its Status response to all data errors. For the 1553B mode, the Message Error bit in the internal Status Register will be set. In this instance, the BUS-65149 will respond with Status/Message Error if the next message is a Transmit Status or Transmit Last Command mode code.

The 65149 may be operated from either a 12MHz or 16 MHz clock input. In the 12 MHz mode, the decoder samples incoming data with both edges of the clock input. This, in effect, provides for 24 MHz decoder sampling. The benefits of the faster sampling rate include a wider tolerance for zero-crossing distortion and improved bit error rate performance.

The BUS-65149 includes a hardwired R.T. address input. This includes 5 address lines, an address parity input and an address parity error output.

The BUS-65149 RT Status Word may be pin-programmed to conform to either MIL-STD-1553B or to 1553A or other protocols. In the "1553A" mode, all 11 Status Word bits are under direct control of the external subsystem.

The 65149 supports command illegalization. In the 1553B mode, commands may be illegalized by asserting S10 low at the time of the falling edge of INCMD or by asserting S09 low when the Status Word inputs are sampled, approximately 3  $\mu$ s later; this latter time is approximately 5  $\mu$ s after the mid-parity bit crossing of the received Command Word.

Command words may be illegalized as a function of broadcast, T/R bit, subaddress, and/or word count/mode code.

For the 1553A modes, only the "S10" illegalizing option is available. For 1553A, bit 10 (bit 15 is MSB) of the Status Word will be set if S10 is sampled low. However, for a transmit command in 1553A mode, data words will be transmitted, regardless of the status of bit 10 of the Status Word.

Two options are provided for the RT BIT Word. In one option, an internal BIT Word register is updated at the end of each message. The contents of this register may be read by the subsystem whenever the BUS-65149 is not servicing a 1553 command. The BUS-65149 is servicing a command from the time of the beginning of the pulse output NBGRT until the rising edge of INCMD at the end of the message cycle. With the second BIT Word option, the subsystem provides the BIT WORD to the BUS-65149 by means of its 8/16-bit data bus.

The BUS-65149 performs a loopback self-test at the end of each message processed. The last word transmitted is received, validated and compared to the last transmitted word. If the loopback test fails, the user has the option of having the Terminal Flag Status Word bit set in response to the next non-broadcast message.

The use or non-use of broadcast is pin programmable. If broadcast is disabled, R.T. address 31 may be used as a discrete terminal address.

The BUS-65149 provides a number of real time output signals. These various signals provide indications of message start, bus channel, message in progress, message completion, valid received message, message error, handshake fail, and looptest fail.

The BUS-65149 may be used in a wide variety of interface configurations. The 65149 has an 8/16-bit tri-state data bus and an address/control bus that may be pin programmed for either two-state or three-state operation. The three-state mode allows the BUS-65149 to be connected directly to the host processor's data, address and control buses in a DMA configuration. The BUS-65149 includes standard DMA handshake signals (Request, Grant, and Acknowledge) as well as transfer control outputs (CS and WRT). The DMA interface may operate in either a 16-bit or 8-bit mode, supporting both word-wide and byte-wide transfers.

The DMA interface also allows the 65149 to be interfaced directly to a simple system that doesn't have a microprocessor. This provides a low cost 1553 interface for A/D and D/A converters, switch closures and actuators.



The BUS-65149 may also be used in a shared RAM interface configuration. By means of tri-state buffers and a very small amount of "glue" logic, the 65149 will store Command Words and access Data Words to/from dedicated "mailbox" areas in a shared RAM for each broadcast /  $\overline{T/R}$  bit / subaddress / mode code.

If a more elaborate shared RAM interface is needed, the BUS-65149 may be interfaced to a BUS-66312 memory management unit. If a BUS-66312 is used, the address bus of the BUS-65149 is not used for accessing the system RAM (although the address outputs may still be used for command illegalizing). The BUS-66312 provides an RT Lookup Table, allowing the mapping of the various  $\overline{T/R}$ /subaddresses to user programmable areas in the BUS-66312's 64K X 16 shared RAM address space. The BUS-66312 also provides a stack area of RAM. The stack provides a chronology of all messages processed, storing a Block Status Word (message channel, completion and validity information), an optional Time Tag Word and the received Command Word for each message processed. The BUS-66312 also provides maskable interrupts to the host processor for end-of-message and/or message error conditions.

## OPERATING MODES

To provide the flexibility for operation in a wide variety of 1553-based platforms, the BUS-65149 may be operated in one of three modes: 1553B, BASIC 1553A, and MODIFIED 1553A.

The BUS-65149 mode of operation is selected by means of the two input pins A1553 and ABASE, as follows:

A1553	ABASE	BUS-65149 MODE
0	X	1553B
1	0	Modified 1553A
1	1	Basic 1553A

The three modes of operation are summarized in the Table 2:

TABLE 2. BUS-65149 MODES OF OPERATION			
PARAMETER	1553B	MODIFIED 1553A	BASIC 1553A
Response Time	4 to 7 $\mu$ s, per MIL-STD-1553B.	2 to 5 $\mu$ s, per MIL-STD-1553A.	
Mode Codes	Subaddresses 0 and 31 are both reserved for mode code operation. All dual redundant 1553B mode codes are implemented.	Only subaddress 0 is treated as a mode code subaddress. Subaddress 31 is treated as a standard non-mode code subaddress. For a Command Word to Subaddress 0 followed by no Data Words, the BUS-65149 will respond with Status, per S10-S0. For a Command Word to Subaddress 0 followed by one or more Data Words, the BUS-65149 will not respond. Dynamic Bus Control is the only mode code defined for MIL-STD-1553A.	

TABLE 2. BUS-65149 MODES OF OPERATION(continued)			
PARAMETER	1553B	MODIFIED 1553A	BASIC 1553A
Status Word and Command Illegalizing	Message Error and Broadcast Command Received implemented per MIL-STD-1553B. In addition, Message Error may be set by an external illegalizing device by means of S10 or S09. Service Request (S08), Busy (S03), SSFlag (S02), Accept Dynamic Bus Control (S01) and Terminal Flag (S00) are under subsystem control. The Terminal Flag bit may be inhibited and reactivated by mode code commands, per MIL-STD-1553B.	Status Word bits are under direct subsystem control by means of S10-S0. Command illegalization (setting Message Error bit) controlled by S10 input from subsystem.	Same as for MODIFIED 1553A mode, except that Message Error bit will also be set in response to a receive message containing a Manchester II or Parity error in any Data Word or a low bit count error in the last Data Word.
Definition of extra word at end of message	Valid sync field plus two valid data bits.		Valid sync field.
Response to receive messages with errors in Data Word portion of message	Per MIL-STD-1553B: no response. Message Error bit is set internally; ME bit will be set in response to next message if the next message is a Transmit Status Word or Transmit Last Command mode code.	No response	For Sync Error, high or low word count, gap error or high/low bit count in Data Word other than last Data Word: no response.  For Manchester II encoding or parity errors in any Data Word or low bit count in the last Data Word: Respond with Status with the Message Error bit set.
BUSY bit.	BUSY bit set in Status Word. No data is transmitted by the BUS-65149.	Bit 3 of Status Word under direct subsystem control. Has no effect on received or transmitted data.	

## ADDRESS MAPPING

The memory allocation scheme for the BUS-65149 14-bit address bus is defined as follows:

A13:	BROADCAST/OWN ADDRESS
A12:	TRANSMIT/RECEIVE
A11-A7:	SUBADDRESS 4-0
A6:	DATA/COMMAND
A5-A1:	WORD COUNT/CURRENT WORD COUNT
A0:	UPPER/LOWER BYTE (8-BIT MODE ONLY)

The method of address mapping implemented by the BUS-65149 provides for a "mailbox" allocation scheme for the storage of Command and Data Words. The address outputs A13 through A1 map directly into 8K words (16K bytes) of processor address space. A0 is used for upper/lower byte selection in the 8-bit DMA mode. The same address map is applicable for both the DMA and shared RAM (without the BUS-66312) interface configurations.

The BUS-65149's addressing scheme maps messages in terms of broadcast/own address, transmit/receive, subaddress, and mode code. A 64-word message block is allocated for each T/R-subaddress. The received Command Word for all non-mode code messages is stored at relative word location zero (0) within each message block. For mode code messages, the received Command Word is offset from location zero (0) within the message block for subaddress 0 or 31. The value of the address offset is equal to the mode code field of the respective Command Word (0 to 31).

The data words to be transmitted or received are accessed from (to) relative locations 32 through 63 within the message block. Data Words for the Synchronize with Data and Transmit Vector Word mode codes are mapped to subaddresses 0 and 31. The Data Word transmitted in response to a Transmit Last Command mode code is accessed from an internal register. The Data Word transmitted in response to a Transmit BIT Word command is accessed either from an internal register or from the subsystem via the 8/16-bit data bus, as determined by pin programming.

## DMA INTERFACE

An 8/16-bit data bus, a 14-bit address bus, and six control signals are provided to facilitate communication with the parallel subsystem. The control signals include the standard DMA handshake signals DT\_REQ, DT\_GRT, DT\_ACK as well as the transfer control outputs CS and WRT. HS\_FAIL provides an indication to the subsystem of a handshake failure condition.

Data is transferred between the subsystem and the BUS-65149 via a DMA handshake, initiated by the BUS-65149. A READ operation is defined to be the transfer of data from the subsystem to the BUS-65149. Conversely, a WRITE operation transfers data from the BUS-65149 to the subsystem. If the BUS-65149 is in

16-bit mode, data is transferred as a single 16-bit word. In 8-bit mode, data is transferred in a pair of byte transfers within the same DMA handshake cycle. The upper byte is transferred first with A0=1, followed by the lower byte with A0=0.

If the BUS-65149 asserts DT\_REQ and the subsystem does not respond with DT\_GRT in time for the BUS-65149 to complete the word transfer, the HS\_FAIL output will be asserted low to inform the subsystem of the handshake failure.

## DMA READ Operation

Whenever the BUS-65149 needs to read a word from the subsystem, it asserts the signal DT\_REQ low. If the subsystem asserts DT\_GRT in time, the BUS-65149 will then assert A13 through A1 (and A0 for the 8-bit mode), WRT high, along with DT\_ACK and CS low to enable data from the subsystem.

After the transfer of each Data Word has been completed, address bus outputs A5 through A1 are incremented. This provides the option of connecting the BUS-65149 address lines directly to the host processor's address bus to access the subsystem RAM, if desired.

## DMA WRITE Operation

Whenever the BUS-65149 wishes to transfer data to the subsystem, it initiates a DMA WRITE cycle. The BUS-65149 asserts DT\_REQ. The subsystem must respond with DT\_GRT.

If DT\_GRT was received in time, the BUS-65149 will then assert DT\_ACK. The BUS-65149 will then assert A13 through A1 (and A0 in 8-bit mode) and WR low, followed by CS low. The subsystem may then use the rising edge of CS to latch the data. Similar to the DMA read operation, the address outputs A5 through A1 are incremented after the completion of a DMA WRITE operation.

## MESSAGE PROCESSING OPERATION

Following the receipt and transfer of a valid Command Word, the BUS-65149 will attempt to (1) transfer received 1553 data to the subsystem, (2) read data from the subsystem for transmission on the 1553 bus, (3) transmit status information to 1553, or (4) set status conditions. The BUS-65149 responds to all non-broadcast messages with a 1553 Status Word.

## RT Address

RT Address (RT\_AD 4-0, (RT\_AD4 = MSB)) and RT Address Parity (RT\_AD\_P) should be programmed to a unique RT address. The BUS-65149 will not respond to any MIL-STD-1553 commands or transfer received data from any non-broadcast messages if an odd parity sum is not presented by RT\_AD4-0 and RT\_AD\_P. An address parity error will be indicated by a low output on the RT\_AD\_ERR pin.

## Command Illegalization

The BUS-65149 provides two options for command illegalization. With one method, the input signal S10 (Illegal Command Input 1) is sampled on the falling edge of INCMD. With the other method, S09 (Illegal Command Input 2) is sampled approximately 5  $\mu$ s following the mid-parity bit zero crossing of the received Command Word. In the 1553B mode, both S10 and S09 may be used for command illegalizing. In the 1553A modes, only S10 may be used for illegalizing. This supports command illegalization for 1553B applications using either a two-state or three-state address bus as well as for 1553A applications using a two-state address bus. Command illegalization is implemented by means of an external PROM, PLD, or RAM device. The BUS-65149 allows any subset of the possible 1553 commands to be illegalized as a function of broadcast, T/R bit, subaddress, word count and/or mode code.

## Transmit Command (RT-to-BC Transfer).

If the BUS-65149 receives a valid Transmit Command Word that the subsystem determines is legal (inputs S10 and S09 high) and the subsystem is not BUSY (input S03 is high), the BUS-65149 will initiate a transmit data response. Following transmission of the Status Word, this entails a handshake/read cycle for each Data Word, with the total number of Data Words to be transmitted specified by the Word Count field of the Command Word. A low on S10 (1553A and 1553B modes) or S09 (1553B mode) will result in the Message Error bit being set. In the 1553B mode, no Data Words will be transmitted following transmission of the Status Word to an illegalized transmit command. For the 1553B mode, a low on the BUSY (S03) input will set the BUSY bit in the Status Word; in this instance, only the Status Word will be transmitted, with no Data Words. In the 1553A modes, a low on BUSY has no effect on Data Word transmission.

## Receive Command (BC-to-RT Transfer).

A DMA handshake will be initiated for each word received over the 1553 data bus. If successful, the respective handshake will be followed by a corresponding write cycle. A handshake timeout will not terminate transfer attempts for the remaining Data Words, error flagging or Status Word transmission. After the reception of a valid receive Command Word followed by the correct number of valid Data Words and assuming that all words are successfully transferred to the subsystem, a negative pulse will be asserted on the output Good Block Received (GBR).

## RT-to-RT Transfers (Transmitting/Receiving).

An RT-RT transfer will appear to both RTs as a standard transmit or receive command except that: (1) transmission of the Data Words will not be contiguous with that of the receive Command Word and (2) upon detection of a command sync field following the receive command, the receiving RT will recognize an RT-RT transfer and store the RT address field from the transmit Command Word for comparison with the RT address field of the Status Word from the transmitting RT. If the T/R bit of the "transmit" command is a one, the transmitting RT does not respond in time

or an address mismatch is detected in the transmitting RT's Status Word, the receiving RT will classify the condition as a "Command error" and will not respond.

If the BUS-65149 is the transmitting RT for an RT-to-RT transfer, it will respond with Status and Data Words as in an RT-to-BC transmit command.

## RT Status, Error Handling and Message Timing Signals

Message transfer errors are indicated by means of the HS\_FAIL, ME, and RT\_FAIL error indication outputs. Additional error detection and indication mechanisms include updating of the internal Status and BIT Word registers.

The BUS-65149 provides a number of timing signals during the processing of 1553 messages. NBGR provides a negative pulse output following receipt of a 1553 Command Word. INCMD is asserted low when a new command is received. At the end of a message (either valid or invalid), INCMD transitions high while EOM pulses low. Following the last data word of a valid receive message, GBR is asserted low. CH. B/A provides an indication of what bus a message is being processed on. ME is asserted as a low output following any detected error in a received message.

## Loopback Test.

The last word to be transmitted in a given message transfer (Status Word, BIT Word, last Command Word or Data Word) is stored in an internal register. When this word is transmitted on the 1553 bus, it is "looped back" through the active receiver and decoder and a loopback test is performed. The loopback test is considered to have failed if the received version of the word is either invalid and/or does not match the transmitted version of the word. If the loopback test fails, the RT\_FAIL output will be asserted low. If RT\_FAIL is connected to S00 (TERMINAL FLAG), the Terminal Flag bit will be set in the Status response to the next non-broadcast message.

## Use of Status Word.

In the 1553B mode, the Broadcast Command Received bit is formulated internally. The Message Error Status bit will be set if the current command is a Transmit Status Word or Transmit Last Command mode command and if there was an error in the data portion of a previous receive message. In the BASIC 1553A mode, Message Error will be set in response to a receive message containing either a Manchester II or parity error in any Data Word or a low bit count error in the last Data Word of a receive message. Message Error will also be set if either ILLEGAL COMMAND 1 (1553A and 1553B modes) or ILLEGAL COMMAND 2 (1553B mode only) has been sampled low for the current message. In the 1553B mode, Service Request, Busy, Subsystem Flag, Dynamic Bus Control and Remote Terminal Flag will be sampled from their respective Status (S10-S0) input pins.

In the 1553A modes, all 11 Status Word Bits are sampled from the S10 through S0 inputs.

## BIT Word.

The BUS-65149 provides two options for implementing the Transmit BIT Word mode command. In one option, a 16-bit BIT word is formulated in an internal register. Under this option, the subsystem may read the contents of the internal BIT register at any time. In the second option, the BIT Word may be read from the subsystem as part of the response to a Transmit BIT Word Mode Command.

## INTERNAL BUILT-IN-TEST (BIT) WORD DEFINITION

- D15: Transmitter Timeout
- D14: Loop Test Failure - B Bus
- D13: Loop Test Failure - A Bus
- D12: Handshake Failure
- D11: Bus B Transmitter Shutdown
- D10: Bus A Transmitter Shutdown
- D09: Terminal Flag Inhibited
- D08: CH. B / CH. A
- D07: High Word Count
- D06: Low Word Count
- D05: Incorrect Sync Type Received
- D04: Invalid Word Received - Manchester or Parity Error
- D03: RT-RT Transfer Response Error (no gap, data sync, address mismatch)
- D02: RT-RT Transfer No Response Timeout
- D01: RT-RT Transfer - T/R Error on Second Command or My Valid Address
- D00: Command Word Contents Error

## Mode Codes

Nine of the 13 available, dual redundant mode codes are handled by the BUS-65149 without user intervention. Of the four remaining codes, Dynamic Bus Control and Synchronize (without data) entail subsystem notification. The remaining two mode codes, Transmit Vector Word and Synchronize (with data) involve data transfer with the subsystem. For the Transmit BIT Word mode code, the user may either make use of the internally formulated BIT Word or transmit a BIT Word provided by the subsystem. Table 3 provides a summary of the 1553B mode codes supported by the BUS-65149. Note that Dynamic Bus Control is the only mode code defined for MIL-STD-1553A.

TABLE 3. MIL-STD-1553A/B MODE CODES

T/R BIT	MODE CODE	FUNCTION	DATA WORD	BROADCAST ALLOWED
1	00000	Dynamic Bus Control (Note 1)	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	Yes
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag	No	Yes
1	00111	Override Inhibit Terminal Flag	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001-11111	RESERVED	No	TBD
1	10000	Transmit Vector Word	From Subsystem	No
0	10001	Synchronize with Data	To Subsystem	Yes
1	10010	Transmit Last Command	From Internal Register	No
0	10100	Selected Transmitter Shutdown (Note 2)	To Subsystem	Yes
0	10101	Override Selected Transmitter Shutdown (Note 2)	To Subsystem	Yes
1	10011	Transmit BIT Word	(Note 3)	No
0	10110-11111	RESERVED	Yes	TBD
1	10110-11111	RESERVED	Yes	TBD

### Notes:

- Dynamic Bus Control is the only mode code defined for MIL-STD-1553A.
- Terminal responds with Clear Status but no action is taken.
- If the input S06 is high, the transmitted BIT Word is read from an internal register. If S06 is low, the BIT Word is read from the subsystem.



**RESET:** MASTER RESET - ACTIVE LOW INPUT SIGNAL USED TO RESET THE ENTIRE CIRCUIT.

**CLOCK:** 12 OR 16 MHz MASTER SYSTEM CLOCK INPUT. PRIMARILY USED TO RUN THE 1553 DECODER SECTIONS. INTERNALLY DIVIDED DOWN TO GENERATE AN 6 OR 8 MHz PROTOCOL CLOCK.

**A1553:** 1553A / 1553B SELECT - INPUT SIGNAL USED TO SELECT WHICH MODE OF OPERATION THE TERMINAL WILL PERFORM. FOR 1553 A OPERATION, SET TO LOGIC "1". FOR 1553 B OPERATION, SET TO LOGIC "0".

**ABASE:** 1553 A BASE MODE SELECT - INPUT SIGNAL, ACTIVE ONLY IN THE 1553 A MODE OF OPERATION THAT IF SET HIGH, WILL ALLOW THE RT TO RESPOND TO AN INVALID MESSAGE (THAT IS, A MESSAGE WITH THE ONLY TYPE OF ERRORS BEING INVALID DATA WORDS DUE TO PARITY OR MANCHESTER ERRORS) WITH A STATUS WORD THAT HAS THE MESSAGE ERROR BIT SET. IF SET LOW, ANY ERROR ON THE 1553 BUS WILL SUPPRESS THE STATUS WORD RESPONSE.

**BRO\_ENA:** BROADCAST ENABLE - INPUT SIGNAL WHICH WHEN HIGH ENABLES THE RECOGNITION OF TERMINAL ADDRESS 31 AS A BROADCAST MESSAGE. WHEN LOW, IT RECOGNIZES TERMINAL ADDRESS 31 AS A UNIQUE REMOTE TERMINAL ADDRESS.

**RT\_AD\_4, (MSB) THROUGH RT\_AD\_0 (LSB):** REMOTE TERMINAL ADDRESS [4:0] - INPUT SIGNALS, USUALLY HARDWIRED, USED TO DEFINE THE UNIQUE 1553 REMOTE TERMINAL ADDRESS (FROM 0 TO 31) THAT THE REMOTE TERMINAL WILL RESPOND TO. RT\_AD\_4 IS THE MSB, RT\_AD\_0 IS THE LSB.

**RT\_AD\_P:** REMOTE TERMINAL ADDRESS PARITY LINE - INPUT SIGNAL OF THE ADDRESS PARITY BIT. THE COMBINATION OF RT\_AD\_[0:4] , AND RT\_AD\_P MUST BE ODD TO ENABLE RECOGNITION OF THE TERMINAL'S ADDRESS.

**NBGR:** NEW BUS GRANT - LOW LEVEL OUTPUT PULSE (2 CLOCK CYCLES WIDE), THAT IS USED TO INDICATE THE START OF A NEW PROTOCOL SEQUENCE IN RESPONSE TO THE COMMAND WORD JUST RECEIVED FROM THE 1553 BUS.

**CHB/CHA:** CHANNEL A / CHANNEL B - OUTPUT SIGNAL USED TO INDICATE WHICH CHANNEL IS PRESENTLY BEING USED OR MONITORED. LOGIC "0" INDICATES CHANNEL A, LOGIC "1" INDICATES CHANNEL B. THIS LINE IS UPDATED ON THE RISING EDGE OF NBGR AND RESETS TO CHANNEL A.

**INCMD:** IN COMMAND - ACTIVE LOW LEVEL OUTPUT SIGNAL USED TO INFORM THE SUBSYSTEM THAT THE BUS-65149 IS PRESENTLY SERVING A COMMAND THAT CAME IN ON THE 1553 BUS.

**GBR:** GOOD BLOCK RECEIVED - LOW LEVEL OUTPUT PULSE (2 CLOCK CYCLES WIDE) THAT IS USED TO FLAG THE SUBSYSTEM THAT A VALID, LEGAL, NON-MODE RECEIVE COMMAND WITH THE CORRECT NUMBER OF DATA WORDS HAS BEEN RECEIVED WITHOUT A MESSAGE ERROR AND SUCCESSFULLY TRANSFERRED TO THE SUBSYSTEM.

**EOM:** END OF MESSAGE - LOW LEVEL OUTPUT PULSE (2 CLOCK CYCLES WIDE), PRESENT AT THE END OF INCMD, USED TO FLAG THE SUBSYSTEM THAT ALL COMMAND WORD SERVICING HAS BEEN COMPLETED. MASKED IF A SUPERCEEDING COMMAND INTERRUPTS THE PRESENT COMMAND WORD SERVICING.

**LMC:** LATCHED MODE CODE - OUTPUT SIGNAL THAT INFORMS THE SUBSYSTEM THAT THE PRESENT COMMAND WORD IS A MODE COMMAND. IT IS UPDATED AFTER NBGR BUT BEFORE INCMD GOES ACTIVE. A LOGIC "0" INDICATES A MODE CODE. CLEARED (LOGIC "1") BY RESET.

**TEST\_MODE:** FACTORY TEST INPUT - CONNECT TO LOGIC "1"

**T\_A\_STR:** FACTORY TEST INPUT - CONNECT TO LOGIC "1"

**T\_D\_STR:** FACTORY TEST INPUT - CONNECT TO LOGIC "1"



## INPUT/OUTPUT PIN DESCRIPTIONS (continued)

### REMOTE TERMINAL STATUS WORD CONTROL SIGNALS

**S10-S00:** STATUS BIT INPUTS - THESE INPUT SIGNALS CONTROL THE SETTING OF THE BITS IN THE STATUS WORD RESPONSE. THEY ARE ACTIVE LOW. IN 1553A OPERATION MODE, THESE SIGNALS CONTROL THE STATUS WORD BITS DIRECTLY. THAT IS, IF A LOGIC "0" IS APPLIED TO ANY BIT WHEN THE STATUS WORD IS UPDATED, (DURING STATEN\_L PULSE), THE CORRESPONDING BIT WILL BE SET. IF A LOGIC "1" IS APPLIED, THE BIT WILL BE CLEARED. S00 IS THE LSB. THE ONLY EXCEPTION TO THIS IS THE S10 BIT IN THE STATUS WORD IN THE BASIC 1553A MODE. IN THIS CASE, THE PROTOCOL WILL AUTOMATICALLY SET THE BIT IF AN INVALID DATA WORD WAS RECEIVED. IN 1553B OPERATION MODE, THE BITS ARE DEFINED AS FOLLOWS:

**S10; ILLEGAL COMMAND INPUT 1:** INPUT STROBED IN ON THE FALLING EDGE OF INCMD USED TO ILLEGALIZE ANY COMMAND AND SET THE MESSAGE ERROR BIT OF THE STATUS WORD. ACTIVE LOW.

**NOTE:** IF A COMMAND IS DEFINED AS ILLEGAL, THE MESSAGE ERROR BIT (D10) IN THE STATUS WORD TRANSMITTED WOULD BE SET. ALSO, IF THE THE COMMAND WAS A TRANSMIT COMMAND, ONLY THE STATUS WORD WOULD BE TRANSMITTED. HAS NO EFFECT ON RECEIVE COMMANDS OTHER THEN INHIBITING GBR. ON MODE COMMANDS, THE ACTUAL MODE FUNCTION WOULD NOT BE PERFORMED.

**S09; ILLEGAL COMMAND INPUT 2:** INPUT STROBED IN WHEN THE STATUS REGISTER IS UPDATED (APPROXIMATELY 5.0 US AFTER THE PARITY CROSSING OF THE COMMAND WORD) IN THE 1553B MODE. USED TO ILLEGALIZE COMMANDS AND SET THE MESSAGE ERROR BIT OF THE STATUS WORD. ACTIVE LOW.

**S08; SERVICE REQUEST:** INPUT SIGNAL USED TO CONTROL THE SERVICE REQUEST BIT (BIT 8) IN THE STATUS WORD. IF LOW WHEN THE STATUS REGISTER IS UPDATED, THE SERVICE REQUEST BIT WILL BE SET. IF HIGH, IT WILL BE CLEARED.

**S07; SERVICE REQUEST LATCH INPUT** - A LOW LEVEL APPLIED AT ANY TIME ON THIS INPUT WILL SET AN INTERNAL LATCH THAT WILL HOLD THE SERVICE REQUEST UNTIL IT HAS BEEN TRANSMITTED OVER THE 1553 BUS WHICH IN TURN CLEARS THE INTERNAL LATCH. THIS INTERNAL LATCH CAN ALSO BE CLEARED BY PULSING S08 OR BY A RESET OR BY SWITCHING TO 1553A MODE.

**S06; EXTERNAL BIT WORD ENABLE:** A LOW LEVEL APPLIED TO THIS INPUT SELECTS THE EXTERNAL BIT WORD OPTION. THAT IS, IF A MODE TRANSMIT BIT WORD COMMAND IS RECEIVED AND THIS INPUT IS LOW, THEN THE BUS-65149 WILL REQUEST THE BIT WORD FROM THE SUBSYSTEM THRU A DT\_REQ, DT\_GRT, AND DT\_ACK CYCLE. SEE VW\_BW\_FL FOR MORE DETAILS ON WHEN TO ENABLE THE BIT WORD ON THE BUS.

**S05; SUBSYSTEM CHANNEL B TX INHIBIT** - A LOW LEVEL ON THIS INPUT WILL BLOCK ANY TRANSMISSION ON CHANNEL B FROM BEING SENT OUT ON THE 1553 BUS PROVIDED THAT THE 1553B MODE IS SELECTED.

**NOTE:** INTERNALLY THE TRANSMISSION WILL CONTINUE. THEREFORE, IF THIS INPUT IS RETURNED TO A HIGH LEVEL DURING THE INTERNAL TRANSMISSION, THE BUS-65149 WILL START TRANSMITTING ON THE 1553 BUS.

**S04; SUBSYSTEM CHANNEL A TX INHIBIT:** A LOW LEVEL ON THIS INPUT WILL BLOCK ANY TRANSMISSION ON CHANNEL A FROM BEING SENT OUT ON THE 1553 BUS PROVIDED THAT THE 1553B MODE IS SELECTED.

**NOTE:** INTERNALLY THE TRANSMISSION WILL CONTINUE. THEREFORE, IF THIS INPUT IS RETURNED TO A HIGH LEVEL DURING THE INTERNAL TRANSMISSION, THE BUS-65149 WILL START TRANSMITTING ON THE 1553 BUS.

## INPUT/OUTPUT PIN DESCRIPTIONS (continued)

### REMOTE TERMINAL STATUS WORD CONTROL SIGNALS (continued)

**S03; BUSY:** INPUT SIGNAL USED TO CONTROL THE BUSY BIT (BIT 3) IN THE STATUS WORD. IF LOW WHEN THE STATUS REGISTER IS UPDATED, THE BUSY BIT WILL BE SET. IF HIGH, IT WILL BE CLEARED. NOTE, IF THE BUSY BIT IS SET AND THE COMMAND WAS A TRANSMIT COMMAND, ONLY THE STATUS WORD WOULD BE TRANSMITTED. HAS NO EFFECT ON RECEIVE COMMANDS.

**S02; SUBSYSTEM FLAG:** INPUT SIGNAL USED TO CONTROL THE SUBSYSTEM FLAG BIT (BIT 2) IN THE STATUS WORD. IF LOW WHEN THE STATUS REGISTER IS UPDATED, THE SUBSYSTEM FLAG BIT WILL BE SET. IF HIGH, IT WILL BE CLEARED.

**S01; ACCEPT DYNAMIC BUS CONTROL:** INPUT SIGNAL USED TO CONTROL THE DYNAMIC BUS CONTROL BIT (BIT 1) IN THE STATUS WORD. IF LOW WHEN THE STATUS REGISTER IS UPDATED, THE DYNAMIC BUS CONTROL BIT WILL BE SET IN RESPONSE TO A LEGAL VALID DYNAMIC BUS CONTROL MODE COMMAND. IF HIGH, OR A DIFFERENT COMMAND WAS RECEIVED, THE DYNAMIC BUS ACCEPTANCE BIT WILL BE CLEARED.

**S00; REMOTE TERMINAL FLAG:** INPUT SIGNAL USED TO CONTROL THE TERMINAL FLAG BIT (BIT 0) IN THE STATUS WORD. IF LOW WHEN THE STATUS REGISTER IS UPDATED, THE TERMINAL FLAG BIT WILL BE SET. IF HIGH, IT WILL BE CLEARED. NORMALLY CONNECTED TO RT\_FAIL.

### ERROR FLAG INDICATORS

**RT\_AD\_ERR:** REMOTE TERMINAL ADDRESS PARITY ERROR OUTPUT SIGNAL THAT REFLECTS THE PARITY COMBINATION OF THE RT\_AD [4:0] INPUTS AND RT\_AD\_PAR INPUT. HIGH LEVEL INDICATES ODD PARITY, LOW LEVEL INDICATES EVEN PARITY. NOTE, IF OUTPUT IS LOW, THEN THE BUS-65149 WILL NOT RECOGNIZE ANY COMMAND WORD AS AN EXPLICIT VALID ADDRESS.

**ME:** MESSAGE ERROR - ACTIVE LOW LEVEL OUTPUT SIGNAL USED TO FLAG THE SUBSYSTEM THAT THERE WAS A MESSAGE ERROR ON THE 1553 BUS COMMUNICATION. THIS LINE GOES LOW UPON DETECTING THE ERROR AND IS RESET BY THE NEXT NBGRТ OR MASTER RESET. IF THIS LINE GOES LOW, ALL FURTHER COMMAND SERVICING IS ABORTED.

**HS\_FAIL:** HANDSHAKE FAILURE - ACTIVE LOW LEVEL OUTPUT USED TO FLAG THE SUBSYSTEM THAT DT\_GRT WAS NOT RECEIVED IN RESPONSE TO DT\_REQ IN TIME TO PERFORM A DATA TRANSFER. LATCHED LOW AND CLEARED BY THE NEXT NBGRТ OR RESET.

**RT\_FAIL:** REMOTE TERMINAL FAILURE - LATCHED LOW LEVEL OUTPUT THAT GOES LOW IF A LOOP BACK FAILURE OR A TRANSMITTER SHUT-DOWN TIMEOUT HAS OCCURRED DURING A TRANSMISSION CYCLE. RESET BY THE START OF THE NEXT TRANSMISSION CYCLE (STATUS WORD) OR A LOW LEVEL ON THE RESET INPUT. NORMALLY CONNECTED TO S00 (RTFLAG INPUT) DURING 1553B OPERATION TO CONTROL THE TERMINAL FLAG IN THE STATUS REGISTER.

## INPUT/OUTPUT PIN DESCRIPTIONS (continued)

### DATA BUS TRANSFER SIGNALS

**DB\_SEL:** DATA BUS SELECT - INPUT SIGNAL USED TO SELECT THE DATA BUS STRUCTURE (8 OR 16 BIT WIDTH).

LOGIC "0" SELECTS 16 BIT BUS.

LOGIC "1" SELECTS 8 BIT BUS.

**NOTE:** FOR AN 8-BIT DATA BUS OPERATION, D15 TO D08 SHOULD BE CONNECTED TO D07 TO D00, DIRECTLY.

**ADDR\_ENA:** ADDRESS ENABLE - ACTIVE LOW LEVEL INPUT SIGNAL USED TO CONTROL THE OPERATION OF **WRT**, **CS**, AND ADDRESS BUS (A13 TO A00). IF A LOGIC "0" IS APPLIED, THE ABOVE SIGNALS ARE ALWAYS ACTIVE. IF A LOGIC "1" IS APPLIED, THESE SIGNALS ARE KEPT IN THEIR HIGH IMPEDANCE STATE EXCEPT FOR WHEN A DATA TRANSFER IS BEING PERFORMED (**DT\_ACK** = LOGIC "0").

**DT\_REQ:** DATA TRANSFER REQUEST - ACTIVE LOW LEVEL OUTPUT SIGNAL USED TO INFORM THE SUBSYSTEM THAT THE BUS-65149 NEEDS CONTROL OF THE DATA BUS TO DO A TRANSFER. STAYS LOW UNTIL **DT\_GRT** IS RECEIVED AND THE TRANSFER IS COMPLETED OR UNTIL A HANDSHAKE FAILURE TIMEOUT HAS OCCURRED.

**DT\_GRT:** DATA TRANSFER GRANT - ACTIVE LOW LEVEL INPUT SIGNAL FROM THE SUBSYSTEM THAT INFORMS THE BUS-65149, WHEN **DT\_REQ** IS ASSERTED, TO START THE TRANSFER CYCLE. ONCE THE TRANSFER IS STARTED, **DT\_GRT** CAN BE REMOVED.

**DT\_ACK:** DATA TRANSFER ACKNOWLEDGE - ACTIVE LOW LEVEL OUTPUT SIGNAL USED TO INFORM THE SUBSYSTEM THAT THE BUS-65149 HAS RECEIVED **DT\_GRT** IN RESPONSE TO **DT\_REQ** AND IS PRESENTLY DOING A DATA TRANSFER OVER THE PARALLEL DATA BUS.

**WRT:** READ / WRITE - OUTPUT SIGNAL THAT CONTROLS THE DIRECTION OF THE DATA TRANSFERS. THE DIRECTION IS NORMALLY OUT (WRITE = LOGIC "0") AND TURNS INWARD (READ = LOGIC "1") WHEN THE FIRST DATA WORD IS NEEDED FROM THE SUBSYSTEM. THE OUTPUT WILL RETURN LOW (WRITE) AFTER THE LAST DATA WORD TRANSMISSION HAS BEGUN ON THE 1553 BUS.

**NOTE:** THIS SIGNAL CAN BE PLACED IN A HIGH IMPEDANCE STATE IF **DT\_ACK** IS NOT ACTIVE. SEE **ADDR\_ENA** FOR MORE DETAILS.

**CS:** CHIP SELECT - ACTIVE LOW LEVEL OUTPUT PULSE PRESENT IN THE MIDDLE OF EVERY DATA TRANSFER. WHEN THE BUS-65149 IS WRITING DATA TO THE SUBSYSTEM, THIS SIGNAL OCCURS WHEN THE DATA IS VALID AND SHOULD BE USED TO LATCH THE DATA (RECOMMEND USING RISING EDGE). WHEN THE BUS-65149 IS READING DATA FROM THE SUBSYSTEM, THIS SIGNAL IS USED TO INFORM THE SUBSYSTEM WHEN TO DRIVE THE DATA BUS.

**NOTE:** THIS SIGNAL CAN BE PLACED IN A HIGH IMPEDANCE STATE IF **DT\_ACK** IS NOT ACTIVE. SEE **ADDR\_ENA** FOR MORE DETAILS.

**BIT\_WD\_REQ:** BIT WORD REQUEST - A RAISING EDGE ON THIS INPUT SIGNAL WHEN THE RT IS NOT PRESENTLY SERVICING A COMMAND WILL TRIGGER A DATA TRANSFER SEQUENCE (**DT\_REQ**, **DT\_GRT**, AND **DT\_ACK**) WHICH WILL TRANSFER THE CONTENTS OF THE INTERNAL BUILT-IN-TEST WORD REGISTER OVER THE PARALLEL DATA BUS TO THE SUBSYSTEM. DURING THIS TRANSFER, **CS** WILL NOT GO ACTIVE. **BW\_STR** WILL GO ACTIVE IN ITS PLACE AND SHOULD BE USED TO LATCH THE DATA. COULD BE CONNECTED DIRECTLY TO EOM IF THE BIT WORD IS DESIRED.

**BW\_STR:** BIT WORD STROBE - ACTIVE LOW LEVEL OUTPUT PULSE PRESENT IN THE MIDDLE OF THE BIT WORD TRANSFER TO THE SUBSYSTEM. THIS SIGNAL OCCURS WHEN THE DATA IS VALID. SHOULD BE USED TO LATCH THE DATA (RECOMMEND USING THE RISING EDGE).

**VW\_BW\_FL:** VALID WORD / BIT WORD ENABLE FLAG - MULTIPLEXED OUTPUT SIGNAL THAT IS DEFINED AS FOLLOWS: IN 1553B MODE OF OPERATION, IF THE EXTERNAL BIT WORD OPTION IS USED (S06 IS SET TO LOGIC "0") AND A MODE TRANSMIT BIT WORD COMMAND IS RECEIVED, THEN THIS SIGNAL WILL GO LOW DURING THE TRANSFER OF THE BIT WORD FROM THE SUBSYSTEM TO THE RT TO BE USED TO INDICATE WHEN THE SUBSYSTEM SHOULD DRIVE THE BUS WITH THE DATA. NOTE, **CS** WILL REMAIN INACTIVE DURING THIS TRANSFER. IN 1553A MODE OF OPERATION, THIS SIGNAL IS USED AS A FLAG TO INFORM THE SUBSYSTEM THAT THE DATA WORD THAT WAS JUST RECEIVED AND IS BEING TRANSFERRED HAD A PARITY OR MANCHESTER ERROR IN IT. LOGIC "0" INDICATES AN ERROR. PRIMARILY USED IN THE BASIC 1553A MODE.

## ADDRESS BUS SIGNALS

**A13:** BROADCAST - LATCHED OUTPUT SIGNAL THAT REPRESENTS THE ADDRESSING OF THE PRESENT COMMAND WORD. THAT IS, IT WAS EITHER A BROADCAST MESSAGE (ALL ONES IN THE RT ADDRESS FIELD AND BRO\_ENA WAS SET TO LOGIC "1") OR A COMMAND ADDRESSSED EXPLICITLY TO THIS TERMINAL (THE ADDRESS FIELD OF THE COMMAND WORD MATCHES THE TERMINAL'S RT\_AD\_4 TO RT\_AD\_0 INPUTS). IT IS UPDATED AFTER NBGRT BUT BEFORE INCMD GOES ACTIVE. A LOGIC "1" INDICATES A BROADCAST COMMAND, A LOGIC "0" INDICATES A COMMAND TO THE BUS-65149'S RT ADDRESS. CLEARED BY RESET.

**NOTE:** THIS SIGNAL CAN BE PLACED IN A HIGH IMPEDANCE STATE IF DT\_ACK IS NOT ACTIVE. SEE ADDR\_ENA FOR MORE DETAILS.

**A12:** TRANSMIT / RECEIVE - LATCHED OUTPUT SIGNAL THAT REPRESENTS THE LATCHED T/R BIT (D10) OF THE PRESENT COMMAND WORD. IT IS UPDATED AFTER NBGRT BUT BEFORE INCMD GOES ACTIVE. A LOGIC "1" INDICATES A TRANSMIT COMMAND, A LOGIC "0" INDICATES A RECEIVE COMMAND. CLEARED BY RESET.

**NOTE:** THIS SIGNAL CAN BE PLACED IN A HIGH IMPEDANCE STATE IF DT\_ACK IS NOT ACTIVE. SEE ADDR\_ENA FOR MORE DETAILS.

**A11 (MSB) THROUGH A07 (LSB):** SUBADDRESS [4:0] - THESE OUTPUTS ARE THE LATCHED DATA FROM THE SUBADDRESS FIELD OF THE COMMAND WORD RECEIVED. THEY ARE UPDATED AFTER NBGRT BUT BEFORE INCMD GOES ACTIVE. THEY ARE CLEARED BY RESET. A11 CORRESPONDS TO SA4 WHICH IS THE MSB AND A07 CORRESPONDS TO SA0 WHICH IS THE LSB.

**NOTE:** THESE SIGNALS CAN BE PLACED IN A HIGH IMPEDANCE STATE IF DT\_ACK IS NOT ACTIVE. SEE ADDR\_ENA FOR MORE DETAILS.

**A06:** COMMAND WORD TRANSFER - ACTIVE LOW LEVEL OUTPUT SIGNAL THAT IS ASSERTED WHEN THE 1553 COMMAND WORD IS BEING TRANSFERRED TO THE SUBSYSTEM OVER THE PARALLEL DATA BUS.

**NOTE:** THIS SIGNAL CAN BE PLACED IN A HIGH IMPEDANCE STATE IF DT\_ACK IS NOT ACTIVE. SEE ADDR\_ENA FOR MORE DETAILS.

**A05(MSB) THROUGH A01(LSB):** WORD COUNT [4:0] / CURRENT WORD COUNT [4:0] MULTIPLEXED OUTPUT SIGNAL WHICH DEFINED AS FOLLOWS: THESE OUTPUTS ARE THE LATCHED DATA FROM THE WORD COUNT FIELD OF THE COMMAND WORD RECEIVED. THEY ARE UPDATED AFTER NBGRT BUT BEFORE INCMD GOES ACTIVE. THEY ARE CLEARED BY RESET. IF THE PRESENT COMMAND IS NOT A MODE CODE AND INCMD IS ACTIVE THEN THESE LINES BECOME THE OUTPUT OF A CURRENT WORD COUNTER. THAT IS, WHEN INCMD GOES ACTIVE, THESE OUTPUTS GO TO LOGIC 0 AND ARE THEN INCREMENTED AFTER EVERY DATA WORD TRANSFER OR TIMEOUT. WHEN INCMD GOES INACTIVE, THEY BECOME THE LATCHED WORD COUNT FIELD AGAIN. A5 CORRESPONDS TO WC4 WHICH IS THE MSB AND A1 CORRESPONDS TO WC0 WHICH IS THE LSB.

**NOTE:** THESE SIGNALS CAN BE PLACED IN A HIGH IMPEDANCE STATE IF DT\_ACK IS NOT ACTIVE. SEE ADDR\_ENA FOR MORE DETAILS.

**A00:** MSB / LSB - OUTPUT SIGNAL THAT IS USED DURING EIGHT BIT DATA TRANSFERS TO INDICATE WHICH BYTE OF THE PRESENT 16 BIT WORD IS BEING TRANSFERRED. A LOGIC "1" INDICATES THE UPPER BYTE (MSB) AND A LOGIC "0" INDICATES THE LOWER BYTE (LSB). IF A 16 BIT DATA STRUCTURE IS USED (DB\_SEL = LOGIC "0"), THIS BIT WILL ALWAYS BE LOGIC "1".

**NOTE:** THIS SIGNAL CAN BE PLACED IN A HIGH IMPEDANCE STATE IF DT\_ACK IS NOT ACTIVE. SEE ADDR\_ENA FOR MORE DETAILS.

## DATA BUS HIGHWAY

**D15 (MSB) THROUGH D00 (LSB):**

BI-DIRECTIONAL DATA BUS. IN THE 8-BIT MODE, D15 CONNECTS TO D7, ... D8 CONNECTS TO D0.

## 1553 BUS INPUT/OUTPUTS

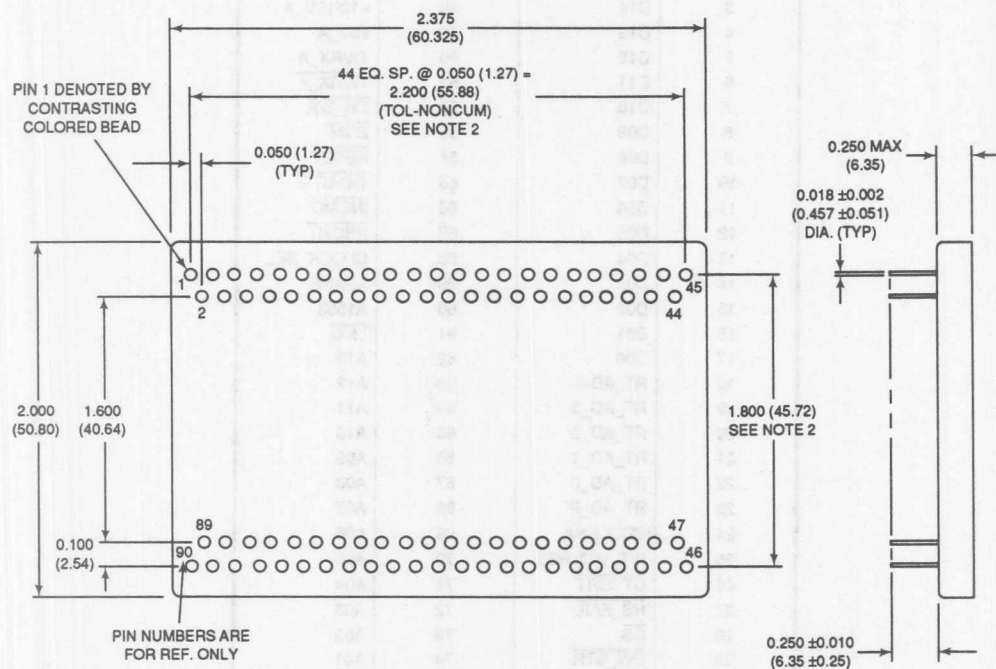
**TX\_RX\_A, TX\_RX\_A, TX\_RX\_B, and TX\_RX\_B:** INPUT/OUTPUTS TO 1553 ISOLATION TRANSFORMERS.



TABLE 4. BUS-65149 PINOUT (preliminary, 2/14/90)

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	+5V (LOGIC)	46	-12/15V_B
2	D15	47	GND_A
3	D14	48	+12/15V_A
4	D13	49	+5V_A
5	D12	50	TX/RX_A
6	D11	51	TX/RX_A
7	D10	52	CH_B/A
8	D09	53	EOM
9	D08	54	RESET
10	D07	55	T-D-STR
11	D06	56	INCMD
12	D05	57	NBGR
13	D04	58	CLOCK_SEL
14	D03	59	ABASE
15	D02	60	A1553
16	D01	61	LMC
17	D00	62	A13
18	RT_AD-4	63	A12
19	RT_AD_3	64	A11
20	RT_AD_2	65	A10
21	RT_AD_1	66	A09
22	RT_AD_0	67	A08
23	RT_AD_P	68	A07
24	BRO_ENA	69	A06
25	BIT_WD_REQ	70	A05
26	DT_GRT	71	A04
27	HS_FAIL	72	A03
28	CS	73	A02
29	BW_STR	74	A01
30	WRT	75	A00
31	DB_SEL	76	TEST_MODE
32	VW_BW_FL	77	CLOCK_IN
33	ADDR_ENA	78	T_A_STR
34	DT_REQ	79	S10
35	RT_FAIL	80	S09
36	ME	81	S08
37	RT_AD_ERR	82	S07
38	GBR	83	S06
39	DT_ACK	84	S05
40	TX/RX_B	85	S04
41	TX/RX_B	86	S03
42	+5VB	87	S02
43	+12/15V_B	88	S01
44	GND_B	89	S00
45	-12/15V_B	90	GND (LOGIC)





**Notes:**

1. Dimensions are in inches (millimeters).
2. Pin cluster to be centralized within ±0.010 (0.25 mm) of outline dimensions.

**BUS-65149 MECHANICAL OUTLINE  
(90-PIN DIP HYBRID)**

**ORDERING INFORMATION**

**BUS-65149-883B**

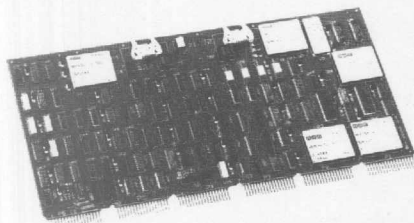
Reliability Grade:

**883B** = Fully compliant with MIL-STD-883.

**B** = Screened to MIL-STD-883 but without  
QCI testing.

Blank = 0° to 70° C

# BUS-65505 AND BUS-65506



## MIL-STD-1553B BC/RTU/MT UNIBUS® INTERFACE UNIT

### FEATURES

- COMPLETE DUAL REDUNDANT INTELLIGENT BC/RTU/MT WITH UNIBUS INTERFACE
- SUPPORTS ALL MIL-STD-1553B MESSAGE FORMATS AND 12 MODE CODES
- 4K x 16 DUAL PORT RAM STORES:  
60 BC MESSAGES PLUS ADDRESS STACK, POINTER AND MESSAGE COUNT;  
119 RTU MESSAGES PLUS COMMAND WORDS AND POINTERS;  
16 MT DATA AREAS AND POINTER
- STANDARD ONE HEX HEIGHT UNIBUS CARD
- UNIBUS NON-PROCESSOR REQUEST DMA TRANSFERS
- COMPLETE WRAP AROUND BUILT-IN-TEST

### DESCRIPTION

The BUS-65505 provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553B data bus and the DEC Unibus. The BUS-65505 Unibus Interface Unit (UBIU) can be operated as a 1553 bus monitor (MT), bus controller (BC) or remote terminal (RTU). The UBIU's 1553 data bus mode of operation is under the control of the subsystem processor's software. The BUS-65505 is packaged on one multi-layer printed circuit card conforming to Unibus size specifications and complies fully with MIL-STD-1553B; supporting 12 mode codes, all message formats and complete wraparound Built-In-Test capability.

The BUS-65505 is easy and flexible to use. User overhead is reduced by the onboard 4K x 16 memory, vectored interrupt priority and bus grant levels.

Unit mode and operation are under subsystem control with functional and electrical compatibility with Unibus specifications.

Double buffering the UBIU's onboard memory prevents partially updated data from being read by the subsystem processor or transmitted to the 1553 data bus. The BUS-65505 will store, respond to and transmit up to 119 messages, depending on the mode of operation selected.

All MIL-STD-1553B functions: address recognition, Manchester coding validation, bit count and mode code response are provided transparent to and without user subsystem intervention.

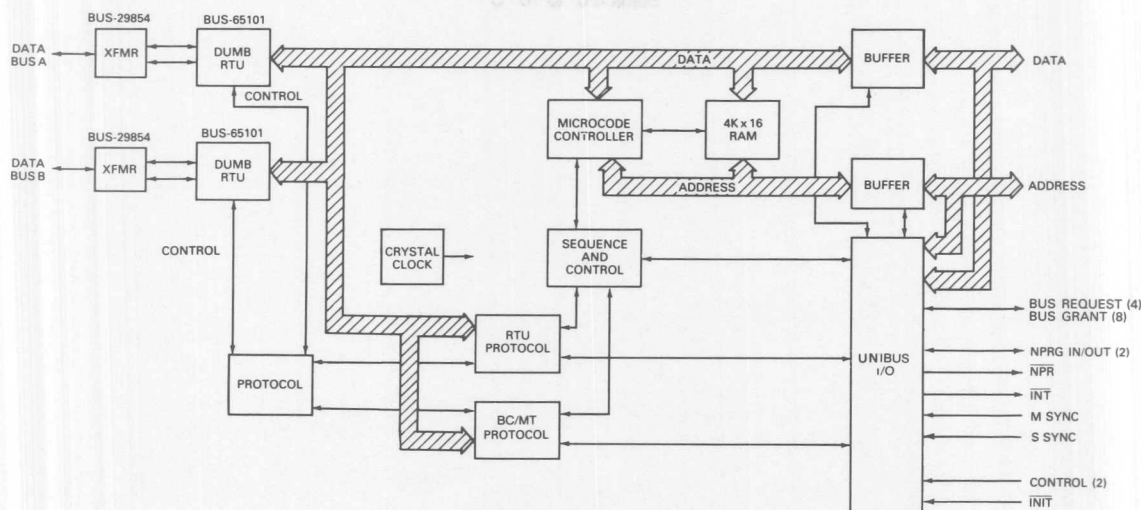


FIGURE 1. BUS-65505 BLOCK DIAGRAM

**TABLE 1. BUS-65505 SPECIFICATIONS**

Values at nominal power supply voltages.		
PARAMETER	UNITS	VALUE
<b>LOGIC</b>		
$I_{IH}, I_{IL}, I_{OH}, I_{OL}$		1 Standard UNIBUS load. See table 5)
$V_{OH}$	V	2.5 min
$V_{OL}$	V	0.4 max
$V_{IH}$	V	2.4 min
$V_{IL}$	V	0.8 max
<b>POWER SUPPLIES</b>		
+5V Supply		
Voltage Tolerance	%	10
Current Drain	A	4.0 max
+12V Supply*		
Voltage Tolerance	%	5
Current Drain	mA	300 max
-12V Supply*		
Voltage Tolerance	%	5
Current Drain	mA	300 max
<b>TEMPERATURE RANGE (Case)</b>		
Operating**	°C	0 to +70
Storage	°C	-65 to +150
<b>SIZE</b>		
	in (cm)	8.43×15.6×0.6 max (21.4×39.6×0.157)

\*BUS-65505 uses  $\pm 12V$  supplies and BUS-65506 uses  $\pm 15V$  supplies.

\*\*Consult factory for wider operating temperature range.

## GENERAL

All data transfers between the UBIU and the subsystem processor are made on a word basis by either a cycle steal DMA using Unibus NPR (non-processor request) or normal I/O transfer with indirect UBIU memory addressing.

Two command/status registers are used by the subsystem processor to read status and load operating parameters. Five additional registers are used for DMA and memory transfers between the UBIU and subsystem. Address for memory and the I/O registers are programmable through groups of jumpers on the circuit board. Interrupt request and grant level are selectable to one of four levels through user programmable jumpers.

The dual redundant 1553B data bus connects to the UBIU by a set of connectors mounted to the top of the circuit board. The UBIU requires one hex Unibus slot.

## BUS CONTROLLER MEMORY OPERATION

While in the bus controller (BC) mode of operation, the UBIU's memory is allocated into 4 main areas:

- Message Count Areas (A & B)
- Data Block Address Pointers (A & B)
- Data Block Address Stacks (A & B)
- Data Blocks

Memory allocations in the BC mode are listed in table 2.

**TABLE 2. BC MEMORY ALLOCATION**

BYTE ADDRESS	CONTENTS
0000	MESSAGE COUNT (A)
0002	MESSAGE COUNT (B)
0004 - 007E	NOT USED
0080 - 00FE	DATA BLOCK 0
0100 - 017E	DATA BLOCK ADDRESS STACK (A)
0180 - 01FE	DATA BLOCK ADDRESS STACK (B)
0200	STACK POINTER (A)
0202	STACK POINTER (B)
0204 - 027E	NOT USED
0280 - 02FE	DATA BLOCK 1
0300 - 037E	DATA BLOCK 2
1F80 - 1FFE	DATA BLOCK 57

## Message Count (A & B)

These memory locations contain the number of messages to be transmitted on the 1553 bus. They are loaded by the subsystem processor before the issuance of the controller start command and decremented by the UBIU during 1553 transfer operations.

## Stack Pointer (A & B)

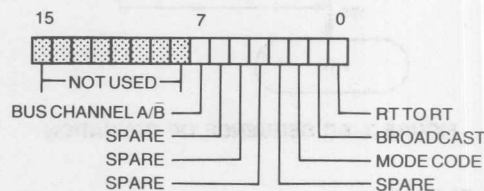
These pointers contain the address of the next data block location to be transferred to the 1553 data bus. The pointers are initialized to stack -2 by the subsystem and incremented by the BC when a data block is to be transferred. In the event of an error interrupt, the pointer will indicate the data block stack location of the error.

## Data Block Address Stack (A & B)

There are FIRST-IN-FIRST-OUT, 64 word stacks. The offset address of each data block ready to be processed is loaded by the subsystem in sequential locations.

## Data Blocks

A maximum of 64 data blocks can be handled by the bus controller. The subsystem processor loads each data block sequentially. Each data block consists of a control word (figure 2) followed by the 1553 command and data word(s) to be transferred. The last data word transferred is looped back to the next addressable location for a loop error test. Received status and data are added to the data block and stored in the same format they appeared on the bus.



**FIGURE 2. CONTROL WORD**

if the transmitting or receiving RT fails to respond with a status word within 14 $\mu$ s. The BC will then issue a format error interrupt to the subsystem processor. This is done to prevent locking the bus as described in MIL-STD-1553B.

### BC Sequence of Operation

The BC START COMMAND, once received, starts the BC sequence of operation. This sequence is illustrated in figure 3.

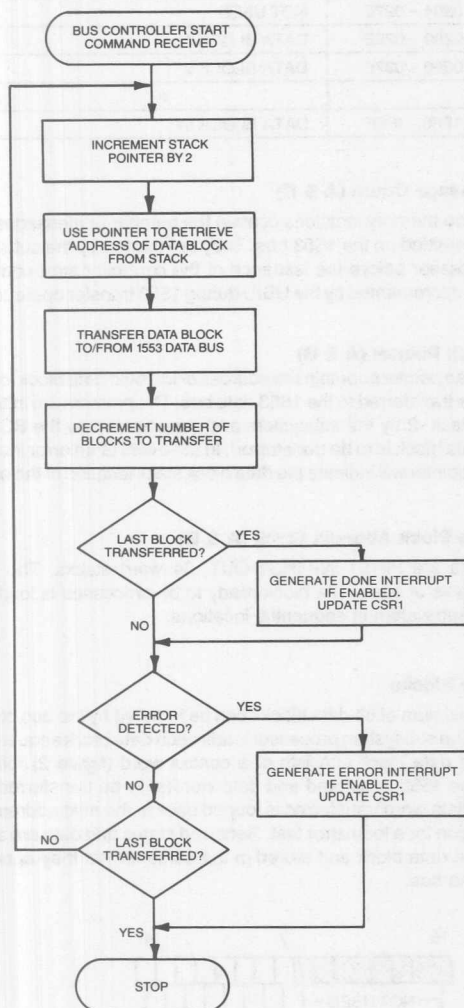


FIGURE 3. BC SEQUENCE OF OPERATION

### DATA FORMATS

Data is stored in the format illustrated in figure 4.

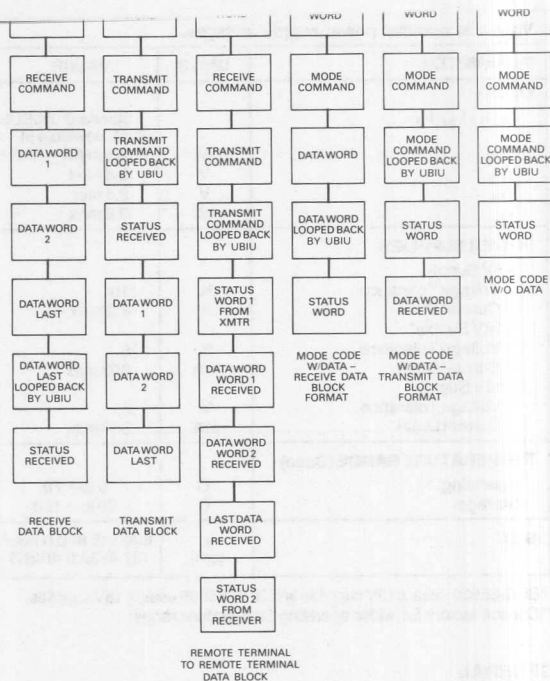


FIGURE 4. DATA FORMATS

### REMOTE TERMINAL MODE – MEMORY OPERATION

In the remote terminal mode (RT), the UBIU's memory is divided into 4 main areas:

- Data Block Look-Up Tables (A & B)
- Command Word Stacks (A & B)
- Command Word Stack Pointers (A & B)
- 119 Data Blocks

Memory allocations in the RT mode are listed in table 3.

TABLE 3. RT MEMORY ALLOCATION	
BYTE ADDRESS	CONTENTS
0000 – 007E	DATA BLOCK LOOK-UP TABLE (A)
0080 – 00FE	COMMAND WORD STACK (A)
0100 – 017E	DATA BLOCK LOOK-UP TABLE (B)
0180 – 01FE	COMMAND WORD STACK (B)
0200	COMMAND WORD STACK POINTER (A)
0202	COMMAND WORD STACK POINTER (B)
0204 – 023E	NOT USED
0240 – 027E	DATA BLOCK 1
	•
	•
	•
1FC0 – 1FFE	DATA BLOCK 119



## Command Word Stack (A & B)

This is a 64 word stack that will store valid received 1553 command words. The command stack may be examined by the subsystem processor (by way of the pointer) to determine the last or current 1553 command received.

## Stack Pointers (A & B)

These locations contain the stack address of the last command word received.

## Data Block Look-up Table (A & B)

The look-up table is a 64 word area that contains the data block base addresses. It is initialized by the subsystem processor with the addresses of the data blocks. The look-up table is addressed by the hardware using the T/R bit and 5 subaddress bits from the command word received. These bits are illustrated in figure 5.

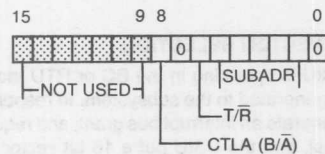


FIGURE 5. DATA BLOCK LOOK-UP TABLE SELECT

## Data Blocks

The data words within each data block are placed sequentially using an internal UBIU word counter. At the beginning of a data block access, bit 15 of the look-up table word is set to indicate a busy condition. This bit is reset after the data block transfer is complete, and a DONE interrupt is generated (if enabled) to the subsystem processor.

## Invalid Command

An incomplete data transfer will result in the RTU generating an error interrupt. If the command being executed at the time of error is to transfer data, the busy flag previously set in the look-up table will not be reset and can be interpreted as an incomplete transfer. If the command had been to transmit data, bit 15 indicates a partially transmitted block. An incomplete data transfer can be caused by the arrival of a superseding command.

## RT Sequence of Operation

A 1553 command, once received by the RT starts the sequence of operation illustrated in figure 6.

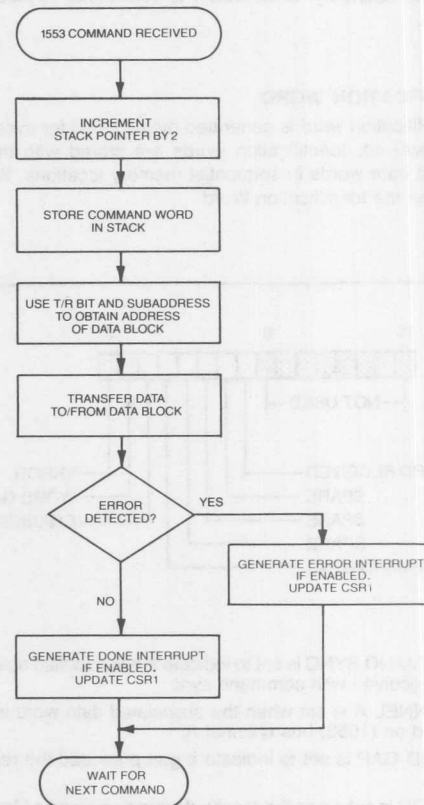


FIGURE 6. RT SEQUENCE OF OPERATION

## BUS MONITOR – MEMORY OPERATION

In this mode, the UBIU's memory is divided into two main areas:

- Data Area Address Pointers (A & B)
- 16 Data Areas

Memory allocations in the MT mode are listed in table 4.

## Data Area Address Pointers (A & B)

The pointers are updated by the UBIU and contain the address (13 LSB) of the last data location processed by the UBIU. Bit 15 of the pointer is set to logic '1' to indicate a word has been received. The pointers should be initialized to the value equal to the starting address of the first Data Block.

TABLE 4. MT MEMORY ALLOCATION

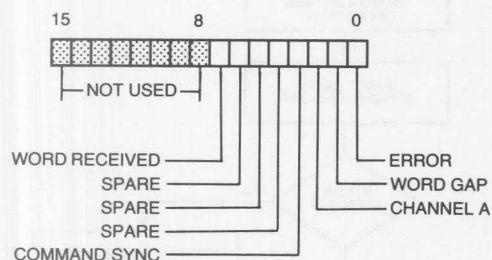
BYTE ADDRESS	CONTENTS
0000	DATA AREA ADDRESS POINTER (A)
0002	DATA AREA ADDRESS POINTER (B)
0004 – 0FFF	NOT USED
1000 – 10FE	DATA AREA 1
1100 – 11FE	DATA AREA 2
	•
	•
	•
1F00 – 1FFF	DATA AREA 16

## Data Areas

Each data area is a 128 word section of sequential memory. Whenever the end of a data area is reached, the beginning of the next area is selected. A DONE flag is set in the CSR1 control register to indicate a word transfer and a DONE interrupt is generated by the UBIU whenever memory addresses cross a data area boundary. Data area 1 is considered to follow data area 16.

## IDENTIFICATION WORD

An identification word is generated by the UBIU for every 1553 word received. Identification words are stored with their associated data words in sequential memory locations. Figure 7 illustrates the Identification Word.



### Notes:

- (1) COMMAND SYNC is set to indicate the associated data word was received with command sync.
- (2) CHANNEL A is set when the associated data word was received on (1553) bus channel A.
- (3) WORD GAP is set to indicate a gap preceded the received word.
- (4) ERROR is set when the received word contained a Manchester, parity or gap error.

**FIGURE 7. IDENTIFICATION WORD**

## DOUBLE BUFFERING

Double buffering is used to prevent partially updated data blocks from being read by the subsystem processor or transmitted to the 1553 data bus. The UBIU's memory is divided into two control areas, A and B, one of which is designated the "current" area by the subsystem processor. The current area is used by the UBIU for receiving and transmitting on the 1553 data bus, while the non-current area is used by the subsystem processor to write into or read from the UBIU memory. The selection of the current area is made by the subsystem processor using the CSR2 command/status register. The actual switching of the control areas is done by the UBIU when it is not active on the 1553 data bus.

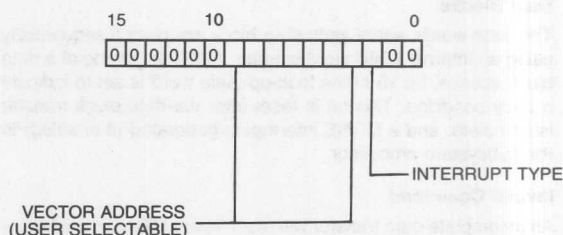
## LOOP TESTS

The UBIU executes loop tests to ensure its operational state. The types of loop tests are:

- **LONG LOOP TEST** – In the bus controller mode only, the UBIU will receive the last word it transmitted and pass this word into memory where it can be processed by the subsystem processor for accuracy of both transmit and receive functions.
- **SHORT LOOP TEST** – is executed whenever the UBIU is operating as bus controller (BC) or remote terminal (RTU). The last word transmitted is looped back to the decoder and compared. An error will cause an error interrupt and a remote terminal to set the terminal flag bit in the 1553 status word.

## INTERRUPT VECTOR SELECTION

When the UBIU is operating in the BC or RTU mode, interrupt requests are generated to the subsystem. In response, the subsystem will generate an interrupt bus grant, and request, through an INTR signal, that the UBIU put a 16 bit vector word on the data lines.



### Notes:

- (1) Bit 2 indicates the INTERRUPT TYPE to the processor. A logic "0" indicates a CSR1, and a logic "1" a CSR2.
- (2) Bus request and grant priorities are user assignable with jumpers to one of four priorities.
- (3) User selectable jumpers determine the interrupt vector address. (See jumper group S3).

**FIGURE 8. INTERRUPT VECTOR**

## MODE CODES

Table 5 lists the 1553 mode codes supported by the UBIU. Any valid 1553 mode code not implemented in the UBIU is considered illegal. The RTU response to an illegal mode code is to set the message error bit in the status word and do nothing further than transmitting the status word.

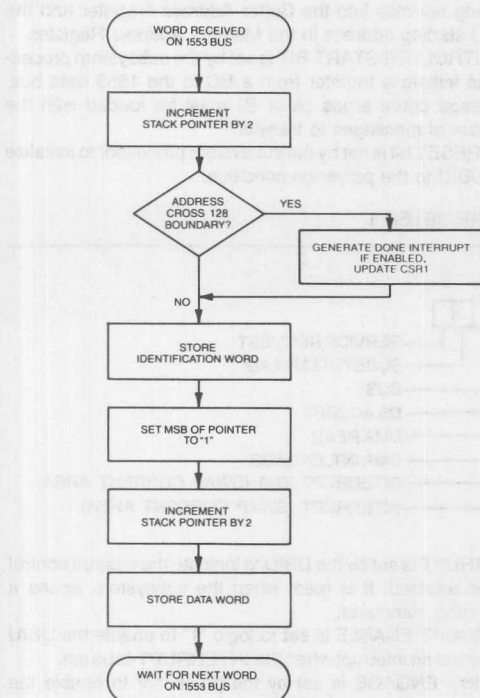
**TABLE 5. MODE CODES**

T/R BIT	MODE CODE	FUNCTION	DATA WORD	BROADCAST
1	00000	Dynamic bus control	NO	NO
1	00001	Synchronize	NO	YES
1	00010	Transmit status word	NO	NO
1	00100	Transmitter shutdown	NO	YES
1	00101	Override transmitter shutdown	NO	YES
1	01000	Reset remote terminal	NO	YES
1	10000	Transmit vector word	From Memory	NO
0	10001	Synchronize	To Memory	YES
1	10010	Transmit last command	From UBIU	NO
1	00110	Inhibit terminal flag	NO	YES
1	00111	Override inhibit terminal flag	NO	YES
1	00011	Initiate self-test	NO	YES

Note: (1) Initiate self-test causes no action since an RT does a continuous short loop test.

## MT Sequence of Operation

Once a word is received on the 1553 bus, the MT sequence of operation follows as illustrated in figure 9.



**FIGURE 9. MT SEQUENCE OF OPERATION**

## SUBSYSTEM I/O

Two forms of Subsystem I/O are available: DMA and non-DMA. To use DMA operation, the subsystem loads the starting address of the UBIU RAM into the UBIU Memory Address Register (MAR XXXXA). The Unibus address can be up to 18 bits. The starting

address of the Unibus memory must be loaded into the DMA Bus Address Register (BAR XXXX6). Address bits 17 and 18 are loaded in bits 4 and 5 of the Command Status Register 1 (CSR1 XXXX0).

The subsystem indicates the direction of data transfer by setting the DMA read bit (bit 4) in the CSR2 (XXXX2) if data is to be transferred from the UBIU to the Unibus subsystem. This bit should be "0" if data is to be written to the UBIU. The subsystem must 1's complement, then enter the word count in the DMA Word Count Register (XXXX8).

DMA transfer is initiated once the subsystem sets the DMA start bit (bit 2) in CSR1. If desired, the UBIU will generate an interrupt when the indicated number of words have been transferred. This is done by setting the DMA Interrupt Enable bit (bit 5) in CSR2.

The subsystem can also implement non-DMA transfers by placing the UBIU RAM address in the BAR (XXXX6) and executing a READ or WRITE statement; this will transfer one word.

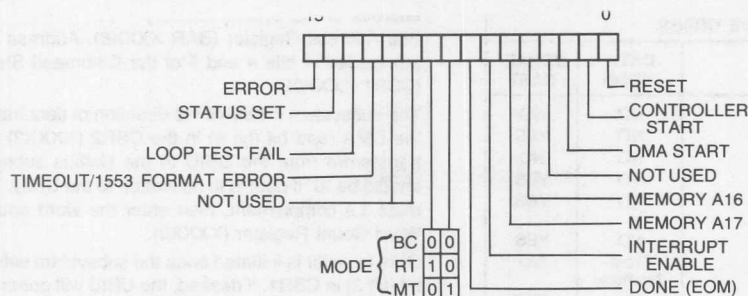
## COMMAND/STATUS REGISTERS

Command/status registers are used to set and read the basic operating parameters of the UBIU. The I/O addresses of these registers are selectable by jumping address bits A13 through A4. The Command/Status Registers are listed in table 6.

**TABLE 6. COMMAND/STATUS REGISTERS**

ADDRESS	NAME	DESCRIPTION	FUNCTION
XXXX0	CSR1	UBIU Command/Status Register 1	Used to load operational mode and to check status of UBIU. Specific modes/functions defined by data word (figure 10).
XXXX2	CSR2	UBIU Command/Status Register 2	Used by subsystem to load/read UBIU control area select, set 4 external 1553 status bits (RT mode), read 1553 channels A and B RT address parity errors, and start/check status of DMA transfer (figure 11).
XXXX4	—	Reserved	—
XXXX6	BAR	DMA Bus Address Register	Loaded by subsystem processor with 16 bit UNIBUS starting address for DMA transfer. The two MSBs are contained in Command/Status Register 1.
XXXX8	WCR	DMA Word Count Register	A 16 bit register loaded by the subsystem processor with the number of words to be transferred during a DMA.
XXXXA	MAR	UBIU Memory Address Register	Contains 13 bit UBIU memory starting address, loaded by subsystem and incremented by two after each DMA transfer.
XXXXC	MDA	UBIU Memory Data Command Register	Memory Data Command issued by the subsystem to initiate transfer of a data word to or from the UBIU memory. The address of the data word is contained in the UBIU MAR.
XXXXE	MDT	UBIU Memory Data Register	Same as Memory Data Command Register.

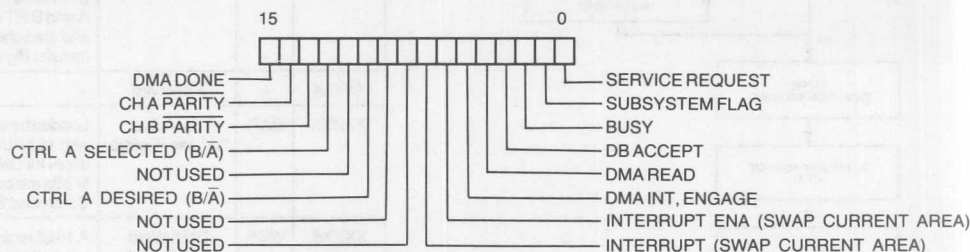
Note: XXXX indicates user programmable hex digits.



**Notes:**

- (1) ERROR will be set by the UBIU if either loop test fail, format error, or status word set are set to a logic "1" condition.
- (2) STATUS SET will be set by a BC whenever the status response from a RTU contains an incorrect address or any of the eight status bits of the 1553 data word are set.
- (3) LOOP TEST FAIL will be set by the UBIU in BC or RTU mode when the last word transmitted over the 1553 bus did not loop back correctly.
- (4) TIMEOUT/1553 FORMAT ERROR is set by the UBIU in the BC or RTU mode to indicate a word/message fault or a no response time out has occurred.
- (5) DONE is set by the UBIU when all the blocks required are transmitted to the 1553 data bus (BC mode) at the completion of every 1553 message transfer (RT mode), or when data has overflowed into the next data area (MT mode).
- (6) INTERRUPT ENABLE bit is set to logic "1" by the subsystem processor to enable the UBIU generating an interrupt when either the DONE or ERROR bit is set. When an interrupt is acknowledged by the processor, further interrupts are inhibited until reenabled. A CSR1 read command issued by the processor clears and reenables the interrupts.
- (7) MEMORY BITS A17 and A16 are set by the subsystem processor when an 18 bit address is used. A17 is the MSB.
- (8) DMA START is set by the subsystem processor to start a DMA transfer. The subsystem must place the number of words to transfer in the Word Count Register, the UNIBUS starting address into the Buffer Address Register and the UBIU starting address in the Memory Address Register.
- (9) CONTROLLER START BIT is set by the subsystem processor to initiate a transfer from a BC to the 1553 data bus. Message count areas (A or B) must be loaded with the number of messages to transfer.
- (10) The RESET bit is set by the subsystem processor to initialize the UBIU to the power-on condition.

**FIGURE 10. COMMAND STATUS REGISTER 1**



**Notes:**

- (1) DMA DONE is set by the UBIU after the number of messages loaded by the processor for transfer have been transferred. This bit is reset when the processor issues a CSR2 read command.
- (2) CHANNEL A/CHANNEL B PARITY reflects the result of the parity check of the RTU address, (0 = error detected, 1 = good status).
- (3) CTRLA SELECTED (B/A) is set by the UBIU when control area A has been selected.
- (4) CTRLA DESIRED (B/A) is set by the processor to request the UBIU set control area A as "current".
- (5) INTERRUPT is set by the UBIU to indicate the desired control area is selected. It is reset when the subsystem issues a CSR2 read command.
- (6) INTERRUPT ENABLE is set to logic "1" to enable the UBIU to generate an interrupt when the INTERRUPT bit is set.
- (7) DMA INT ENGAGE is set by the processor to enable the UBIU to generate DMA DONE interrupts.
- (8) DMA READ is used to indicate the direction for a DMA transfer. When set to logic "1", data direction is from the UBIU to the processor.
- (9) The last four bits are set by the processor and used for the RTU status word.

**FIGURE 11. UBIU COMMAND/STATUS REGISTER 2**



# BUS-65505 AND BUS-65506

**TABLE 7. BUS-65505 CONNECTOR C  
PIN FUNCTIONS**

PIN NO.	NAME	DESCRIPTION	STANDARD BUS LOADS*
CA1	NPRGIN	Non processor request grant in.	1
CA2	+5	+5 Volts	N/A
CB1	NPRGOUT	Non processor request grant out.	1
CB2	-12	-12 Volts	N/A
CC1	$\overline{PA}$	Parity error A. (Not Used)	1
CC2	GROUND	Signal ground.	N/A
CD1		No connection.	
CD2	$\overline{D15}$	Data bit 15.	1
CE1		No connection.	
CE2	$\overline{D14}$	Data bit 14.	1
CF1		No connection.	
CF2	$\overline{D13}$	Data bit 13.	1
CH1	$\overline{D11}$	Data bit 11.	1
CH2	$\overline{D12}$	Data bit 12.	1
CJ1		No connection.	
CJ2	$\overline{D10}$	Data bit 10.	1
CK1		No connection.	
CK2	$\overline{D09}$	Data bit 09.	1
CL1		No connection.	
CL2	$\overline{D08}$	Data bit 08.	1
CM1		No connection.	
CM2	$\overline{D07}$	Data bit 07.	1
CN1		No connection.	
CN2	$\overline{D04}$	Data bit 04.	1
CP1		No connection.	
CP2	$\overline{D05}$	Data bit 05.	1
CR1		No connection.	
CR2	$\overline{D01}$	Data bit 01.	1
CS1	$\overline{PB}$	Parity Error B. (Not Used)	
CS2	$\overline{D00}$	Data bit 00.	1
CT1	Ground	Signal ground.	N/A
CT2	$\overline{D03}$	Data bit 03.	1
CU1	+12	+12 Volts	N/A
CU2	$\overline{D02}$	Data bit 02.	1
CV1		No connection.	
CV2	$\overline{D06}$	Data bit 06.	1

\*One standard Unibus load is defined as:

$I_{IH}$  = maximum input HIGH current at  $V_{in}$  = 2.4V min. = 60 mA.

$I_{IL}$  = maximum input LOW current at  $V_{in}$  = 0.8V max. = -2.0 mA.

$I_{OH}$  = maximum output HIGH current at  $V_{out}$  = 4.5V min. = 25 mA.

$I_{OL}$  = maximum output LOW current at  $V_{out}$  = 0.4V max. = 48 mA.

**TABLE 8. BUS-65505 CONNECTOR D  
PIN FUNCTIONS**

PIN NO.	NAME	DESCRIPTION	STANDARD BUS LOADS*
DA1		No connection.	
DA2	+5	+5 Volts	N/A
DB1		No connection.	
DB2	-12	-12 Volts	N/A
DC1		No connection.	
DC2	GROUND	Signal ground.	N/A
DD1		No connection.	
DD2	$\overline{BR7}$	Bus request 07.	1
DE1		No connection.	
DE2	$\overline{BR6}$	Bus request 06.	1
DF1		No connection.	
DF2	$\overline{BR5}$	Bus request 05.	1
DH1		No connection.	
DH2	$\overline{BR4}$	Bus request 04.	1
DJ1		No connection.	
DJ2		No connection.	
DK1		No connection.	
DK2	BG7IN	Bus grant in 07.	1
DL1	$\overline{INIT}$	Initialize.	1
DL2	BG7OUT	Bus grant out 07.	1
DM1		No connection.	
DM2	BG6IN	Bus grant in 06.	1
DN1		No connection.	
DN2	BG6OUT	Bus grant out 06.	1
DP1		No connection.	
DP2	BG5IN	Bus grant in 05.	1
DR1		No connection.	
DR2	BG5OUT	Bus grant out 05.	1
DS1		No connection.	
DS2	BG4IN	Bus grant in 04.	1
DT1	Ground	Signal ground.	
DT2	BG4OUT	Bus grant out 04.	1
DU1		No connection.	
DU2		No connection.	
DV1		No connection.	
DV2		No connection.	

\*One standard Unibus load is defined as:

$I_{IH}$  = maximum input HIGH current at  $V_{in}$  = 2.4V min. = 60 mA.

$I_{IL}$  = maximum input LOW current at  $V_{in}$  = 0.8V max. = -2.0 mA.

$I_{OH}$  = maximum output HIGH current at  $V_{out}$  = 4.5V min. = 25 mA.

$I_{OL}$  = maximum output LOW current at  $V_{out}$  = 0.4V max. = 48 mA.



# BUS-65505 AND BUS-65506

**TABLE 9. BUS-65505 CONNECTOR E  
PIN FUNCTIONS**

PIN NO.	NAME	DESCRIPTION	STANDARD BUS LOADS*
EA1		No connection.	
EA2	+5	+5 Volts	N/A
EB1		No connection.	
EB2	-12	-12 Volts	N/A
EC1	A12	Address bit 12.	1
EC2	GROUND	Signal ground.	N/A
ED1	A17	Address bit 17.	1
ED2	A15	Address bit 15.	1
EE1	MSYNC	Master sync.	1
EE2	A16	Address bit 16.	1
EF1	A02	Address bit 02.	1
EF2	C01	Control 1.	1
EH1	A01	Address bit 01.	1
EH2	A00	Address bit 00.	1
EJ1	SSYNC	Slave sync.	1
EJ2	C00	Control 0. (Not Used)	1
EK1	A14	Address bit 14.	1
EK2	A13	Address bit 13.	1
EL1	A11	Address bit 11.	1
EL2		No connection.	
EM1		No connection.	
EM2		No connection.	
EN1		No connection.	
EN2	A08	Address bit 08.	1
EP1	A10	Address bit 10.	1
EP2	A07	Address bit 07.	1
ER1	A09	Address bit 09.	1
ER2		No connection.	
ES1		No connection.	
ES2		No connection.	
ET1	GROUND	Signal ground.	N/A
ET2		No connection.	
EU1	A06	Address bit 06.	1
EU2	A04	Address bit 04.	1
EV1	A05	Address bit 05.	1
EV2	A03	Address bit 03.	1

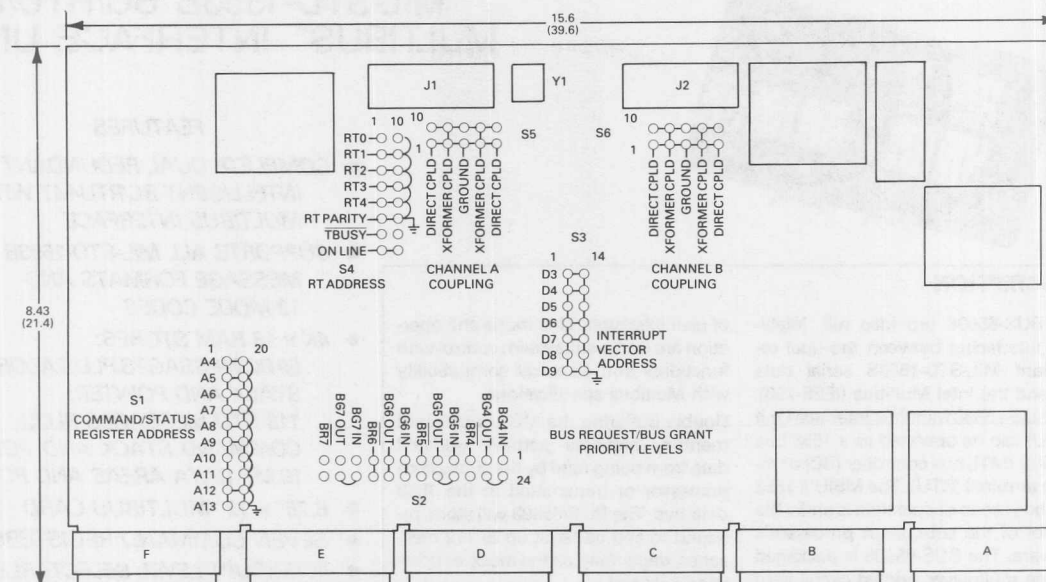
\*One standard Unibus load is defined as:  
 $I_{IH}$  = maximum input HIGH current at  $V_{in}$  = 2.4V min. = 60 mA.  
 $I_{IL}$  = maximum input LOW current at  $V_{in}$  = 0.8V max. = -2.0 mA.  
 $I_{OH}$  = maximum output HIGH current at  $V_{out}$  = 4.5V min. = 25 mA.  
 $I_{OL}$  = maximum output LOW current at  $V_{out}$  = 0.4V max. = 48 mA.

**TABLE 10. BUS-65505 CONNECTOR F  
PIN FUNCTIONS**

PIN NO.	NAME	DESCRIPTION	STANDARD BUS LOADS*
FA1		No connection.	
FA2	+5	+5 Volts	N/A
FB1		No connection.	
FB2	-12	-12 Volts	N/A
FC1		No connection.	
FC2	GROUND	Signal ground.	N/A
FD1	BBUSY	Bus busy.	2
FD2		No connection.	
FE1		No connection.	
FE2		No connection.	
FF1		No connection.	
FF2		No connection.	
FH1		No connection.	
FH2		No connection.	
FJ1	NPR	Non processor request.	1
FJ2		No connection.	
FK1		No connection.	
FK2		No connection.	
FL1		No connection.	
FL2		No connection.	
FM1	INTR	Interrupt.	1
FN1		No connection.	
FN2		No connection.	
FP1		No connection.	
FP2		No connection.	
FR1		No connection.	
FR2		No connection.	
FS1		No connection.	
FS2		No connection.	
FT1	GROUND	Signal ground.	N/A
FT2	SACK	Slave acknowledge.	2
FU1		No connection.	
FU2		No connection.	
FV1		No connection.	
FV2		No connection.	

\*One standard Unibus load is defined as:  
 $I_{IH}$  = maximum input HIGH current at  $V_{in}$  = 2.4V min. = 60 mA.  
 $I_{IL}$  = maximum input LOW current at  $V_{in}$  = 0.8V max. = -2.0 mA.  
 $I_{OH}$  = maximum output HIGH current at  $V_{out}$  = 4.5V min. = 25 mA.  
 $I_{OL}$  = maximum output LOW current at  $V_{out}$  = 0.4V max. = 48 mA.

Dimensions are in inches (cm).



**Notes:**

- (1) Command Status Register address bits A14-A17 are non-selectable and set to logic "1". Bits A4-A13 are user selectable.
- (2) Interrupt Vector Address bits, D0, D1, and D10 through D15 are non-selectable and set internally to logic "0". D2 indicates the type of interrupt: CSR1 or CSR2, (1 = interrupt received, 0 = no interrupt active).
- (3) The UBIU is shipped factory strapped for:  
1553 Channel A = XFMR Coupled  
1553 Channel B = XFMR Coupled  
Remote Terminal Address = 01  
Command/Status Register Address = 111 110 110 000 00- ...  
Interrupt Vector = 0 000 000 100 100 -00  
Interrupt Priority Level = 6

(4) Pin Definitions

Pin No.	J1 Connector Connection
J1/1	BUS A POS
J1/3	
J1/5	BUS A NEG
J1/2	FRAME GROUND
J1/4	FRAME GROUND
J1/6	FRAME GROUND

Pin No.	J2 Connector Connection
J2/1	BUS B POS
J2/3	
J2/5	BUS B NEG
J2/2	FRAME GROUND
J2/4	FRAME GROUND
J2/6	FRAME GROUND

**FIGURE 12. MECHANICAL OUTLINE AND JUMPER CONFIGURATIONS**

**ORDERING INFORMATION**

BUS-65505

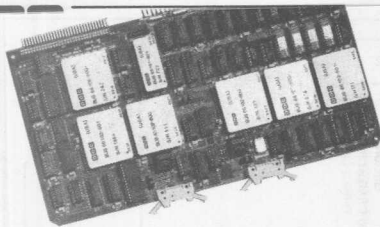
Power Supply Option:  
5 =  $\pm 12$ VDC supplies  
6 =  $\pm 15$ VDC supplies

Mating J1/J2 1553 connectors supplied with card:  
2 each – BERG 65846-007 (connector housing)  
12 each – BERG 47712 (associated terminals)

For Driver Software contact:

Digital Equipment Corporation  
1901 West 14th Street  
Tempe, Az. 85281-6983

Contact: Ms. Darla Lasky  
602/894-4751



# MULTIBUS<sup>®</sup> INTERFACE UNIT

## FEATURES

- COMPLETE DUAL REDUNDANT INTELLIGENT BC/RTU/MT WITH MULTIBUS INTERFACE
- SUPPORTS ALL MIL-STD-1553B MESSAGE FORMATS AND 12 MODE CODES
- 4K x 16 RAM STORES:  
59 BC MESSAGES PLUS ADDRESS STACK AND POINTER;  
119 RTU MESSAGES PLUS COMMAND STACK AND POINTER;  
16 MT DATA AREAS AND POINTER
- 6.75" x 12" MULTIBUS CARD
- SEVEN COMMAND REGISTERS
- INTERRUPT LEVEL SELECTABLE TO ANY OF THE EIGHT MULTIBUS INTERRUPTS
- WRAPAROUND BUILT-IN-TEST CAPABILITY

## DESCRIPTION

The BUS-65508 provides full, intelligent interfacing between the dual redundant MIL-STD-1553B serial data bus and the Intel Multibus (IEEE-796). The BUS-65508 Multibus Interface Unit (MBIU) can be operated as a 1553 bus monitor (MT), bus controller (BC) or remote terminal (RTU). The MBIU's 1553 data bus mode of operation is under the control of the subsystem processor's software. The BUS-65508 is packaged on one multi-layer printed circuit card conforming to Multibus size specifications and complies fully with MIL-STD-1553B; supporting 12 mode codes, all message formats and complete wrap-around Built-In-Test capability.

The BUS-65508 is easy and flexible to use. User overhead is reduced by the onboard 4K x 16 memory and six types

of user interrupts. Unit mode and operation are under subsystem control with functional and electrical compatibility with Multibus specifications.

Double buffering the MBIU's onboard memory prevents partially updated data from being read by the subsystem processor or transmitted to the 1553 data bus. The BUS-65508 will store, respond to and transmit up to 119 messages, depending on the mode of operation selected.

All MIL-STD-1553B functions: address recognition, Manchester coding validation, bit count and mode code response are provided transparent to and without user subsystem intervention.

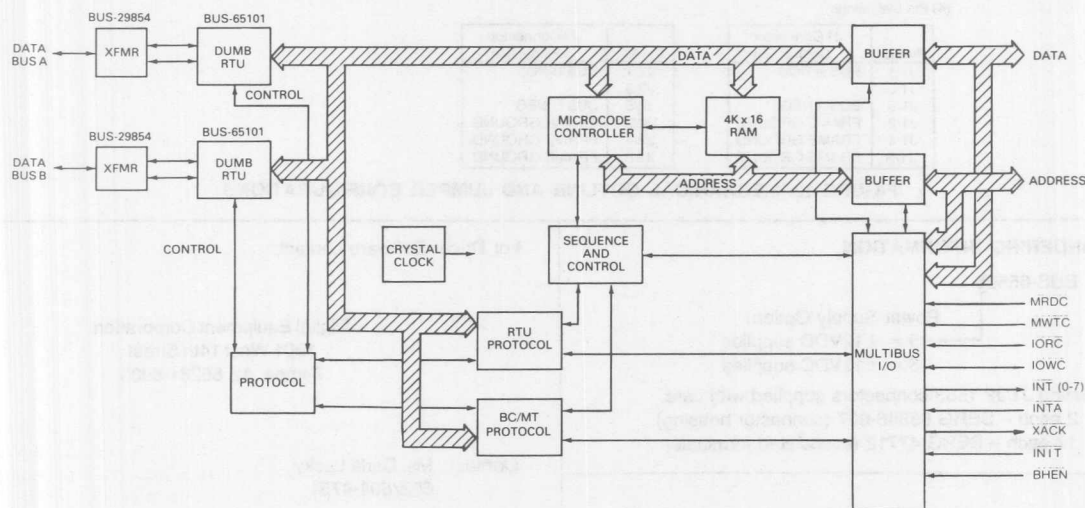


FIGURE 1. BUS-65508 BLOCK DIAGRAM

®Multibus is a Registered Trademark of Intel Corporation.

**TABLE 1. BUS-65508 SPECIFICATIONS**

Values at nominal power supply voltages.		
PARAMETER	UNITS	VALUE
<b>LOGIC</b>		
$I_{IH}, I_{IL}, I_{OH}, I_{OL}$		See Pin Function & Loading Table
$V_{OH}$	V	2.5 min
$V_{OL}$	V	0.4 max
$V_{IH}$	V	2.4 min
$V_{IL}$	V	0.8 max
<b>POWER SUPPLIES</b>		
+5V Supply		
Voltage Tolerance	%	10
Current Drain	A	4.0 max
+15V Supply*		
Voltage Tolerance	%	5
Current Drain	mA	300 max
-15V Supply*		
Voltage Tolerance	%	5
Current Drain	mA	300 max
<b>TEMPERATURE RANGE (Case)</b>		
Operating**	°C	0 to +70
Storage	°C	-65 to +150
<b>SIZE</b>		
	in (cm)	6.75×12.0×0.6 max (17.2×30.5×0.157)

\*BUS-65508 uses ±15V supplies and BUS-65509 uses ±12V supplies.

\*\*Consult factory for wider operating temperature range.

## GENERAL

The BUS-65508 is Multibus compliant as a bus slave device and appears to the subsystem processor as programmed I/O. Onboard 4K x 16 memory is directly addressable by the subsystem processor, memory allocation and use is dependent on the mode of operation selected. Addresses for memory and the I/O registers are programmable through groups of jumpers on the circuit board. The 1553 bus interface and onboard memory management are transparent to the subsystem processor.

Seven registers are provided to the subsystem processor to read the status and load the operating parameters of the MBIU. Interrupt level is jumperable to any of the eight parallel interrupt lines supported on the Multibus.

The dual redundant 1553B data bus connects to the MBIU by two connectors mounted to the top of the circuit board. The MBIU mounts to the Multibus by the 86 pin P1 connector; the 60 pin P2 connector is not used.

## MEMORY MAPPING

All data transfers between the MBIU and the subsystem processor are made through the Multibus data bus. This is accomplished by considering the MBIU's onboard 4K x 16 memory as processor memory. Memory starting location is user selectable by jumpering the 7 MSBs of the address lines. The 13 LSBs are used to select the desired 4K x 16 onboard memory location. Memory access is only valid when the Multibus signals MRDC or MWTC are asserted by the subsystem processor. Memory transfers to the 1553 bus in all modes of operation are with an indirect addressing scheme. Data is written into the odd and even bytes of the onboard RAM as per Multibus specifications.

## BUS CONTROLLER – MEMORY OPERATION

While in the bus controller (BC) mode of operation, the MBIU's memory is allocated into three main areas:

- Data Block Address Stack (A & B)
- Stack Pointers (A & B)
- Data Blocks

Memory allocation in the BC mode is listed in table 2.

**TABLE 2. BC MEMORY ALLOCATION**

BYTE ADDRESS	CONTENTS
0000 – 007F	DATA BLOCK 58
0080 – 00FF	DATA BLOCK 59
0100 – 017F	DATA BLOCK ADDRESS STACK (A)
0180 – 01FF	DATA BLOCK ADDRESS STACK (B)
0200 – 0201	STACK POINTER (A)
0202 – 0203	STACK POINTER (B)
0204 – 027F	NOT USED
0280 – 02FF	DATA BLOCK 1
0300 – 037F	DATA BLOCK 2
0380 – 03FF	DATA BLOCK 3
	•
	•
	•
1F80 – 1FFF	DATA BLOCK 57

## Data Block Address Stacks (A & B)

These are FIRST-IN-FIRST-OUT, 64 word stacks. The address of each data block ready to be processed is contained in sequential locations.

## Stack Pointers (A & B)

These memory locations contain the offset of the next data block location to be transferred on the 1553 data bus. The pointers are initialized to stack minus 2 and incremented by the BC when a data block is to be transferred. In the event of an error interrupt, the pointer will indicate the data block stack location of the error.

## Data Blocks

Each data block contains one 1553 message. A maximum of 64 data blocks can be handled by the bus controller.

The subsystem processor loads each data block sequentially. Each data block consists of a control word followed by the 1553 command and data word(s) to be transferred. The last data word transferred is looped back to the next addressable location for a short loop error test. Received status and data are added to the data block and stored in the same format they appeared on the bus.

## Time Out – Bus Controller Mode

The BC will reset itself and prepare to receive a new command if the transmitting or receiving RT fails to respond with a status word within 14μs. The BC will then issue a format error interrupt to the subsystem processor. This is done to prevent locking the bus as described in MIL-STD-1553B.

## Data Formats

The different data formats are shown in figure 4. Note that one block represents one memory location.



## BC Sequence of Operation

Figure 2 illustrates the BC sequence of operation once a BC Start Command is received.

## BC Control Word

Figure 3 illustrates the Control Word which determines the type of operation that is performed.

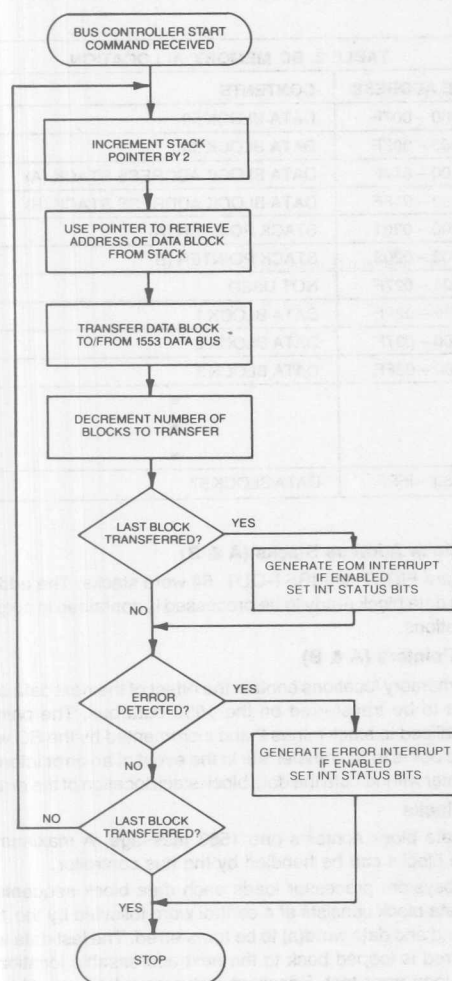


FIGURE 2. BC SEQUENCE OF OPERATION

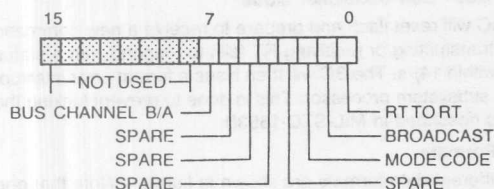


FIGURE 3. BC CONTROL WORD

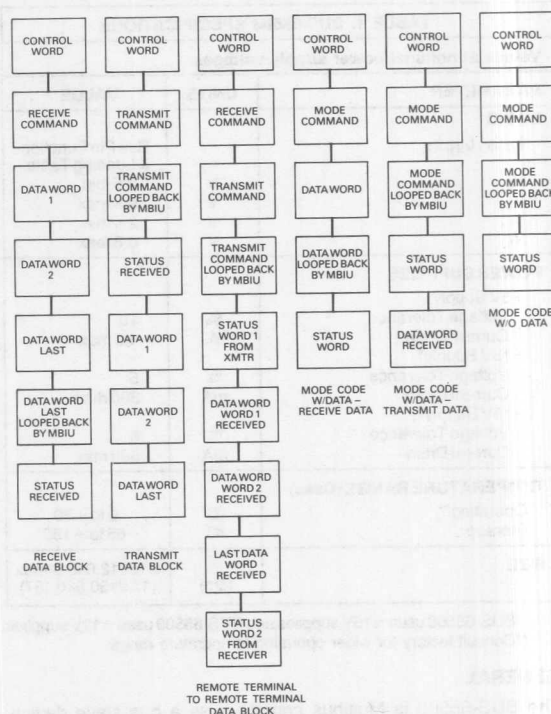


FIGURE 4. DATA FORMATS

## REMOTE TERMINAL MODE - MEMORY OPERATION

In the remote terminal mode (RT), the MBIU's memory is divided into 4 main areas:

- Data Block Look-Up Tables (A & B)
- Command Word Stacks (A & B)
- Stack Pointers (A & B)
- 119 Data Blocks

Memory allocation in the RT mode is listed in table 3.

TABLE 3. RT MEMORY ALLOCATION	
BYTE ADDRESS	CONTENTS
0000 - 007F	DATA BLOCK LOOK-UP TABLE (A)
0080 - 00FF	COMMAND WORD STACK (A)
0100 - 017F	DATA BLOCK LOOK-UP TABLE (B)
0180 - 01FF	COMMAND WORD STACK (B)
0200 - 0201	STACK POINTER (A)
0202 - 0203	STACK POINTER (B)
0204 - 023F	NOT USED
0240 - 027F	DATA BLOCK 1
	•
	•
	•
1FC0 - 1FFF	DATA BLOCK 119



word placed in the command stack. They should be initialized to a value equal to the first stack entry minus two byte locations.

#### Command Word Stacks (A & B)

These are 64 word stacks that will store valid received 1553 command words. The command stack may be examined by the subsystem processor (by way of the pointer) to determine the 1553 command received.

#### Data Block Look-up Table (A & B)

The look-up table is a 64 word area that contains the data block addresses. It is initialized by the subsystem processor with the addresses of the data blocks. The look-up table is addressed by the hardware using the T/R bit and 5 subaddress bits from the command word received. These bits are illustrated in figure 5.

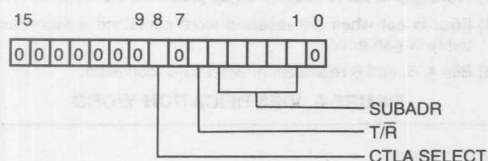


FIGURE 5. DATA BLOCK LOOK-UP TABLE SELECT

#### Data Blocks

The data words within each data block are placed sequentially using an internal MBIU word counter. At the beginning of a data block access, bit 15 of the look-up table word is set to indicate a busy condition. This bit is reset after the data block transfer is complete, and an EOM interrupt is generated to the subsystem processor.

#### Invalid Command

An incomplete data transfer will result in the RTU generating an error interrupt. The busy flag previously set in the look-up table will not be reset and can be interpreted as an invalid or incomplete data transfer.

Figure 6 illustrates the RT sequence of operation once a 1553 command is received.

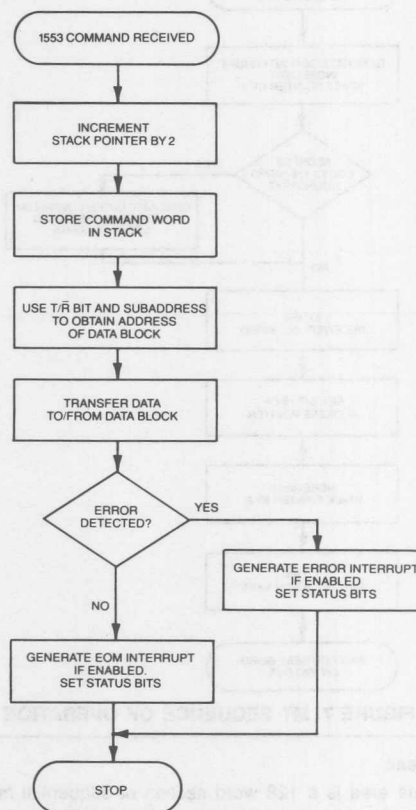


FIGURE 6. RT SEQUENCE OF OPERATION

#### BUS MONITOR – MEMORY OPERATION

In this mode, the MBIU's memory is divided into two main areas:

- Data Area Address Pointers
- 16 Data Areas

Memory allocation in the MT mode is listed in table 4.

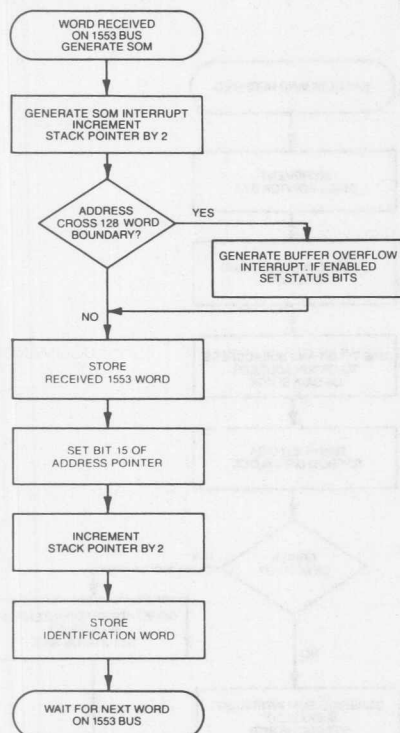
#### Data Area Address Pointers

Pointers are updated by the MBIU and contain the address (13 LSB) of the last data location processed by the MBIU. Bit 15 of the Identification Word is set to logic '1' to indicate a word has been received.

BYTE ADDRESS	CONTENTS
0000 – 0001	DATA AREA ADDRESS POINTER (A)
0002 – 0003	DATA AREA ADDRESS POINTER (B)
0004 – 0FFF	NOT USED
1000 – 11FF	DATA AREA 1
1100 – 11FF	DATA AREA 2
	•
	•
	•
1F00 – IFFF	DATA AREA 16

## MT Sequence of Operation

Figure 7 illustrates the MT sequence of operation once a word is received on the 1553 bus.



**FIGURE 7. MT SEQUENCE OF OPERATION**

## Data Areas

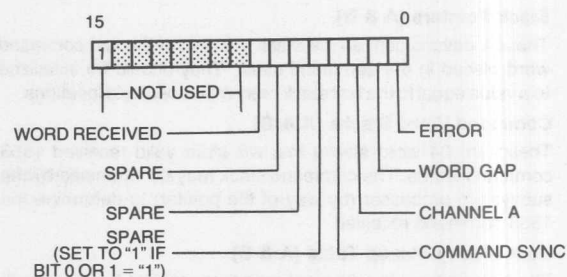
Each data area is a 128 word section of sequential memory. Whenever the end of a data area is reached, the beginning of the next area is selected. A buffer overflow interrupt is generated whenever the data overflows into the next data area. Data area 1 is considered to follow data area 16.

## Identification Word

An identification word is generated by the MBIU for every 1553 word received (figure 8). Identification words are stored with their associated data words in sequential memory locations.

## DOUBLE BUFFERING

Double buffering is used to prevent partially updated data blocks from being read by the subsystem processor or transmitted to the 1553 data bus. The MBIU's memory is divided into two control areas, A and B, one of which is designated the "current" area by the subsystem processor. The current area is used by the MBIU for receiving and transmitting on the 1553 data bus, while the non-current area is used by the subsystem processor to write into or read from the MBIU memory. The selection of the current area is made by the subsystem processor using the MODE/STATUS register command. The actual switching of the control areas is done by the MBIU when it is not active on the 1553 data bus.



### Notes:

- (1) Command sync is set to indicate the associated data word was received with command sync.
- (2) Channel A is set when the associated data word was received on (1553) bus channel A.
- (3) Word gap is set to indicate a gap preceded the received word.
- (4) Error is set when the received word contained a Manchester, parity or gap error.
- (5) Bits 4, 5, and 6 represent a "don't care" condition.

**FIGURE 8. IDENTIFICATION WORD**

## LOOP TESTS

The MBIU executes loop tests to ensure its operational state. The types of loop tests are:

- **LONG LOOP TEST** – The MBIU, in the bus controller mode only, will receive the last word it transmitted and pass this word into memory where it can be processed by the subsystem processor for accuracy of both transmit and receive functions.
- **SHORT LOOP TEST** – is executed whenever the MBIU is operating as bus controller (BC) or remote terminal (RTU). The last word transmitted is looped back to the decoder and compared. An error will cause an error interrupt and in addition, a remote terminal to set the terminal flag bit in the 1553 status word.

## INTERRUPT PROCESSING

The MBIU will generate an interrupt to the subsystem to indicate a completed transfer (EOM) or an error condition. The interrupt is non-vectored and is received on the level indicated via the S7 jumpers. The subsystem must issue an Interrupt Status command (XXXC) to read the interrupt. This command also clears the interrupt register and the interrupt request.

On power-on or MBIU reset command, the interrupt register is not cleared, but interrupt requests are inhibited. The Interrupt Status register must be read to clear the register and enable future interrupts.

## COMMAND/STATUS REGISTERS

Command/status registers are used to set and read the basic operating parameters of the MBIU. I/O addresses are user selectable by jumpers on the 3 most significant hex digits, the least significant hex digit identifies the specific register. These registers appear to the subsystem processor as I/O and will only respond when the Multibus signals IORC or IOWC are asserted. The data word associated with each command/status register defines the specific function(s) required. The registers are listed along with their function in table 5. Figures 9 through 14 illustrate and further define the registers.

TABLE 5. COMMAND/STATUS REGISTER

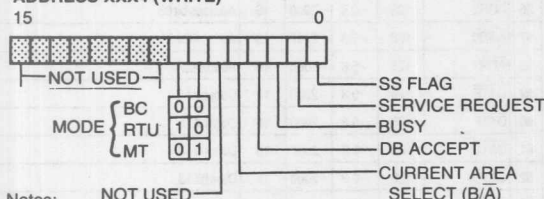
ADDRESS <sup>(1)</sup>	REGISTER NAME	FUNCTION	READ/WRITE
XXX0	—	NOT USED	
XXX2	—	NOT USED	
XXX4	MODE	SET MBIU MODE	IOWC
XXX4	STATUS	READ MBIU STATUS	IORC
XXX6	START	CONTROLLER START	IOWC
XXX8	RESET	MBIU RESET <sup>(2)</sup>	IOWC
XXXA	—	NOT USED	
XXXC	MASK	INTERRUPT MASK	IOWC
XXXC	INTSTAT	READ INTERRUPT STATUS	IORC
XXxE	CSR7	CONTINUE/STOP	IOWC

Notes:

(1) XXX indicates user programmable hex digit.

(2) No data word is associated with the MBIU RESET command register. Upon receipt, the MBIU will reset to its initialized state as a bus controller.

ADDRESS XXX4 (WRITE)



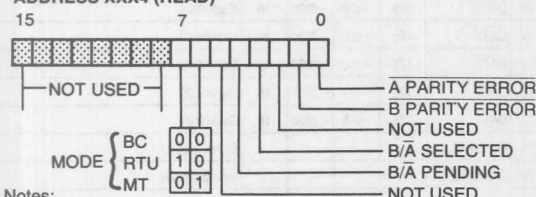
Notes:

(1) This register selects the MBIU mode and sets the four 1553 status bits in the RT mode. The four LSBs are write only bits. Bits 4, 5, 6, and 7 can be set by the subsystem to define the operating parameters and can be read by requesting a MBIU status.

(2) The DB ACCEPT bit is reflected in the 1553 Status Word only after receipt of a Dynamic Bus Control mode code.

FIGURE 9. MBIU MODE DATA WORD

ADDRESS XXX4 (READ)



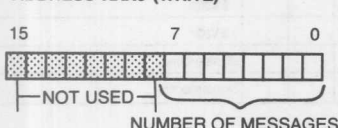
Notes:

(1) This register returns the current operating status to the subsystem processor. Bits 0 and 1: 1 = GOOD STATUS, 0 = ERROR.

(2) An error in CHANNEL A or CHANNEL B parity will not suppress transmission of a Status Word to the BC.

FIGURE 10. MBIU STATUS DATA WORD

ADDRESS XXX6 (WRITE)



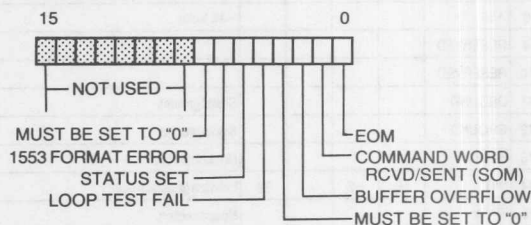
Note: This command register will cause the BC to initiate the transfer of messages preloaded into memory to the 1553 bus. The eight LSBs will contain the number of blocks to transfer (1111111 = 256, 0000000 = 1).

FIGURE 11. CONTROLLER START DATA WORD

ADDRESS XXX8

No data word is associated with this RESET command. Upon receipt, the MBIU will reset to its initialized state as a bus controller.

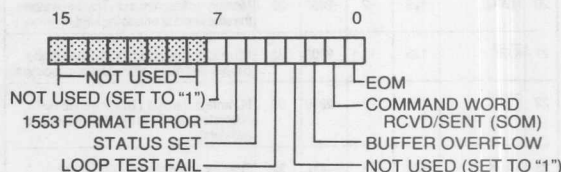
ADDRESS XXXC (WRITE)



Note: This register is written to the MBIU to enable or inhibit the indicated interrupts. A logic "1" will enable the interrupt.

FIGURE 12. INTERRUPT MASK REGISTER

ADDRESS XXXC (READ)



Notes:

(1) This register is read by the subsystem processor to determine which interrupt is pending. A logic "1" indicates a pending interrupt. This register is cleared by the MBIU after it is read by the processor.

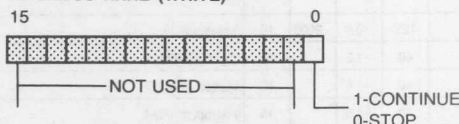
(2) The BC will stop transmission at the end of a data block when an error interrupt is detected.

(3) Status set will be a logic "1" when the BC receives a status word with the wrong RT address or if any of the 8 bits of the 1553 status are set.

(4) Format error will be set if a 1553 word/message format error is received or if a no-response time out occurs.

FIGURE 13. INTERRUPT STATUS DATA WORD

ADDRESS XXxE (WRITE)



Note: Data transmission will cease at the end of the data block upon receipt of a STOP command. The CONTINUE command can then be used to resume processing. In addition, the BC will stop transmitting whenever an Error Interrupt is received. The error could be: LOOP TEST FAIL, TIMEOUT, or FORMAT. After an error condition is detected, the subsystem must issue a MBIU RESET and restart bus transmission via a START command.

FIGURE 14. CONTINUE/STOP DATA WORD

TABLE 7. BUS-65508 (CONNECTOR P1) PIN FUNCTIONS

PIN NO.	NAME	I <sub>IH</sub> ( $\mu$ A)	I <sub>IL</sub> (mA)	I <sub>OH</sub> ( $\mu$ A)	I <sub>OL</sub> (mA)	DESCRIPTION
1	GROUND					Signal ground.
2	GROUND					Signal ground.
3	+5					+5 Volts
4	+5					+5 Volts
5	+5					+5 Volts
6	+5					+5 Volts
7	+15					+15 Volts
8	+15					+15 Volts
9	RESERVED					
10	RESERVED					
11	GROUND					Signal ground.
12	GROUND					Signal ground.
13	BCLK					No connection.
14	INIT	50	-2		32	Initialize (master reset).
15	BPRN					No connection.
16	BPRO					No connection.
17	BUSY					No connection.
18	BREQ					No connection.
19	MRDC	125	-2	-2000	32	Memory read command. (This line enables the subsystem to read the MBIU memory.)
20	MWTC	125	-2	-2000	32	Memory write command. (This line enables the subsystem to write to the MBIU memory.)
21	IORC	125	-2	-2000	32	I/O read command. (This line enables the subsystem to read the MBIU status registers.)
22	IOWC	125	-2	-2000	32	I/O write command. (This line enables the subsystem to write to the MBIU command registers.)
23	XACK	125	-2	-400	32	Transfer acknowledge. (A LOW will acknowledge a memory or I/O transfer.)
24	INH1					No connection.
25	LOCK					No connection.
26	INH2					No connection.
27	BHEN	125	-0.8	-2000	16	Byte Hi Enable. (Enables the upper byte of word transfer.)
28	AD10	125	-0.8	-2000	16	Address bit 16.
29	CBRO					No connection.
30	AD11	125	-0.8	-2000	16	Address bit 17.
31	CCLK					No connection.
32	AD12	125	-0.8	-2000	16	Address bit 18.
33	INTA					No connection.
34	AD13	125	-0.8	-2000	16	Address bit 19.
35	INT6	40	-1.6		16	Interrupt priority 6.
36	INT7	40	-1.6		16	Interrupt priority 7.
37	INT4	40	-1.6		16	Interrupt priority 4.
38	INT5	40	-1.6		16	Interrupt priority 5.
39	INT2	40	-1.6		16	Interrupt priority 2.
40	INT3	40	-1.6		16	Interrupt priority 3.
41	INT0	40	-1.6		16	Interrupt priority 0. (Highest priority.)
42	INT1	40	-1.6		16	Interrupt priority 1.

TABLE 7. BUS-65508 (CONNECTOR P1) PIN FUNCTIONS (CONT'D)

PIN NO.	NAME	I <sub>IH</sub> ( $\mu$ A)	I <sub>IL</sub> (mA)	I <sub>OH</sub> ( $\mu$ A)	I <sub>OL</sub> (mA)	DESCRIPTION
43	ADRE	125	-0.8	-2000	16	Address bit 14.
44	ADRF	125	-0.8	-2000	16	Address bit 15.
45	ADRC	125	-0.8	-2000	16	Address bit 12.
46	ADRD	125	-0.8	-2000	16	Address bit 13.
47	ADRA	125	-0.8	-2000	16	Address bit 10.
48	ADRB	125	-0.8	-2000	16	Address bit 11.
49	ADR8	125	-0.8	-2000	16	Address bit 08.
50	ADR9	125	-0.8	-2000	16	Address bit 09.
51	ADR6	125	-0.8	-2000	16	Address bit 06.
52	ADR7	125	-0.8	-2000	16	Address bit 07.
53	ADR4	125	-0.8	-2000	16	Address bit 04.
54	ADR5	125	-0.8	-2000	16	Address bit 05.
55	ADR2	125	-0.8	-2000	16	Address bit 02.
56	ADR3	125	-0.8	-2000	16	Address bit 03.
57	ADR0	125	-0.8	-2000	16	Address bit 00.
58	ADR1	125	-0.8	-2000	16	Address bit 01.
59	DATE	125	-0.8	-2000	16	Data bit 14.
60	DATF	125	-0.8	-2000	16	Data bit 15.
61	DATC	125	-0.8	-2000	16	Data bit 12.
62	DATD	125	-0.8	-2000	16	Data bit 13.
63	DATA	125	-0.8	-2000	16	Data bit 10.
64	DATB	125	-0.8	-2000	16	Data bit 11.
65	DAT8	125	-0.8	-2000	16	Data bit 08.
66	DAT9	125	-0.8	-2000	16	Data bit 09.
67	DAT6	125	-0.8	-2000	16	Data bit 06.
68	DAT7	125	-0.8	-2000	16	Data bit 07.
69	DAT4	125	-0.8	-2000	16	Data bit 04.
70	DAT5	125	-0.8	-2000	16	Data bit 05.
71	DAT2	125	-0.8	-2000	16	Data bit 02.
72	DAT3	125	-0.8	-2000	16	Data bit 03.
73	DAT0	125	-0.8	-2000	16	Data bit 00.
74	DAT1	125	-0.8	-2000	16	Data bit 01.
75	GROUND					Signal ground.
76	GROUND					Signal ground.
77	RESERVED					
78	RESERVED					
79	-15					-15 Volts
80	-15					-15 Volts
81	+5					+5 Volts
82	+5					+5 Volts
83	+5					+5 Volts
84	+5					+5 Volts
85	GROUND					Signal ground.
86	GROUND					Signal ground.

## Notes:

- (1) I<sub>IH</sub> = maximum input HIGH current with V<sub>in</sub> = 2.4V min.
- (2) I<sub>IL</sub> = maximum input LOW current with V<sub>in</sub> = 0.8V max.
- (3) I<sub>OL</sub> = maximum output LOW current with V<sub>out</sub> = 0.4V max.
- (4) I<sub>OH</sub> = maximum output HIGH current with V<sub>out</sub> = 4.5V min.
- (5) Connector P2 for factory use only.



## MULTIBUS COMPLIANCE

The BUS-65508 is Multibus compliant in the following modes:

- Bus slave device
- D(16) 8/16 bit data path
- (M20) 20 bit memory address path
- (I16) 8/16 bit I/O address path
- (V0) 8 levels, nonvectored interrupts

## MODE CODES

The 1553 mode codes which are supported by the MBIU are listed in table 6.

## BUS-65508 TIMING

Diagrams for RTU and BC Interrupt Timing are shown in figures 15 and 16. Multibus timing is shown in figure 18.

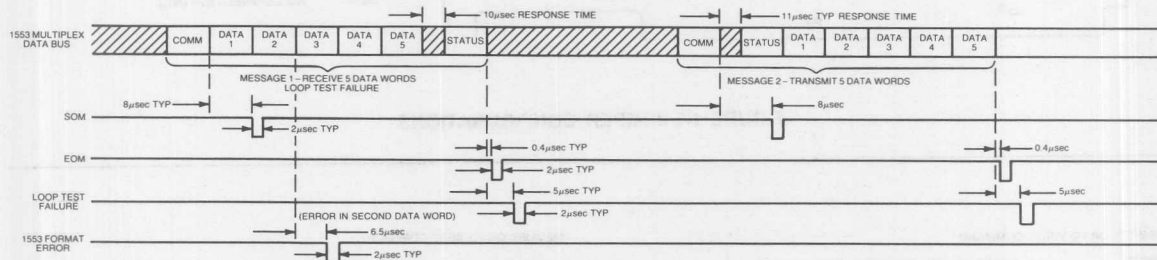
## BUS-65508 PIN FUNCTIONS AND LOADING

Table 7 lists the pin functions along with a description and loading characteristics.

TABLE 6. MODE CODES				
T/R BIT	MODE CODE	FUNCTION	DATA WORD	BROADCAST
1	00000	Dynamic bus control	NO	NO
1	00001	Synchronize	NO	YES
1	00010	Transmit status word	NO	NO
1	00100	Transmitter shutdown	NO	YES
1	00101	Override transmitter shutdown	NO	YES
1	01000	Reset remote terminal	NO	YES
1	10000	Transmit vector word	From Memory	NO
0	10001	Synchronize	To Memory	YES
1	10010	Transmit last command	From MBIU	NO
1	00110	Inhibit terminal flag	NO	YES
1	00111	Override inhibit terminal flag	NO	YES
1	00011	Initiate self-test	NO	YES

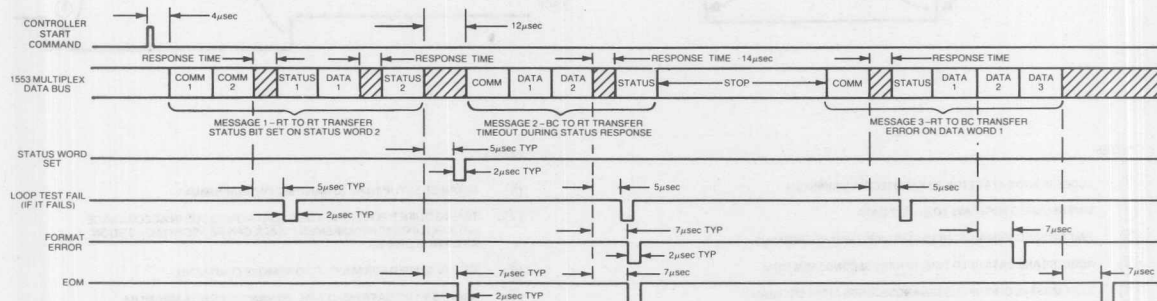
Notes:

- (1) Synchronize without a data word is interpreted as a standard transmit command.
- (2) Initiate self-test causes RT to do a normal short loop test.



Notes:  
(1) Actual interrupt is NOR of the enable interrupts encountered. Interrupt line remains low until interrupt status register is read.  
(2) All measurements taken from mid bit parity crossing of 1553 word indicated.

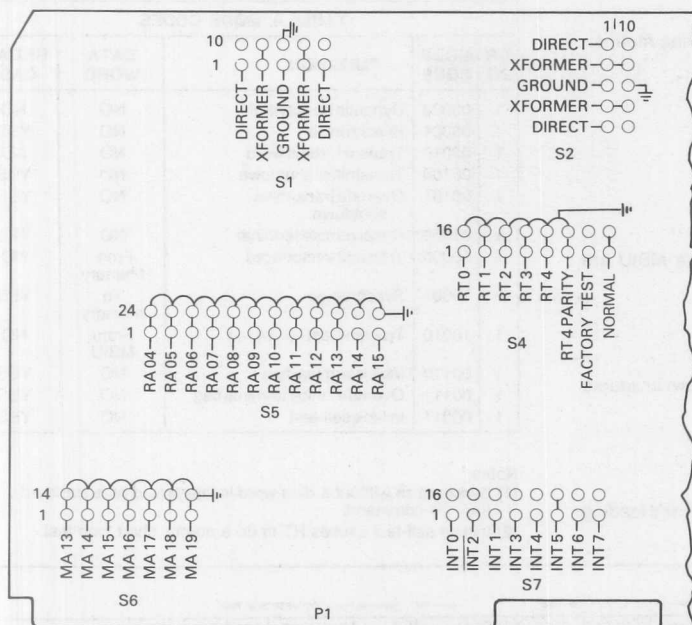
FIGURE 15. RTU INTERRUPT TIMING



Note:  
All measurements taken from mid bit parity crossing of 1553 word indicated.

FIGURE 16. BC INTERRUPT TIMING



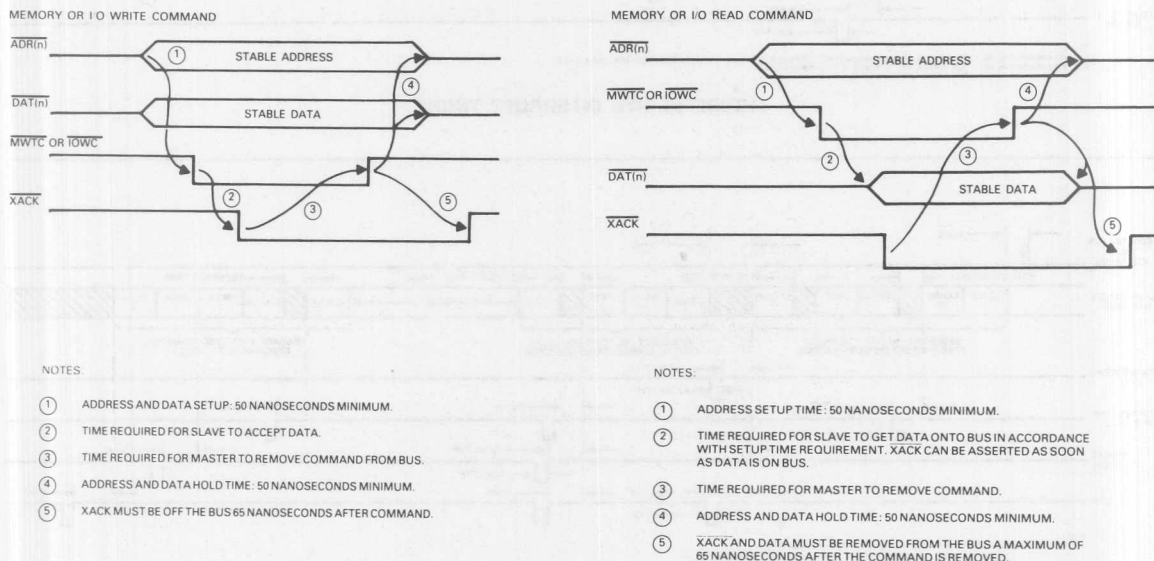


**JUMPER CONFIGURATION**  
S1 & S2: 1553 BUS COUPLING (S1 = CHANNEL A)  
S4: REMOTE TERMINAL ADDRESS,  
JUMPER INSTALLED = 0.  
S6: MEMORY ADDRESS,  
JUMPER INSTALLED = 0.  
S7: INTERRUPT LEVEL

**FACTORY STRAPPING**  
THE MBIU IS SHIPPED STRAPPED FOR:  
1553 CHANNEL A = XFMR COUPLED  
1553 CHANNEL B = XFMR COUPLED  
REMOTE TERMINAL ADDRESS = 01  
REGISTER ADDRESS = C000  
MEMORY ADDRESS = 00000  
INTERRUPT LEVEL = 5

PIN DEFINITION	
J1 CONNECTOR	CONNECTION
PIN NO.	
J1/1	1553 CHANNEL A DATA
J1/2	NO CONNECTION (NC)
J1/3&4	1553 CHANNEL A CHASSIS GROUND
J1/5	1553 CHANNEL A DATA
J1/6	NO CONNECTION (NC)
J2 CONNECTOR	CONNECTION
J2/1	1553 CHANNEL B DATA
J2/2	NO CONNECTION (NC)
J2/3&4	1553 CHANNEL B CHASSIS GROUND
J2/5	1553 CHANNEL B DATA
J2/6	NO CONNECTION (NC)

FIGURE 17. JUMPER CONFIGURATIONS



NOTES:

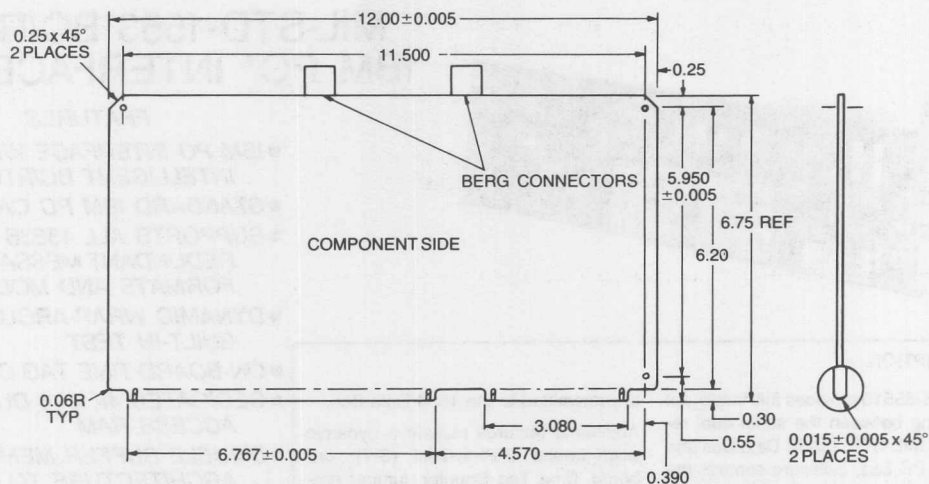
- ① ADDRESS AND DATA SETUP: 50 NANOSECONDS MINIMUM.
- ② TIME REQUIRED FOR SLAVE TO ACCEPT DATA.
- ③ TIME REQUIRED FOR MASTER TO REMOVE COMMAND FROM BUS.
- ④ ADDRESS AND DATA HOLD TIME: 50 NANOSECONDS MINIMUM.
- ⑤ XACK MUST BE OFF THE BUS 65 NANOSECONDS AFTER COMMAND.

NOTES:

- ① ADDRESS SETUP TIME: 50 NANOSECONDS MINIMUM.
- ② TIME REQUIRED FOR SLAVE TO GET DATA ONTO BUS IN ACCORDANCE WITH SETUP TIME REQUIREMENT. XACK CAN BE ASSERTED AS SOON AS DATA IS ON BUS.
- ③ TIME REQUIRED FOR MASTER TO REMOVE COMMAND.
- ④ ADDRESS AND DATA HOLD TIME: 50 NANOSECONDS MINIMUM.
- ⑤ XACK AND DATA MUST BE REMOVED FROM THE BUS A MAXIMUM OF 65 NANOSECONDS AFTER THE COMMAND IS REMOVED.

FIGURE 18. MULTIBUS TIMING DIAGRAMS

# BUS-65508 AND BUS-65509



**FIGURE 19. BUS-65508 MECHANICAL OUTLINE**

## ORDERING INFORMATION

BUS-65508

Power Supply Option:

8 = ±15VDC supplies

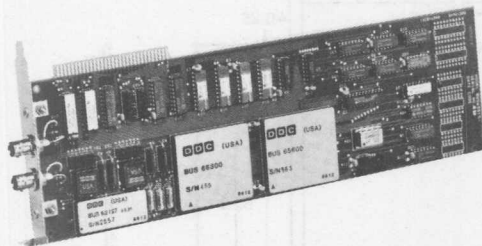
9 = ±12VDC supplies

Mating J1/J2 1553 connectors supplied with card:

2 each – BERG 65846-007 (connector housing)

12 each – BERG 47712 (associated terminals)

## MIL-STD-1553 BC/RTU/MT IBM PC® INTERFACE UNIT



### FEATURES

- IBM PC INTERFACE WITH INTELLIGENT BC/RTU/MT
- STANDARD IBM PC CARD SIZE
- SUPPORTS ALL 1553B DUAL REDUNDANT MESSAGE FORMATS AND MODE CODES
- DYNAMIC WRAP-AROUND BUILT-IN TEST
- ON-BOARD TIME TAG COUNTER
- DEDICATED 4K x 16 DUAL ACCESS RAM
- DOUBLE BUFFER MEMORY ARCHITECTURE TO INSURE DATA INTEGRITY
- MEMORY MAPPED INTERFACE
- SOFTWARE PROGRAMMABLE RTU ADDRESS AND DATA BLOCK ALLOCATIONS
- JUMPER PROGRAMMABLE INTERRUPT LEVEL SELECTION

### DESCRIPTION

The BUS-65515 provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553B Data Bus and the IBM PC Bus. Software controls the BUS-65515's operation as either a 1553 Bus Controller (BC), Remote Terminal Unit (RTU), or Bus Monitor (MT).

The BUS-65515 is packaged on one full size IBM PC printed circuit card. Its on-board 4K x 16 dual access RAM is double buffered, preventing partially updated data from being read by the CPU

or transmitted to the 1553 Data Bus.

Additional features include a dynamic wrap-around Built-In-Test (BIT), on-board Time Tag Counter, jumper programmable interrupt level and BUS-65515 RTU address selection. The BUS-65515 supports all dual redundant mode codes and message formats. Its full compliance with MIL-STD-1553B makes it an excellent choice for dynamic simulation applications.

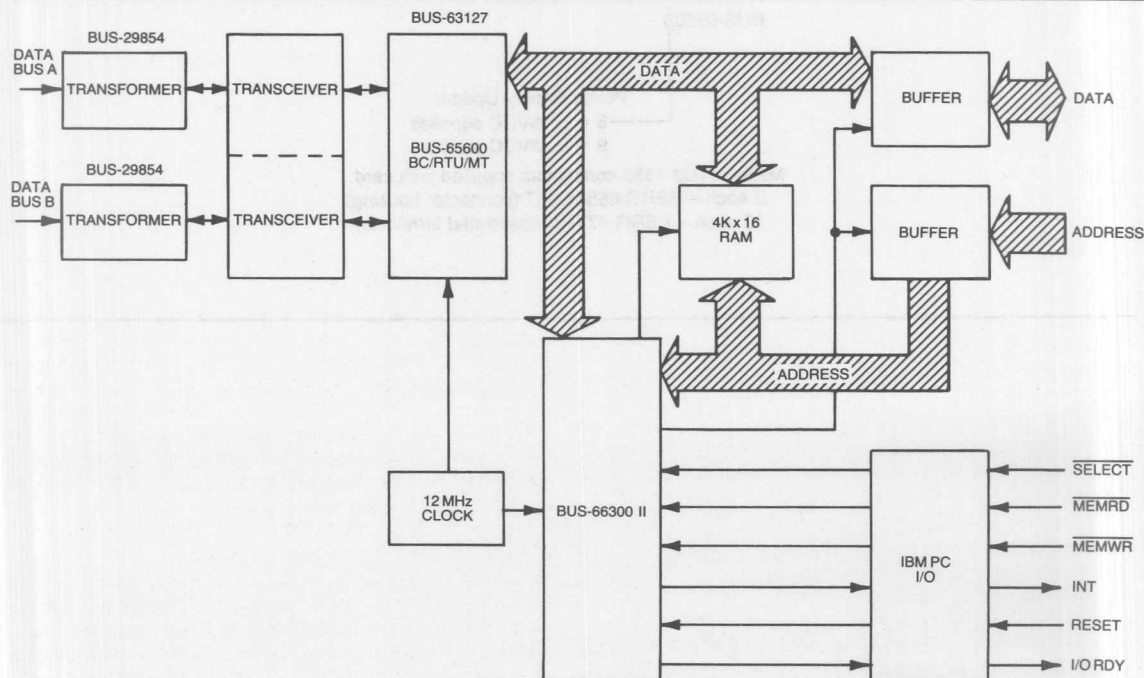


FIGURE 1. BUS-65515 BLOCK DIAGRAM

**TABLE 1. BUS-65515 SPECIFICATIONS**

Specifications at nominal power supply voltages and 25°C.

PARAMETER	UNITS	VALUE
<b>Logic</b>		
V <sub>OH</sub>	V	2.4
V <sub>OL</sub>	V	0.4
I <sub>IH</sub>	μA	40
I <sub>IL</sub>	mA	0.8
I <sub>OH</sub> (1)	mA	-2.6
I <sub>OL</sub> (1)	mA	24
I <sub>OH</sub> (2)	mA	-5.2
I <sub>OL</sub> (2)	mA	16
I <sub>OZH</sub>	μA	40
I <sub>OL</sub>	μA	-40
V <sub>IH</sub>	V	2
V <sub>IL</sub>	V	0.6
<b>Power Supplies</b>		
Voltage, Current Drain	V, Amps	+5.0 ± 10%, 1.00 max
Voltage, Current Drain	V, Amps	+12.0 ± 10%, 0.05 max
Voltage, Current Drain	V, Amps	-12.0 ± 10%, 0.32 max
<b>Temperature Range</b>		
Operating (Case)	°C	0 to +70
Storage	°C	-65 to +150
<b>Physical Characteristics</b>		
Size (Full size IBM PC card)	in (cm)	4.5 x 13.5 x 0.44 (11.4 x 34.3 x 1.1)
Notes: (1) Value for pins A2 through A9. (2) Value for pins B11 and B12.		

## GENERAL

The BUS-65515 provides a user friendly interface between the serial MIL-STD-1553B Bus and the IBM PC Bus. It is memory mapped to the computer's address space and does not require an I/O driver. The operating modes of the BUS-65515 are controlled through the use of four on-board registers. 1553 message traffic is stored and retrieved using the dedicated, memory mapped, on-board RAM.

Internal registers control and operate the BUS-65515. They include the Configuration Register, Start/Reset Register, Interrupt Mask Register, and RTU Address Register. The Configuration Register defines the operating mode. The Start/Reset Register generates the start and reset signals. The Interrupt Mask register enables desired interrupts, with the interrupt priority level being jumper programmable by the user. The RTU Address Register is used to program the RTU address.

The BUS-65515's 4K x 16 high speed static RAM is shared by the CPU and the 1553 Bus with memory arbitration handled automatically by the BUS-65515.

The BUS-65515 will withhold the  $\overline{\text{IOCHRDY}}$  (I/O Channel Ready) signal from the CPU while a word is being transferred to or from the 1553 Bus. Since the memory arbitration is handled by simply stretching the handshake cycle, the wait state is transparent to the CPU's software. A maximum wait of 2.25 μs may occur.

The RAM implements the Stacks and Look-Up Tables required for the different modes of operation, as well as for storing the 1553 messages. A double buffering architecture is available to prevent partially updated information from being transferred to

or from the 1553 Bus. A Descriptor Stack is used in both BC and RTU modes. This stack records the status of each message, the time the message was transmitted or received, and contains either the received 1553 command, (in RTU mode), or the actual address of the data block containing the 1553 message (in BC mode). In the RTU mode, a Look-Up Table is implemented to store the address of the data blocks to be used when receiving or transmitting messages for a particular subaddress.

The BUS-65515 may also be used as a passive MT; in this mode the BUS-65515 records all messages transferred across 1553 Bus A or Bus B. The BUS-65515 generates an Identification Word for each word, indicating its sync type (command or data), the 1553 channel it was received on, (A or B), whether it contained an error, (parity, incorrect bit count, etc.) and whether it was preceded by a gap of more than 2.5 μs. If the gap was more than 2.5 μs, the length of the gap, (in 0.5 μs units) using 8 bit resolution is given.

## ADDRESSING THE BUS-65515 WITH A MICROPROCESSOR

The BUS-65515 contains DDC's BUS-66300 II to manage its on-board 4K x 16 RAM. It converts all CPU supplied byte addresses to word addresses, with two bytes constituting one word. For example, the BUS-65515 divides all addresses supplied by the CPU by two to create the appropriate word address (the memory maps shown in this data sheet reflect the offset).

All pointers used by the BUS-65515 are assumed to be word addresses. For example, to begin Descriptor Stack B at byte locations 1001-1000, the user initializes Descriptor Stack Pointer B to word location 0800 (1000 divided by two). This is done by:

```
POKE 0202, 00  LOAD UPPER BYTE OF
                STACK POINTER B
POKE 0203, 08  LOAD LOWER BYTE OF
                STACK POINTER B
```

Subsequent transfers to or from the Stack will be addressed relative to 1000. The hardware offsetting of the CPU's address bus creates the situation that a "POKE 1000, 01" command actually writes the value 01 into location 0800 of the on-board shared RAM.

## IMPLEMENTATION OF THE DESCRIPTOR STACK

The BUS-65515 uses a Descriptor Stack in BC and RTU modes which may reside anywhere in the non-fixed area of RAM (see figures 2 and 3). The Stack Pointer is 16 bits and resides in a fixed area of RAM. The 8 LSBs of the Stack Pointer are loaded into an internal counter which the BUS-65515 increments by four after each 1553 message has been processed. The results are loaded back into the Stack Pointer location in RAM. Any carry generated by the counter is ignored. As a result, the stack occupies 256 contiguous words of memory, and the 256th word is automatically followed by the first word in the Stack (see figure 4). The 8 MSBs are used as a base address.

The Descriptor Stack is divided into four word descriptor blocks. The first word is the Block Status Word. The second word contains the time tag, and the third is reserved for system use. The contents of the fourth word depend on the operating mode of the BUS-65515. In BC mode it contains the address of the 1553 message. In RTU mode it contains the received 1553 command word. See the description of the particular operating mode for more information.

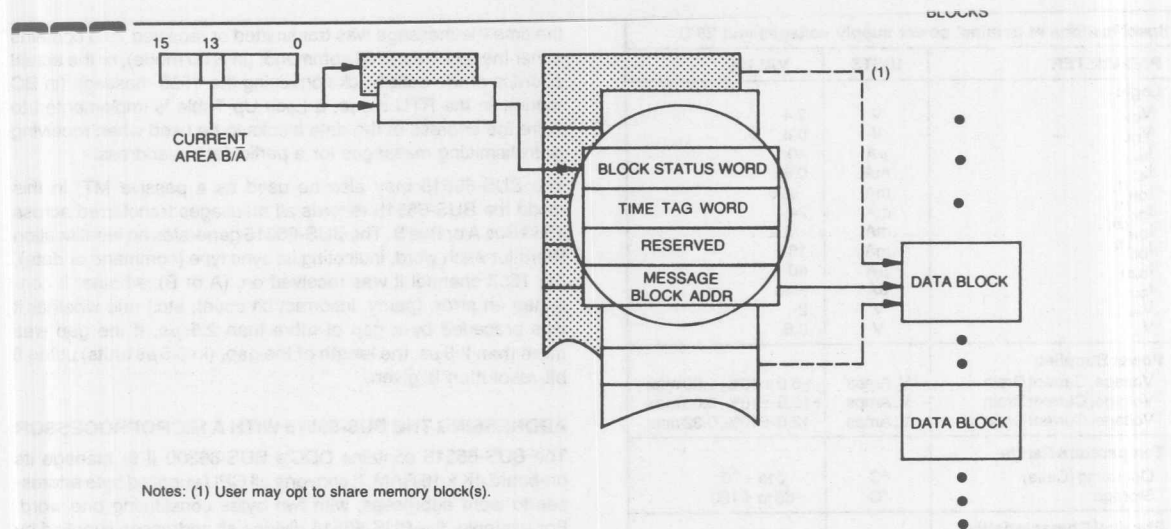


FIGURE 2. USE OF DESCRIPTOR STACK – BC MODE

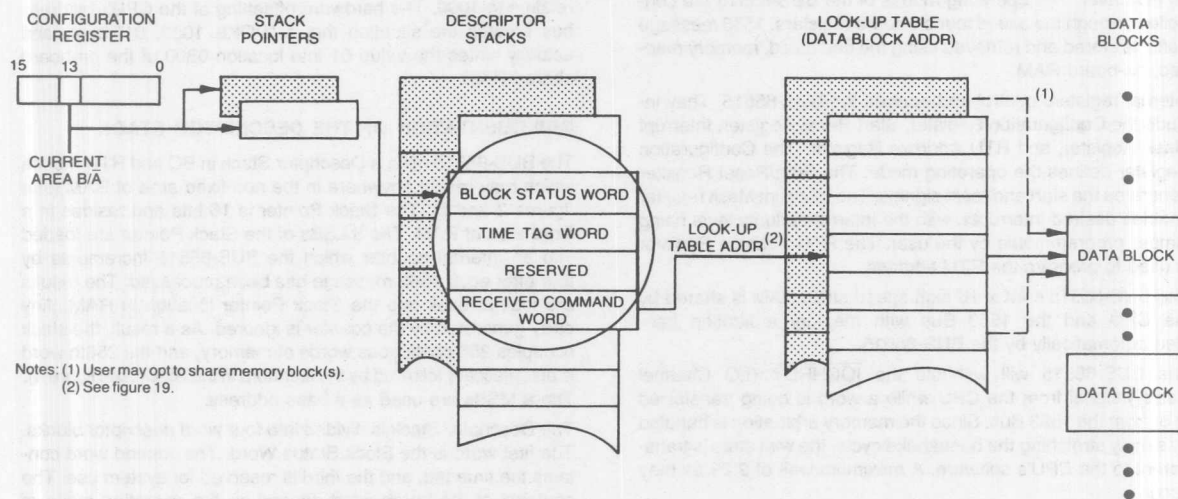
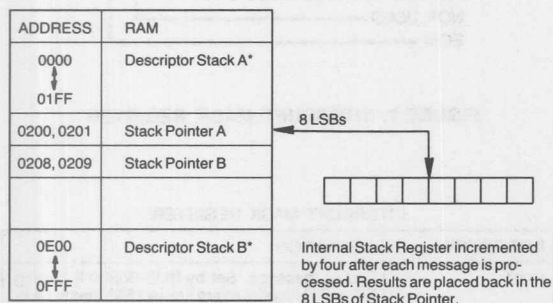


FIGURE 3. USE OF DESCRIPTOR STACK – RTU MODE



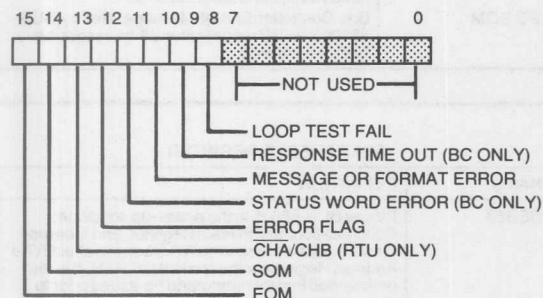
**BLOCK STATUS WORD.** The Start-of-Message (SOM) bit is set by the BUS-65515 when it begins processing the message associated with that particular Descriptor Block. The End-of-Message (EOM) bit is set and the SOM reset upon completion of the message. MESSAGE STATUS and ERROR bits are also set at that time. See figure 5 and table 2.

**TIME TAG:** In BC and RTU modes a Time Tag is loaded into the Descriptor Stack at the beginning of each message and updated at the end. Each of the 16 bits represent 1  $\mu$ s. The Time Tag can be programmed to clear upon receipt of a Reset Mode Code using an optional on-board illegalization PROM. Contact the factory for more information.



\*The address space listed is an example.

**FIGURE 4. IMPLEMENTATION OF DESCRIPTOR STACK**



**FIGURE 5. BLOCK STATUS WORD**

**TABLE 2. BLOCK STATUS WORD BIT DEFINITIONS**

NAME	DEFINITION
EOM	End Of Message. Set at the completion of a message transfer, regardless of whether or not any errors were detected.
SOM	Start Of Message. Set at the beginning of a message transfer and reset upon completion of the message, regardless of whether or not any errors were detected.
CHA/CHB	Channel A/B. Set in RTU mode to indicate whether the message was received on 1553 bus A or B. Set to 0 in BC mode regardless of which bus is used for the message.
ERROR FLAG	Indicates an error was detected during the processing of the particular message. The particular error can be determined by examining bits 0 to 3.
STATUS SET	Set in BC mode to indicate that the received RTU status word had a status bit set or that the wrong RTU responded to the command. Also set in RTU mode when the BUS-65515 is acting as the receiving RTU in an RTU-RTU message transfer to indicate that the wrong RTU responded as the transmitting RTU.
FORMAT ERROR	Set when the MESSAGE ERROR flag is set in the returning RTU's status word or if any word received off the bus violated 1553B specifications (incorrect parity or Manchester sync field, incorrect number of bits, etc.).
RESPONSE TIMEOUT	Set in BC mode if the addressed RTU did not respond within 14 $\mu$ s of receiving a Transmit command or the last data word in a Receive command. Also set in RTU mode when the BUS-65515 is acting as the receiving RTU in a RT-RT message transfer to indicate that the transmitting RTU did not respond in time.
LOOP TEST FAIL	Set to indicate that the BUS-65515 did not pass its continuous on-line self test.

## CONTROL AND STATUS REGISTERS

The BUS-65515 is controlled by seven on-board registers. These registers are also memory mapped to the user's CPU. Table 3 lists the offset address of the registers and they are further defined in the following tables and figures.

**TABLE 3. REGISTERS/DECODER ADDRESS DEFINITIONS**

OFFSET BYTE ADDRESS IN HEX	DEFINITION	R/W	CLEARED BY RESET COMMAND
:2000	Interrupt Mask Register	R/W	Yes
:2001	Illegal	—	—
:2002	Illegal	—	—
:2003	Configuration Register	R/W	Yes
:2004	Illegal	—	—
:2005	Illegal	—	—
:2006	Start/Reset Register	W	Yes
:2007	Illegal	—	—
:2008	RTU Address Register	R/W	No
:2009	Illegal	—	—
:200A	Time Tag Register (byte 0)	R	Yes
:200B	Time Tag Register (byte 1)	R	Yes
:200C	Interrupt Reset Command Register	W	Yes
:200D	Illegal	—	—
:200E	External EOM Command Register	W	No
:200F	Illegal	—	—

**CONFIGURATION REGISTER.** An eight bit read/write register. The four MSBs define the mode of operation; the four LSBs control the RTU status bits in the 1553 Status Word.

Activating the SUBSYSTEM FLAG, SERVICE REQUEST, BUSY, and DB ACCEPT bits to logic "0" in the Configuration Register causes the BUS-65515 to set these bits in the 1553 Status Word. If BUSY is "0", only the Status Word will be transmitted from the BUS-65515 in response to a Transmit Command from the BC, but data associated with a Receive Command will be placed in RAM. Figure 6 shows the Configuration Register and lists the bits definitions.

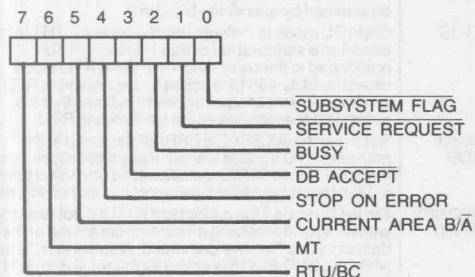


FIGURE 6. CONFIGURATION REGISTER

CONFIGURATION REGISTER

NAME	DEFINITION		
SUBSYSTEM FLAG	1553 Status Word bit.		
SERVICE REQUEST	1553 Status Word bit.		
BUSY	1553 Status Word bit.		
DB ACCEPT	1553 Status Word bit.		
STOP ON ERROR	Causes BC to stop at end of current data block if an error is detected.		
CURRENT AREA B/A	Used for Double Buffering; see description.		
RTU/BC, MT	Operating Mode	Bit 7	Bit 6
	BC	0	0
	MT	0	1
	RTU	1	0
	ILLEGAL	1	1

Note: A "0" in bits 0-3 activates the corresponding bit in the 1553 Status Word.

Note: A "0" in bits 0-3 activates the corresponding bit in the 1553 Status Word.

**INTERRUPT MASK REGISTER.** The Interrupt Mask Register is an eight bit read/write register used to enable interrupt conditions. All interrupts are enabled with a logic "1". Figure 7 shows the register and defines the interrupts.

In BC and RTU modes the BUS-65515 generates an IRQ (Interrupt Request) for an EOM or Error Set condition. An IRQ is generated in the BC mode for a BC EOM indicating that all requested transfers by the BC are completed.

The user may set the priority level of the interrupt to one of six levels (IRQ1-IRQ-7) using the on-board jumper group TB3.

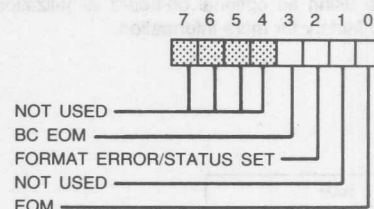


FIGURE 7. INTERRUPT MASK REGISTER

INTERRUPT MASK REGISTER

INTERRUPT	DEFINITION
EOM	End of message. Set by BUS-66300 II (during BC or RTU mode) every time a 1553 message is transferred (regardless of validity).
FORMAT ERROR/STATUS SET	Set by BUS-66300 II for these conditions: <b>Loop Test Failure:</b> Last transmitted word did not match received word. <b>Message Error:</b> Received message contained an address error, one of eight 1553 status bits set, or 1553 specification violated (parity error, Manchester error, etc.). <b>Time-Out:</b> Expected transmission was not received during allotted time. <b>Status Set:</b> Received status word contained status bit(s) set or address error.
BC EOM	Bus Controller End of Message. Set by BUS-66300 II (in BC mode) when all messages have been transferred.

**START/RESET REGISTER.** Two bits of this register are used as shown in figure 8. A logic "1" enables the function.

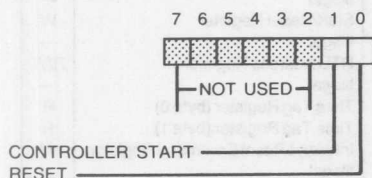
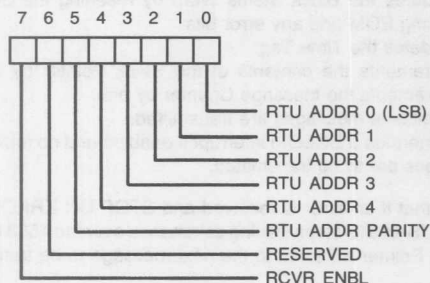


FIGURE 8. START/RESET REGISTER

START/RESET REGISTER

NAME	DEFINITION
RESET	Places BUS-65515 in the power-up condition; Configuration, Start/Reset Register, and Interrupt Mask registers are reset to "0". Does not affect RTU Address Register or the contents of RAM. It is recommended that this command be issued prior to changing the operating mode of the BUS-65515 (RT-BC, BC-MT, etc.).
CONTROLLER START	Used in BC mode to begin transmission of the designated number of messages. The message count must have been previously loaded into the current area message count, using 1's complement notation. Also used in MT mode to begin reception of 1553 message traffic.

**RTU ADDRESS REGISTER.** An internal 8 bit register used to set the RTU address and to enable the BUS-65515 to receive information transferred over the 1553 bus (see figure 9).



**FIGURE 9. RTU ADDRESS REGISTER**

RTU ADDRESS REGISTER	
NAME	DEFINITION
RCVR ENBL	A logic "1" enables the 1553 receivers. Only effective if jumpers TB1-7 are installed.
RTU ADDR PARITY	Odd parity bit associated with five RTU address bits. BUS-65515 will not respond to 1553 commands if the parity is incorrectly set. Set to a logic "1" if RTU Address is 0, 3, 5, or 6.
RTU ADDR 0-4	RTU address bits.

**TIME TAG REGISTERS.** Two registers are used together to form a time tag. The contents are incremented by one every microsecond. The Time Tag is cleared by issuing a Reset command and/or by a received Reset or Synchronize Mode Code command. This is accomplished through an illegalization PROM. Consult the factory for more details.

**INTERRUPT RESET COMMAND REGISTER.** Writing any value to this register will reset the IRQ.

**EXTERNAL EOM COMMAND REGISTER.** This register is used for simulating an EOM condition for factory testing.

## BC MODE

The BC mode is selected by setting the two MSBs of the Configuration Register to logic "0". The BUS-65515 defaults to BC mode upon power up and after receipt of a Reset signal from the CPU.

**BC INITIALIZATION.** For BC operation, the user initializes the RAM, Stack Pointers, Descriptor Stack Entries, and Message Blocks. See table 4 for a sample memory map and follow the steps in figure 10 (A), (B), and (C).

The BUS-65515 uses an indirect addressing architecture to determine which messages to send over the 1553 bus. The Stack Pointer indicates which entry in the Descriptor Stack to use, while the fourth word in the Descriptor Block indicates the location of the 1553 message (see figure 2).

Two Stack Pointers and two Descriptor Stacks are provided to allow the user to double buffer the RAM. All transfers to/from the 1553 bus are made using the "current" Descriptor Stack and Stack Pointer, as defined by the user through bit 5 of the Configuration Register.

The Descriptor Stack in BC mode occupies 256 contiguous words. It may be located anywhere in the non-fixed area of RAM as long as it begins on a 256 word boundary (i. e., HEX 0000, 0700, 1000, XX00, etc.). Each Descriptor Block is four words long; the fourth word of each block is loaded by the user with the address of the message to be transferred onto the 1553 bus.

Each data block should be formatted as shown in figure 11. The first word of the message is the Control Word (see figure 12). The message may be stored anywhere in the non-fixed area of RAM, so long as each individual block does not cross a 256 word boundary. The BUS-65515 uses an 8 bit counter for the lower byte of the internal Address Counter. As a result, the data block may be stored anywhere in the non-fixed area of RAM, so long as the individual data block does not cross a 256 word boundary. For example, a data block should not begin at word location 04FE if the user plans on storing more than two words in the block. The first word will be stored at 04FE, the second at 04FF, and a third word would be stored at 0400 as a result of the lower byte Address Counter overflowing.

The number of messages to be transferred must be stored in the current area Message Counter location of the RAM in 1's complement (XXFE = 1 message). The user instructs the BUS-65515 to begin transferring the messages by setting bit 1 of the Start/Reset Register to logic "1". The BUS-65515 will then begin transferring the messages in the order in which their starting addresses were placed in the Descriptor Stack (see figure 13).

The BUS-65515 can be instructed to end 1553 bus transactions if any message does not transfer successfully. This is done by setting the STOP-ON-ERROR bit in the Configuration Register. An ERROR interrupt will be generated at that time if enabled by the user.

If desired a BCEOM interrupt can be generated to notify the CPU that the BUS-65515 has completed the transfer of the requested number of messages. The CPU can also request that an EOM interrupt be generated upon completion of each individual message.

While the current group of messages is being processed, the CPU may read or write to the non-current area of RAM in order to set up the next group of messages, or to examine the results of the previous bus transfers.

Once a block of messages has been completed, the user may swap the current and non-current areas and instruct the BUS-65515 to execute the next group of messages. This is done by toggling bit 5 of the Configuration Register and issuing a new BCSTART command.

bit in the Start/Reset Register, the BUS-65515 takes the following actions:

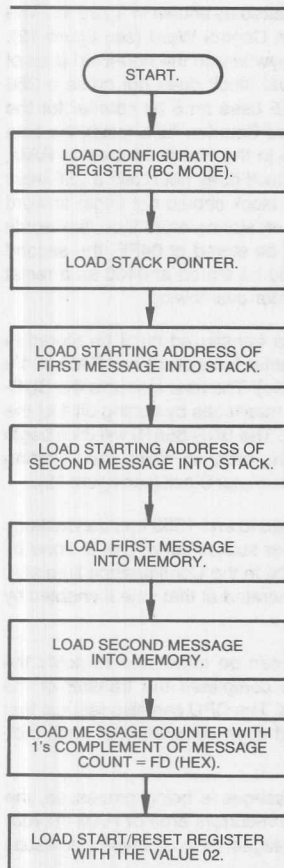
1. Uses Stack Pointer to get the address of the current Descriptor Stack Entry.
2. Sets SOM flag in the Block Status Word to indicate a transfer operation in progress.
3. Stores the Time Tag.
4. Reads the Data Block Address from the fourth location of the Descriptor Stack and transfers the Data Block Address into an internal Address Register.
5. Begins transmission of the message onto the 1553 bus.

Note that data words are transferred to and from memory using the internal Address Register.

**BC EOM SEQUENCE:** Upon completion of a 1553 message, the BUS-65515 takes the following action:

1. Reads the Stack Pointer to get the address of the current Descriptor Stack Entry.
2. Updates the Block Status Word by resetting the SOM and setting EOM and any error bits.
3. Updates the Time Tag.
4. Increments the contents of the Stack Pointer by four and increments the Message Counter by one.
5. Additional messages are transmitted.
6. Generates a BCEOM interrupt if enabled and no further messages are to be transmitted.

Note that if an error is received and STOP ON ERROR is set, the BUS-65515 stops issuing commands over the 1553 bus. The Stack Pointer will point to the next message to be transmitted.



**FIGURE 10A.**  
BC SET-UP EXAMPLE FOR  
TWO MESSAGE TRANSFER

**GIVEN:**

All values are in HEX.

1. Stack area A is used and is located from address 0000 to address 01FF.
2. Message number 1 is located at address 0280.
3. Message number 2 is located at address 0300.

POKE 2003, 0F Initialize Configuration Register.  
 POKE 0200, 00 Initialize Stack Pointer.  
 POKE 0201, 00  
 POKE 0006, 40 Load address of message number 1 into Stack.  
 POKE 0007, 01  
 POKE 000E, 80 Load address of message number 2 into Stack.  
 POKE 000F, 01  
 POKE 0280, 80 Load Control Word.  
 POKE 0281, 00  
 POKE 0282, 21 Load Command Word 0C21.  
 POKE 0283, 0C  
 POKE 0300, 00 Load Control Word.  
 POKE 0301, 00  
 POKE 0302, 23 Load Command Word 1823.  
 POKE 0303, 18  
 POKE 0304, 11 Load Data Word number 1.  
 POKE 0305, 11  
 POKE 0306, 22 Load Data Word number 2.  
 POKE 0307, 22  
 POKE 0308, 33 Load Data Word number 3.  
 POKE 0309, 33  
 POKE 0202, FD Load Message Counter.  
 POKE 2006, 02 Start Transfer.

**FIGURE 10B.** BC SET-UP WRITTEN IN BASIC

0001	0000 (CPU ADDRESS)
01	40
01	80
	0280
00	80
0C	21
*	*
*	*
*	*
	0300
00	00
18	23
11	11
22	22
33	33
*	*
*	*

\*Left empty for RTU's response.

**FIGURE 10C.**  
BC SET-UP MEMORY MAP



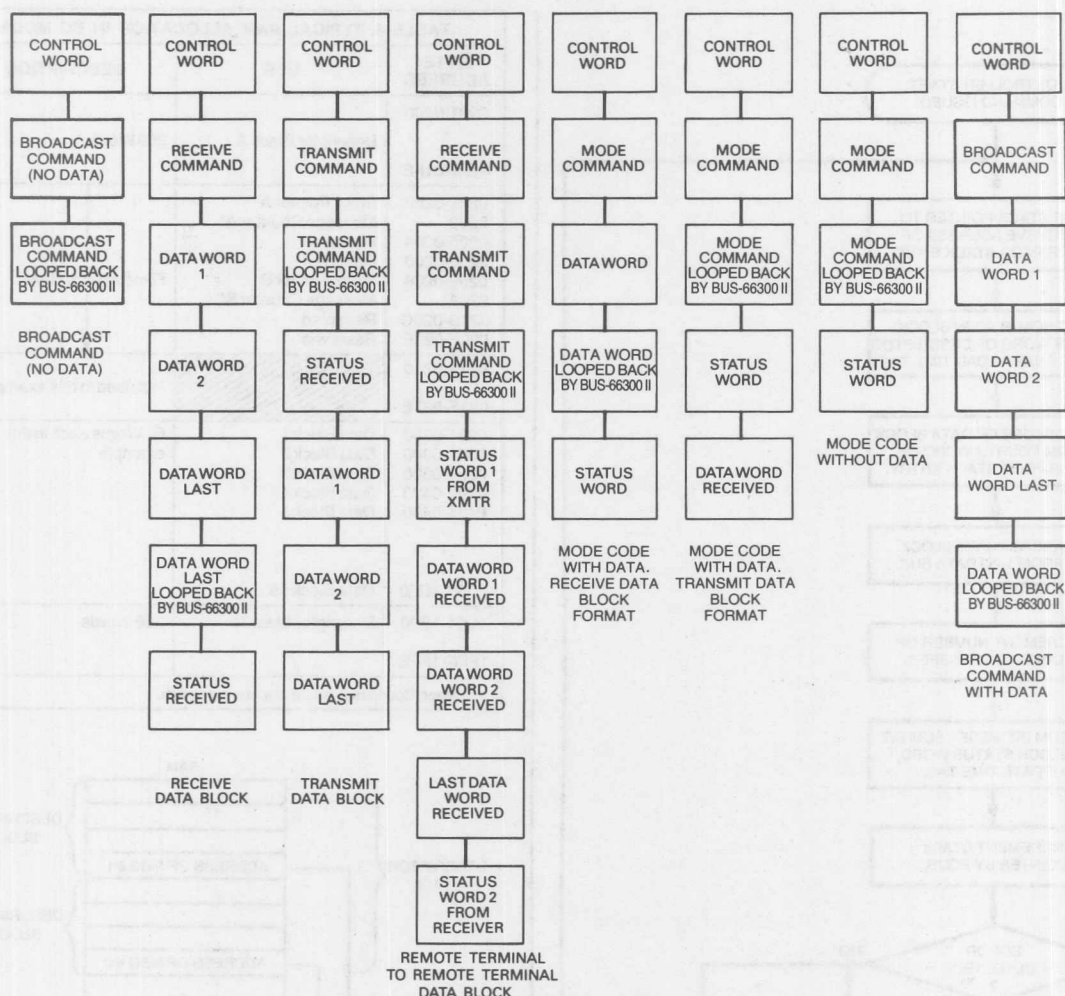


FIGURE 11. BC DATA BLOCK FORMATS

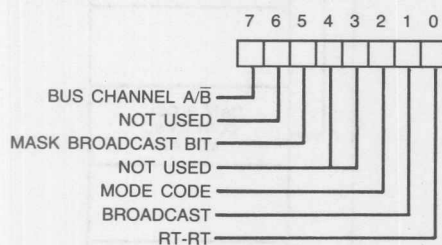
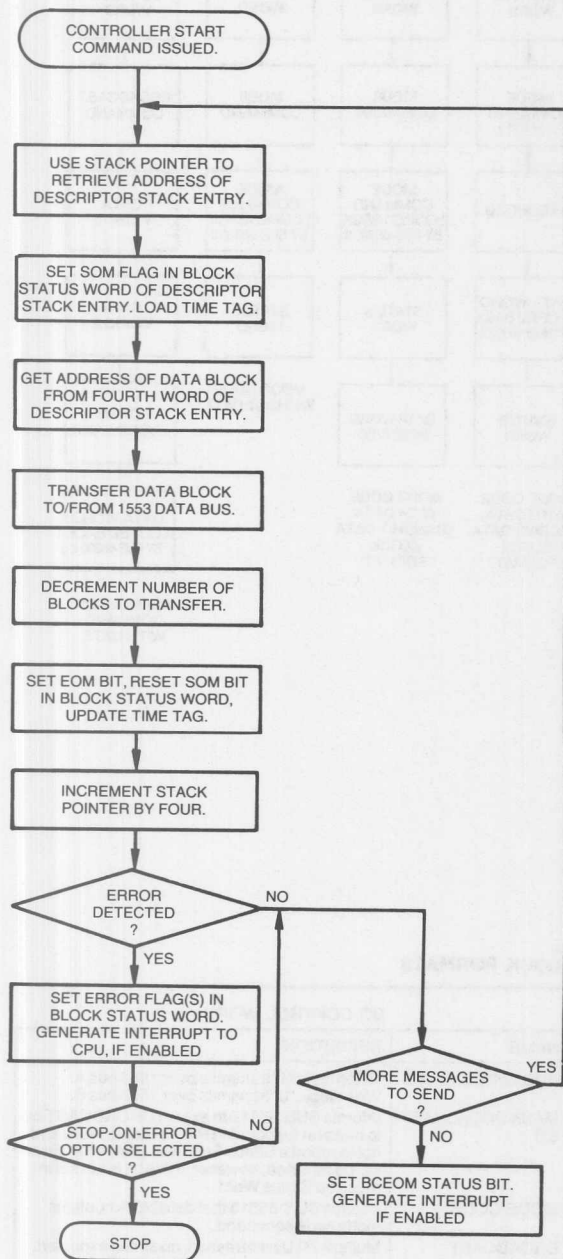


FIGURE 12. BC CONTROL WORD

BC CONTROL WORD	
NAME	DEFINITION
BUS CHANNEL A/B	When logic "1" transmits over 1553 bus A. When logic "0" transmits over 1553 bus B.
MASK BROADCAST BIT	Informs BUS-65515 to expect BROADCAST bit to be set in responding RTU's Status Word and not to report a Status Set Error. Status Set Error will be reported, however, if this bit is not set in received Status Word.
MODE CODE	Informs BUS-65515 that data block contains mode code command.
BROADCAST RT-RT	Multiple RTUs addressed, no status expected. Informs BUS-65515 that data block contains RT-RT message transfer.



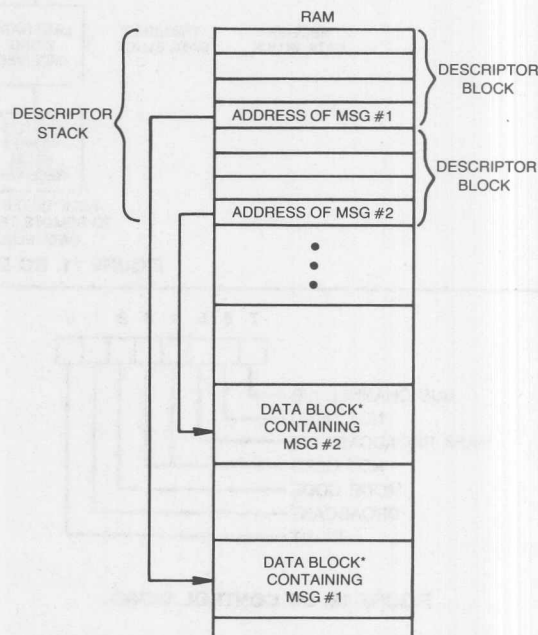


**FIGURE 14. BC SEQUENCE OF OPERATION  
(UNDER BUS-65515 CONTROL)**

**TABLE 4. TYPICAL RAM ALLOCATION IN BC MODE**

BYTE ADDRESS	USE	DESCRIPTION
0001-0000 : 01FF-01FE	Descriptor Stack A	256 Words
0201-0200 0202 0205-0204 0207-0206 0209-0208 020A 020D-020C 020F-020E	Stack Pointer A Message Counter A* Reserved Reserved Stack Pointer B Message Counter B* Reserved Reserved	Fixed Area of RAM
0211-0210 : 027F-027E		
0281-0280 0301-0300 0381-0380 0401-0400 0481-0480 : : 1D81-1D80	Data Block 1 Data Block 2 Data Block 3 Data Block 4 Data Block 5 : : Data Block 55	64 Words each in this example.
1E01-1E00 : 1FFF-1FFE	Descriptor Stack B	256 Words

\*Message Counters A and B are one byte each.



\*DATA BLOCKS NEED NOT BE CONTINUOUS AND MAY BE OF WHATEVER LENGTH IS SUFFICIENT TO HOLD THE PARTICULAR MESSAGE

**FIGURE 13. ORDERING MESSAGES IN BC MODE**

## RTU MODE

The RTU mode is selected by issuing a RESET command and setting bits 7 and 6 of the Configuration Register to logic "1" and "0", respectively. The RTU Address of the BUS-65515 is defined by loading the desired value into the RTU Address Register. Note that bit 5 of the RTU Address Register must be programmed to implement odd parity.

**RTU INITIALIZATION.** For RTU operation, the user initializes the RAM, Stack Pointer, Look-Up Tables, and data to be transmitted to the BC. Table 5 lists a sample memory map for the RTU mode. The user follows the steps shown in Figure 15, RTU Initialization.

The BUS-65515 uses an indirect addressing architecture to determine where to store or retrieve the data required to service the commands received from the BC. The Stack Pointer indicates which block in the Descriptor Stack to use. The fourth word of the Descriptor Stack is used to store the received command word.

The  $\overline{T/R}$  bit and the subaddress field of the command word will then be used to generate a pointer into the Look-Up Table, which contains the starting address of the data block to be used for transmitting or receiving information for the particular subaddress.

Two Stack Pointers, two Descriptor Stacks, and two Look-Up Tables are provided to allow the user to double buffer the RAM. All transfers to and from the 1553 Bus are made using the current Stack and Look-Up Tables as defined by the user through bit 5 of the Configuration Register.

The Stack Pointer should be initialized by the CPU with the starting address of the Descriptor Stack. This pointer must contain a word address (i.e., if the Stack is to begin at HEX bytes 0401-0400, the Stack Pointer should be initialized to 0200).

In the RTU mode, the Descriptor Stack occupies 256 contiguous words. It may be located anywhere in the non-fixed area of RAM, beginning a 256 word boundary (i.e., HEX 0000, 0700, 1000, XX00, etc.).

The Look-Up Table is loaded by the user with the addresses of the data blocks to be used for receiving or transmitting data from the particular subaddress. The first 32 words of each Look-Up Table should contain the word address of the data blocks to be used when receiving data. The next 32 words should contain the address to be used when transmitting data from the various subaddresses.

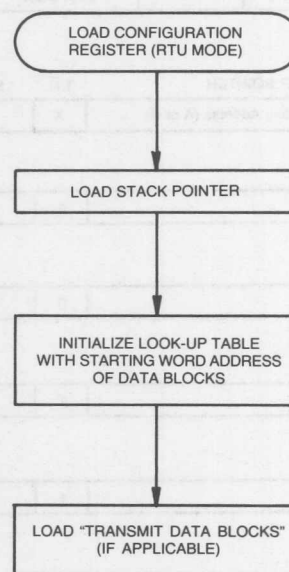
The Look-Up Table is sequentially ordered so that the first location refers to  $\overline{T/R} = 0$ , Subaddress = 0000. The second location refers to  $\overline{T/R} = 1$  and Subaddress = 0001. The last location within the Look-Up Table refers to  $\overline{T/R} = 1$  and Subaddress = 1111 (see figures 16 and 17).

**RTU SOM SEQUENCE.** When a 1553 command is received, the BUS-65515 saves the command received in an internal register. Figure 18 illustrates the RTU Sequence of Operation once a 1553 command word is received. Once the command word is received, the BUS-65515 performs the following steps:

1. Reads the Stack Pointer to get the address of the current Descriptor Stack Entry.
2. Stores an SOM flag in the Block Status Word to indicate a transfer operation in progress.
3. Stores the Time Tag.
4. Stores the Command Word received.
5. Reads a Block address from the Look-Up Table using the  $\overline{T/R}$  bit and the subaddress from the Command Word; transfers the Block address into an internal address register.

**RTU EOM SEQUENCE.** At the end of a 1553 message (valid or invalid), the BUS-65515 performs the following steps:

1. Updates the Block Status Word by resetting the SOM and setting the EOM and any error bits.
2. Updates the Time Tag.
3. Increments the Stack Pointer by four.
4. Generates an Error Interrupt if enabled.



**FIGURE 15. RTU INITIALIZATION (UNDER USER CONTROL)**

BYTE ADDRESS	USE	DESCRIPTION	BYTE ADDRESS	USE	DESCRIPTION
0001-0000 ⋮ 01FF-01FE	Descriptor Stack A	256 Words	0301-0300 033F-03FE 0341-0340 037F-037E	Data Block 1 Data Block 2	32 Words in this example.
0201-0200 0203-0202 0205-0204 0207-0206 0209-0208 020B-020A 020D-020C 020F-020E	Stack Pointer A Reserved Reserved Reserved Stack Pointer B Reserved Reserved Reserved	↑ Fixed Area of RAM ↓	0381-0380 ⋮ 03FF-03FE	Look-Up Table B	↑ Fixed Area of RAM ↓
0211-0210 ⋮ 027F-027E		Unused in this example.	0401-0400 ⋮ 1EC1-1EC0 1EEF-1EE0	Data Block 3 ⋮ Data Block 97	
0281-0280 ⋮ 02FF-02FE	Look-Up Table A	↑ Fixed Area of RAM ↓	1F01-1F00 ⋮ 1FFF-1FFE	Descriptor Stack B	256 Words

# COMMAND WORD RECEIVED

RTADR	T/R	SUBADDR	WORD COUNT
-------	-----	---------	------------

LOOK-UP POINTER	T/R	Subaddress	0
Base Address (A or B)	X	XXXXX	0

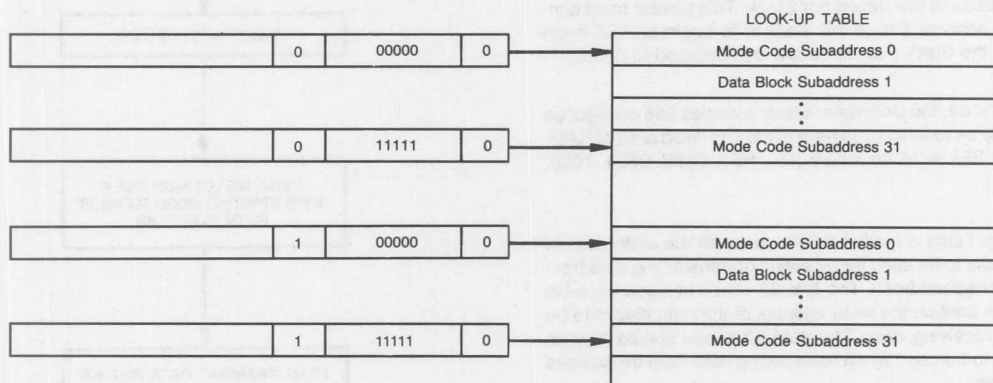


FIGURE 16. LOOK-UP TABLE SET-UP

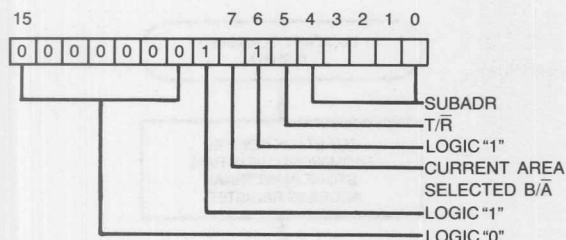


FIGURE 17. LOOK-UP TABLE POINTER

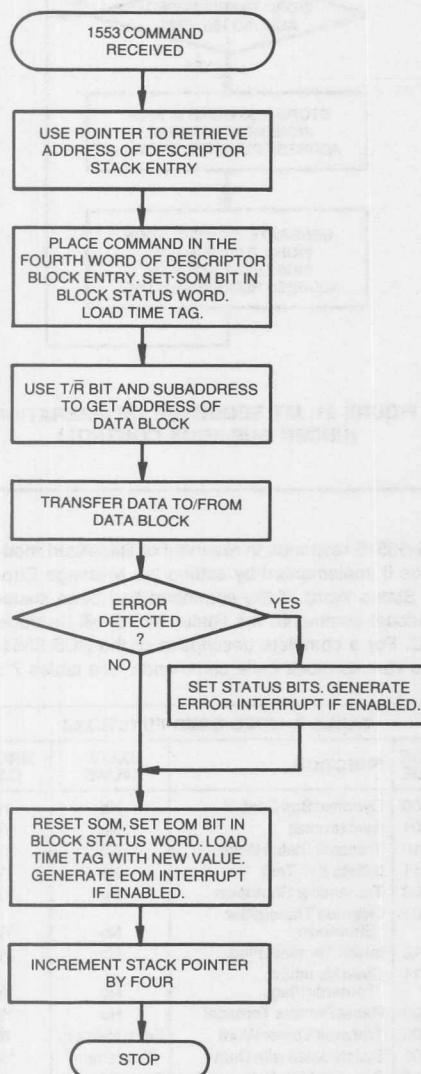


FIGURE 18. RTU SEQUENCE OF OPERATION  
(UNDER BUS-65515 CONTROL)

## MT MODE

The MT mode is selected by setting bit 7 of the Configuration Register to logic "0" and bit 6 to a logic "1".

**MT INITIALIZATION.** For MT operation, the user initializes the RAM as shown in table 6 and follows the steps shown in figure 19, MT Initialization.

The entire RAM is used as the MT stack. The user instructs the BUS-65515 where to store the first Identification Word by loading the starting word address in word 100 HEX of RAM.

To initiate reception of the 1553 bus traffic, the user issues a CONTROLLER START command by setting bit 1 of the Start/Reset Register to a logic "1". This causes the BUS-65515 to load the contents of either Stack Pointer A or B (as selected by the Configuration Register) into an internal address register. Once a word is received from the 1553 bus, the BUS-65515 stores this word at the address indicated by the internal address register. The contents of this register are then incremented by one to point to the next word in RAM.

The BUS-65515 generates an Identification Word for the received word and stores it in the RAM location indicated by the internal address register. The Address Register is again incremented, in preparation for storing the next 1553 word. The RAM automatically wraps around from FFFF to 0000.

The Identification Word is generated by the BUS-65515 in order to provide the CPU with additional information regarding the received 1553 word (see figure 20).

It is recommended that the user reset bit 7 of the Identification Word each time it reads the associated data word into CPU memory. This provides a simple method of keeping track of which words have already been processed by the CPU. For additional information on the use of MT mode, consult the factory.

TABLE 6. TYPICAL RAM ALLOCATION IN MT MODE

BYTE ADDRESS	DESCRIPTION
0001-0000	First Identification Word.
0003-0002	First Received 1553 Word.
0005-0004	Second Identification Word.
0007-0006	Second Received 1553 Word.
.	
.	
1FFF-1FFE	Word stored at FFFF followed by word stored at 0000.
.	
.	
0201-0200	Stack Pointer* A (Fixed area of RAM)
0209-0208	Stack Pointer B (Fixed area of RAM)

\*Stack Pointers are read by the BUS-65515 upon executing a BCSTART command. It is overwritten by data in the course of acting as a MT.

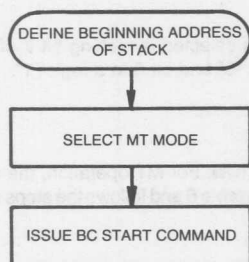
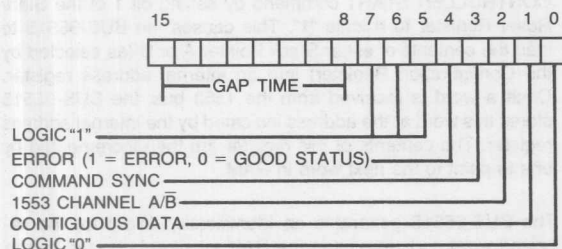


FIGURE 19. MT INITIALIZATION (UNDER USER CONTROL)



Note: Each bit of the GAP TIME field represents 0.5  $\mu$ s.

FIGURE 20. MT IDENTIFICATION WORD

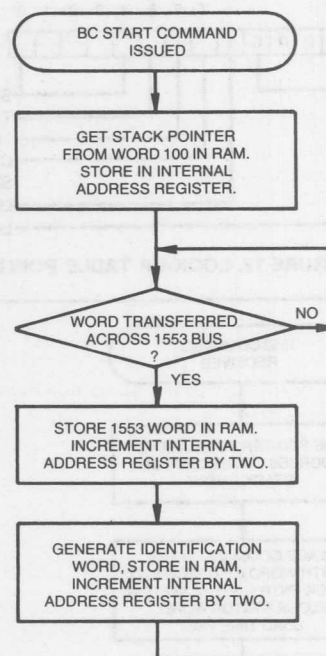


FIGURE 21. MT SEQUENCE OF OPERATION (UNDER BUS-65515 CONTROL)

## MODE CODES

The BUS-65515 supports all 1553B mode codes for dual redundant systems. Note that a Reset mode code command does not have the same effect as issuing a RESET command (setting bit 1 of the Start/Reset Register). A mode code Reset command will override the Inhibit TF Flag, reset the Time Tag Register, and override the Transmitter Shutdown condition if instructed to do so through the user programmable PROM.

A mode code with an associated data word and a T/R bit set to "0" is handled the same as a receive operation. In the RTU mode, the T/R bit and the subaddress field are used as pointers into the Look-Up Table. Thus, the 1st and 31st entries of the Look-Up Table should contain the address of the word in RAM to be used for receiving data associated with the Synchronize with Data mode code command. Note that these entries correspond to a T/R bit equal to "0" and a subaddress field of 00000 or 11111.

The mode code command Transmit Vector word is handled in a similar manner. Look-Up Table entries 32 and 63 (T/R bit = 1 and a subaddress field of 00000 or 11111) should point to the location in RAM containing the user defined Vector Word.

The BUS-65515 maintains separate registers containing the last received Command Word and Status Word, along with the BIT Word. It will automatically transmit these words to the BC when it receives a mode code command instructing it to do so.

The BUS-65515 responds to reserved or illegalized mode code commands if implemented by setting the Message Error bit in its 1553 Status Word. If the command had been issued as a non-broadcast command, the Status Word will be transmitted to the BC. For a complete description of the BUS-65515's response to various mode code commands, see tables 7 and 8.

TABLE 7. MODE CODE FUNCTIONS

T/R BIT	MODE CODE	FUNCTION	DATA WORD	BROADCAST
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	Yes
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag	No	Yes
1	00111	Override Inhibit Terminal Flag	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	10000	Transmit Vector Word	From Memory	No
0	10001	Synchronize with Data	To Memory	Yes
1	10010	Transmit Last Command	From Internal Register	No
1	10011	Transmit Bit Word	From Internal Register	No



TABLE 8. MODE CODES

## DYNAMIC BUS CONTROL (00000)

### MESSAGE SEQUENCE = DBC \* STATUS

The BUS-65515 responds with status. If the subsystem wants control of the bus, it must set DBACC within 2.5 $\mu$ s after  $\overline{\text{NBGR}}\overline{\text{T}}$ .

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

## SYNCHRONIZE WITHOUT DATA WORD (00001)

### MESSAGE SEQUENCE = SYNC \* STATUS

The BUS-65515 responds with status. If sent as a broadcast, the broadcast receive bit will be set and status response suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

## TRANSMIT STATUS WORD (00010)

### MESSAGE SEQUENCE = TRANSMIT STATUS \* STATUS

The status and BIT word registers are not altered by this command and contain the resulting status from the previous command.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

## INITIATE SELF-TEST (00011)

### MESSAGE SEQUENCE = SELF-TEST \* STATUS

The BUS-65515 responds with a status word. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Short-loop test is initiated on the status word transmitted. If the test fails, an RT fail flag is generated.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).
5. **Faulty Test.** Bits set: terminal flag (SW), A/B Loop Test Fail, Current 1553 Bus (A or B) Loop Test Fail (BIT Word).

## TRANSMITTER SHUTDOWN (00100)

### MESSAGE SEQUENCE = SHUTDOWN \* STATUS

This command is only used with dual redundant bus systems. The BUS-65515 responds with status. At the end of the status transmission, the BUS-65515 inhibits any further transmission from the dual redundant channel. Once shutdown, the transmitter can only be reactivated by Override Transmitter Shutdown or RESET RT commands.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

\* = Status response time

TABLE 6. MODE CODES (CONT'D)

**OVERRIDE TRANSMITTER SHUTDOWN (00101)****MESSAGE SEQUENCE = OVERRIDE SHUTDOWN \* STATUS**

This command is only used with dual redundant bus systems. The BUS-65515 responds with status. At the end of the status transmission, the BUS-65515 re-enables the transmitter of the redundant bus. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

**INHIBIT TERMINAL FLAG BIT (00110)****MESSAGE SEQUENCE = INHIBIT TERMINAL FLAG \* STATUS**

The BUS-65515 responds with status and inhibits further internal or external setting of the terminal flag bit in the status register. Once the terminal flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT command. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

**OVERRIDE INHIBIT TERMINAL FLAG BIT (00111)****MESSAGE SEQUENCE = OVERRIDE INHIBIT TERMINAL FLAG \* STATUS**

The RTU responds with status and reactivates the terminal flag bit in the status register. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

**RESET REMOTE TERMINAL (01000)****MESSAGE SEQUENCE = RESET REMOTE TERMINAL \* STATUS**

The BUS-65515 responds with status and internally resets. Transmitter shutdown, mode commands, and inhibit terminal flag commands will be reset. If the command was broadcast, the broadcast received bit is set and the status word is suppressed.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

**RESERVED MODE CODES (01001-01111)****MESSAGE SEQUENCE = RESERVED MODE CODES \* STATUS**

The BUS-65515 responds with status. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.

**ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), Illegal Mode Code (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

\* = Status response time

TABLE 8. MODE CODES (CONT'D)

## TRANSMIT VECTOR WORD (10000)

### MESSAGE SEQUENCE = TRANSMIT VECTOR WORD \* STATUS VECTOR WORD

The BUS-65515 transmits a status word followed by a vector word. The contents of the vector word (from the subsystem) are enabled onto DB0-DB15 with BUSREQ after the command transfer (same as data word in a normal transmit command).

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, (BIT Word).

## SYNCHRONIZE WITH DATA WORD (10001)

### MESSAGE SEQUENCE = SYNCHRONIZE DATA WORD \* STATUS

The data word received following the command word is transferred to the subsystem. The status register is then enabled and its contents transferred onto the data bus and transmitted. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), Low Word Count (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), T/R Error, High Word Count (BIT Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), High Word Count, T/R Error (BIT Word).

## TRANSMIT LAST COMMAND (10010)

### MESSAGE SEQUENCE = TRANSMIT LAST COMMAND \* STATUS LAST COMMAND

The status and BIT word registers are not altered by this command. The SW contains the status from the previous command. The data word transmitted contains the previous valid command (providing it was not another TRANSMIT LAST COMMAND).

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

## TRANSMIT BIT WORD (10011)

### MESSAGE SEQUENCE = TRANSMIT BIT WORD \* STATUS BIT WORD

The BUS-65515 responds with status followed by the BIT word. When activated, BITEN allows the subsystem to latch the BIT word on the parallel data bus. The BIT word is not altered by this command; however, the next SW will reflect errors in this transmission.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bit set: message error (SW).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

\* = Status response time

TABLE 8. MODE CODES (CONT'D)

## SELECTED TRANSMITTER SHUTDOWN (10100)

### MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA \* STATUS

The data word received is transferred to the subsystem and status is transmitted. No other action is taken by the BUS-65515. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Intended for use with RTs with more than one dual redundant channel.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count (BIT Word).

## OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101)

### MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA \* STATUS

The data word received after the command word is transferred to the subsystem. No other action is taken by the BUS-65515. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count, T/R Error (BIT Word).

## RESERVED MODE CODES

### MESSAGE SEQUENCE = RESERVED MODE CODE (T/R = 1) \* STATUS

### RESERVED MODE CODE (T/R = 0) \* STATUS

The BUS-65515 responds with status. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

#### ERROR CONDITIONS (T/R = 1)

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

#### ERROR CONDITIONS (T/R = 0)

1. **Invalid Command.** No response, command ignored.
2. **Command not Followed by Contiguous Data Word.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

\* = Status response time



## SELF TEST

The BUS-65515 performs an automatic self test each time a 1553 message is processed. The last word transferred onto the 1553 bus for each message is "looped back" through the transformer and the BUS-65515's receive circuitry. An on-line comparison of the transmitted word and the received looped back word is then performed. If a discrepancy is detected, the Error bit in the Block Status Word is set, the Terminal Flag bit is set in the 1553 Status Word, and an error interrupt is generated to the CPU, if enabled.

In the BC mode, the looped back word is placed in the next sequential location of the message block in the on-board RAM, where it is available for the CPU to inspect. See the data formats in figure 11 for specific 1553 message types.

The BUS-65515 maintains a separate BIT (Built-In-Test) register which contains information regarding the last message transfer (see figure 22). In RTU mode, the contents of this register are automatically passed to the BC in response to a Transmit BIT Word mode code command.

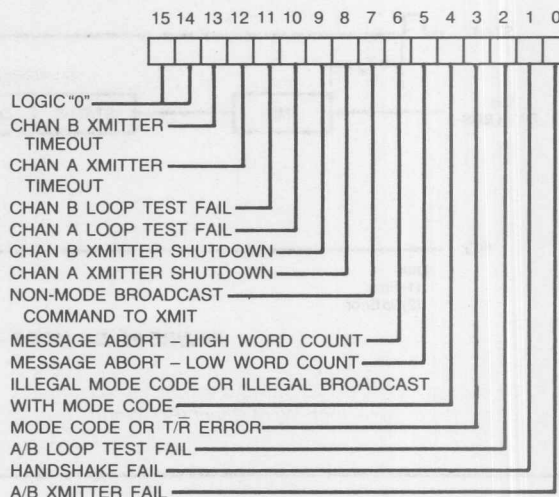


FIGURE 22. BUILT-IN-TEST (BIT) WORD

## BUS-65515 BC AND RTU MODE TIMING

Table 9 defines the times and lists the units for the following 11 timing diagrams.

TIME	DEFINITION	MIN	MAX	UNITS
$T_{st}$	Start timing (start to data on 1553)	3	4	$\mu S$
$T_{ei}$	EOM/Error Interrupt	5	7	$\mu S$
$T_{bi}$	BC EOM Interrupt	10	12	$\mu S$
$T_{ebo}$	EOM/Error Timeout Interrupt	19	21	$\mu S$
$T_{gp}$	Intermessage Gap (Mid parity to mid sync)	16	16	$\mu S$
$T_{gpto}$	Intermessage Gap (Timeout) (Mid parity to mid sync)	24	26	$\mu S$
$T_{rsp}$	Response Time (Mid parity to mid sync)	10	12.5	$\mu S$
$T_{ero}$	RT/RT Timeout Interrupt	19.5	20.5	$\mu S$

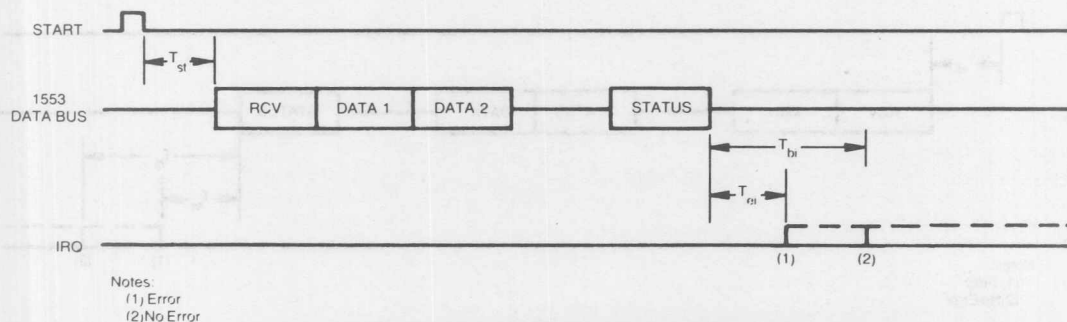
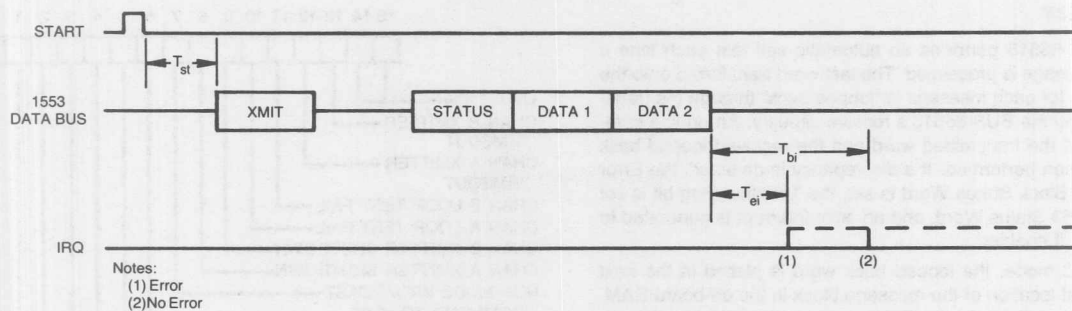
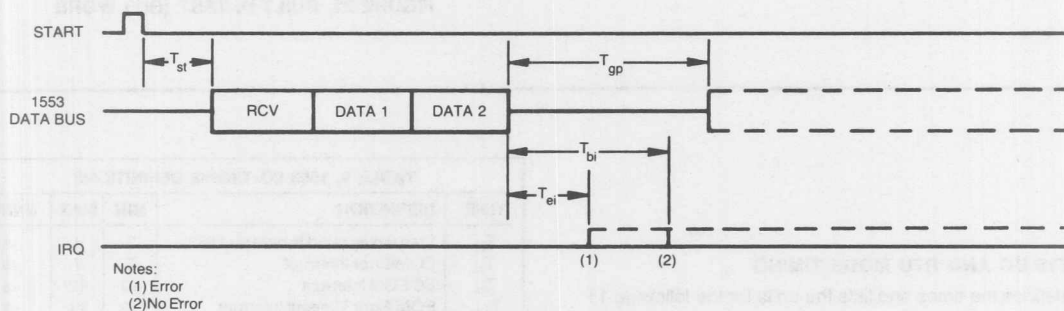


FIGURE 23. BC MODE - RECEIVE COMMAND

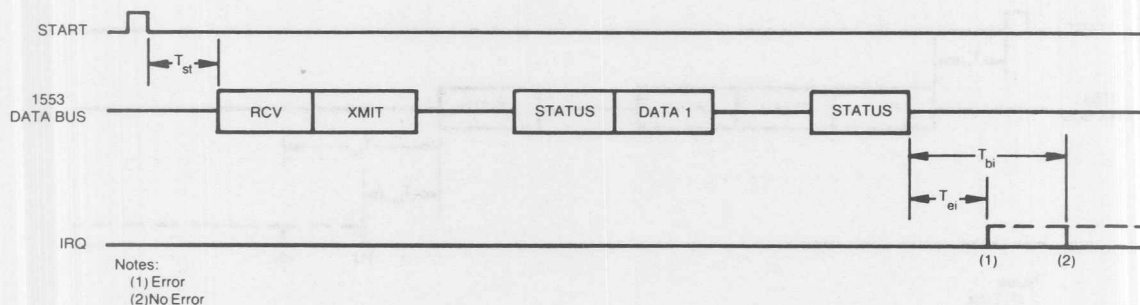




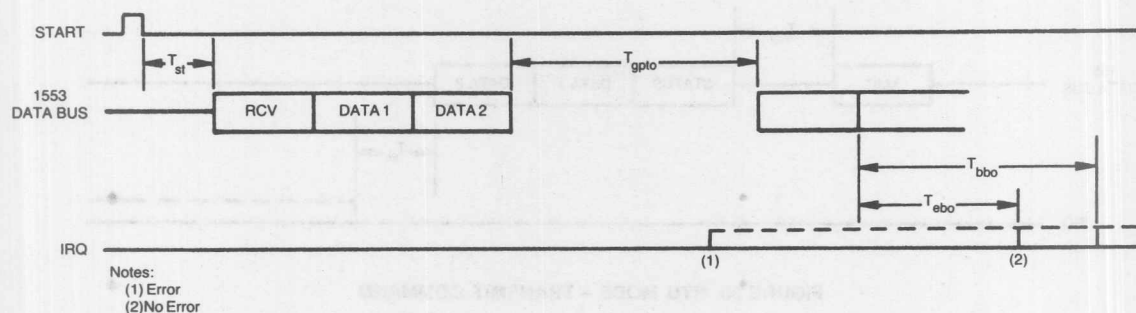
**FIGURE 24. BC MODE - TRANSMIT COMMAND**



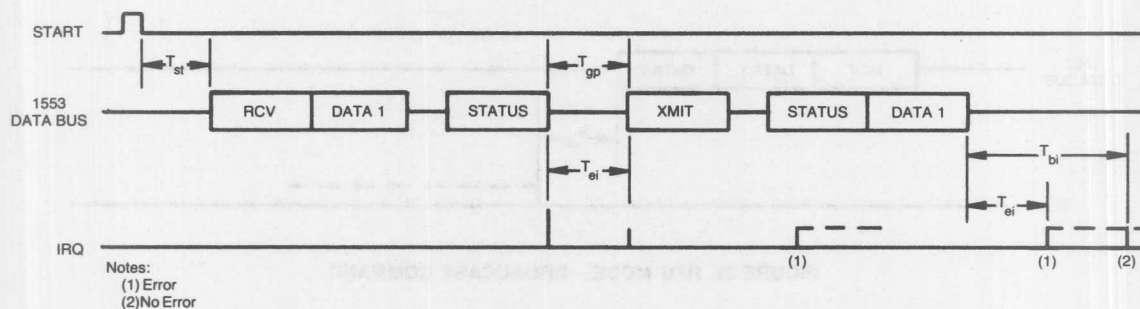
**FIGURE 25. BC MODE - BROADCAST**



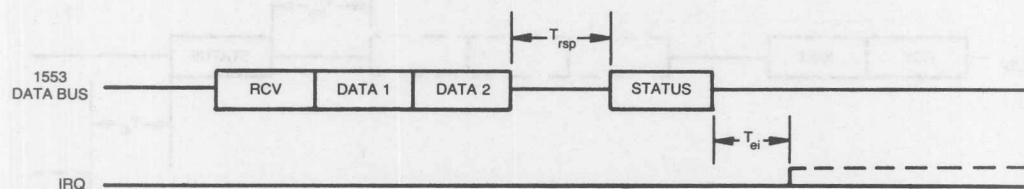
**FIGURE 26. BC MODE - RTU TO RTU TRANSFER**



**FIGURE 27. BC MODE - TIMEOUT**



**FIGURE 28. BC MODE - TWO COMMANDS**



**FIGURE 29. RTU MODE - RECEIVE COMMAND**

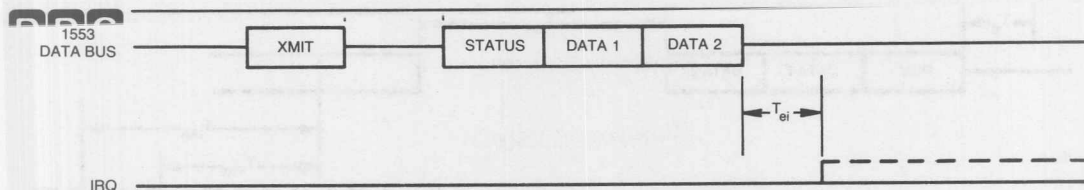


FIGURE 30. RTU MODE – TRANSMIT COMMAND

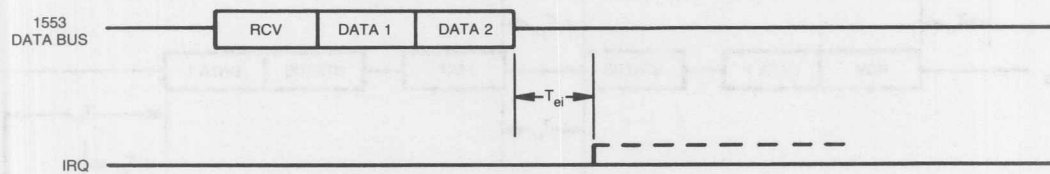


FIGURE 31. RTU MODE – BROADCAST COMMAND

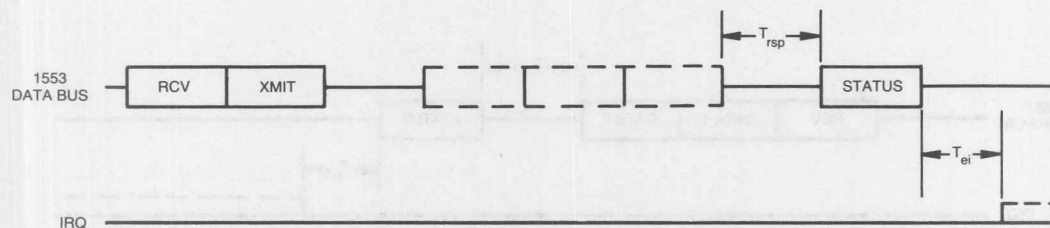
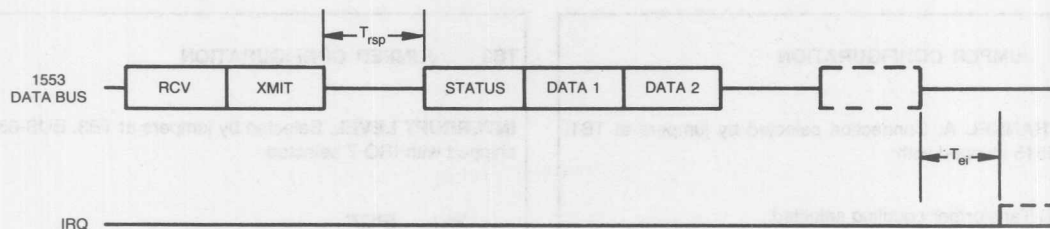
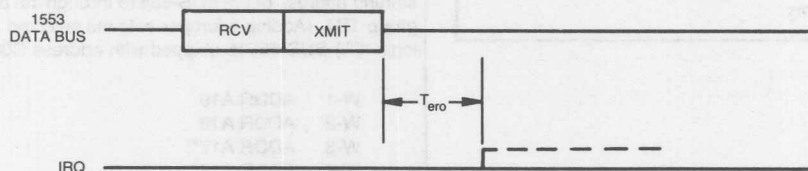


FIGURE 32. RTU MODE – RT/RT RECEIVE



**FIGURE 33. RTU MODE - RT/RT TRANSIT**



**FIGURE 34. RTU MODE - RT/RT TIMEOUT**

## INSTALLATION

The BUS-65515 is designed to work with an IBM PC, PCXT, and PCAT (8 bit slot) computer. Consult factory for use with IBM PC compatibles and clones.

**POWER SUPPLY.** Verify that the power supply in the user's PC is sufficient to drive the BUS-65515 in conjunction with any other peripheral boards being used.

**1553 COUPLING.** The BUS-65515 can be direct coupled or transformer coupled to the 1553 bus. The user selects the type of coupling desired through the on-board jumper groups TB1 and TB2. The BUS-65515 comes equipped with two Bulkhead

connectors, Trompeter part no. BJ77 and mating connector Trompeter Cable Plug, part no. PL-75N.

**INITIALIZATION.** The user must select a used area of memory based on the particular system configuration. An on-board segment decoder is connected to bits A16-A19. A1-A13 define the on-board RAM within the selected segments; bits A14-A15 are not used.

**INTERRUPT PRIORITY SELECTION.** The BUS-65515 generates a standard interrupt, as per IBM PC Bus standards, to inform the user of a variety of events. The user may set this interrupt to occur on 1 of 6 priority levels, (IRQ 2-7), through the on-board jumper group TB3. (Adding a jumper selects the designated interrupt level.)

## TB1 JUMPER CONFIGURATION

**1553 CHANNEL A.** Connection selected by jumpers at TB1. BUS-65515 shipped with:

- (1) Transformer coupling selected.
- (2) Frame floating.
- (3) Receiver enabled always.

W-1	DC COUPLED +
W-2	XFM COUPLED +*
W-3	FRAME TO GROUND
W-4	XFM COUPLED -*
W-5	DC COUPLED -
W-6	RCVRENABLED ALWAYS*
W-7	RCVR ENABLED BY RTADDR REG

Notes: (1) W-6 and W-7 must not be installed at the same time.  
(2) W-6 overrides software control of receiver.  
\*Installed by factory.

## TB2 JUMPER CONFIGURATION

**1553 CHANNEL B.** Connection selected by jumpers at TB2. BUS-65515 shipped with:

- (1) Transformer coupling selected.
- (2) Frame floating.
- (3) Receiver enabled always.

W-1	DC COUPLED +
W-2	XFM COUPLED +*
W-3	FRAME TO GROUND
W-4	XFM COUPLED -*
W-5	DC COUPLED -
W-6	RCVRENABLED ALWAYS*
W-7	RCVR ENABLED BY RTADDR REG

Notes: (1) W-6 and W-7 must not be installed at the same time.  
(2) W-6 overrides software control of receiver.  
\*Installed by factory.

## TB3 JUMPER CONFIGURATION

**INTERRUPT LEVEL.** Selected by jumpers at TB3. BUS-65515 shipped with IRQ 7 selected.

W-1	IRQ7*
W-2	IRQ 6
W-3	IRQ 5
W-4	IRQ 4
W-5	IRQ 3
W-6	IRQ 2

Note: \*Installed by factory.

## TB4 JUMPER CONFIGURATION

**BUS-65515 ADDRESS.** The BUS-65515 is memory mapped to the CPU. The user may select the upper bits, (A14-A19), of the starting address of the BUS-65515 through the on-board jumper group TB4. (Adding a jumper sets the selected address bit to a logic "0".) BUS-65515 shipped with address C000 selected.

W-1	ADDR A19
W-2	ADDR A18
W-3	ADDR A17*
W-4	ADDR A16*
W-5	ADDR A15*
W-6	ADDR A14*
W-7	NOT USED

Note: A14 and A15 can permit memory mapping segment selections to C000, CC00, C800, and C200.

Note: \*Installed by factory.

## INSTALLATION NOTES

1. To use transformer coupling on Channel A, install jumpers across TB1 pins W2, W3, and W4. Remove jumpers W1 and W5.
2. To use transformer coupling on Channel B, install jumpers across TB2 pins W2, W3, and W4. Remove jumpers W1 and W5.
3. To use direct coupling on Channel A, install jumpers across TB1 pins W1, W3, and W5. Remove jumpers W2 and W4.
4. To use direct coupling on Channel B, install jumpers across TB2 pins W1, W3, and W5. Remove jumpers W2 and W4.

It is recommended that the user install a jumper across TB1, pin W6 and TB2 pin W6. A jumper *should not* be installed across TB1 pin W7 and TB2 pin W7.

The jumper connecting pin W6 across TB1 enables the receivers on the 1553 bus and insures the BUS-65515 is capable of receiving data from the bus.

If the jumper connecting pins 6-9 W-7 on TB1 is installed, then the receivers will be controlled by bit 7 of the RTU Address Register. (A logic "1" enables the receivers and a logic "0" disables them). The transmitters are enabled regardless of the selection of bit 7 or the jumper installation.



TABLE 10. BUS-65515 PIN FUNCTIONS

PIN	SIGNAL NAME	DESCRIPTION
A1	IO CHCK	Not Used
A2	D7	Data Bit 7 (MSB)
A3	D6	Data Bit 6
A4	D5	Data Bit 5
A5	D4	Data Bit 4
A6	D3	Data Bit 3
A7	D2	Data Bit 2
A8	D1	Data Bit 1
A9	D0	Data Bit 0
A10	IO CHR DY	I/O Ready
A11	AEN	Address Enable
A12	A19	Address Bit 19 (MSB)
A13	A18	Address Bit 18
A14	A17	Address Bit 17
A15	A16	Address Bit 16
A16	A15	Address Bit 15
A17	A14	Address Bit 14
A18	A13	Address Bit 13
A19	A12	Address Bit 12
A20	A11	Address Bit 11
A21	A10	Address Bit 10
A22	A9	Address Bit 9
A23	A8	Address Bit 8
A24	A7	Address Bit 7
A25	A6	Address Bit 6
A26	A5	Address Bit 5
A27	A4	Address Bit 4
A28	A3	Address Bit 3
A29	A2	Address Bit 2
A30	A1	Address Bit 1
A31	A0	Address Bit 0

TABLE 10. BUS-65515 PIN FUNCTIONS (Cont.)

PIN	SIGNAL NAME	DESCRIPTION
B1	GND	Signal Ground
B2	RESET	Reset
B3	+5V	Logic Power Supply
B4	IRQ2	Interrupt Request 2
B5	-5V	Not Used
B6	DRQ2	Not Used
B7	-12V	System Power Supply
B8	Not Used	Not Used
B9	+12V	System Power Supply
B10	GND	Signal Ground
B11	-MEMW	Memory Write
B12	-MEMR	Memory Read
B13	-IOW	Not Used
B14	-IOW	Not Used
B15	-DACK3	Not Used
B16	DRQ3	Not Used
B17	-DACK1	Not Used
B18	DRQ1	Not Used
B19	-DACK0	Not Used
B20	CLK	Not Used
B21	IRQ7	Interrupt Request 7
B22	IRQ6	Interrupt Request 6
B23	IRQ5	Interrupt Request 5
B24	IRQ4	Interrupt Request 4
B25	IRQ3	Interrupt Request 3
B26	-DACK2	Not Used
B27	T/C	Not Used
B28	ALE	Address Latch Enable
B29	+5V	Logic Power Supply
B30	OSC	Not Used
B31	GND	Signal Ground

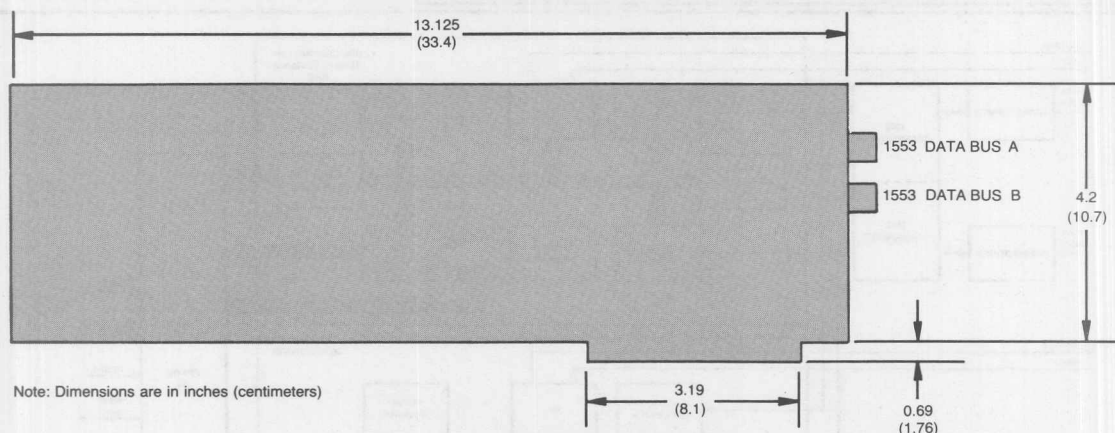


FIGURE 35. BUS-65515 MECHANICAL OUTLINE

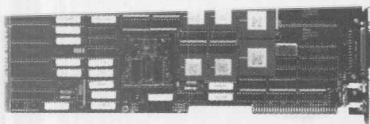
## ORDERING INFORMATION BUS-65515

### SOFTWARE

- Contact factory for free Software
- Contact P.T.I.

For driver and application Software (PC-A/D-D): Mr. Andy Werbach

Phase Two Industries  
1333 Lawrence Expressway  
Suite 418  
Santa Clara, CA 95051  
408-247-1355



# IBM PC COMPATIBLE MIL-STD-1553 SIMULATOR AND TESTER CARD

## PRELIMINARY

### DESCRIPTION

DDC's BUS-65517II is a versatile, full size IBM PC printed circuit card designed for the test and simulation of MIL-STD-1553 systems. It provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553 data bus and the IBM PC. The user friendly software allows the BUS-65517II to simultaneously simulate a Bus Controller (BC), multiple Remote Terminal Units (RTUs), and/or a selectable, triggerable Bus Monitor (MT). The BUS-65517II may be either direct or transformer coupled to an external 1553 bus for use with user provided 1553 devices.

The BC and RTUs evaluate each 1553 message in real-time, determining if any format errors have occurred. Separate registers are maintained for the last command word and the last status word of each emulated RTU. In addition, the user may inject errors into any 1553 message issued by the emulated BC or RTUs. These errors include word count,

bit count, zero crossing, parity, and, in the case of emulated RTUs, response errors (including the setting of any bit within the particular RTU's status word).

The intelligent MT captures the 1553 bus traffic. The user can define when MT operation is to begin and which messages (based on the RTU address, T/R bit, and subaddress) are to be, captured. Monitored information is displayed on a message by message basis.

Operation requires an IBM PC or compatible (with DOS 2.1 or higher), 640K RAM, BUS-65517II card, and DDC provided software. Optional software is available to allow the BUS-65517II RTUs to respond within the timing constraints of MIL-STD-1553A. An optional driver allows the user to control the operation of the BUS-65517II through Turbo Pascal or Microsoft "C". These features make the BUS-65517II an excellent choice for dynamic simulation of MIL-STD-1553B systems.

### FEATURES

- *SIMULATION AND TEST OF MIL-STD-1553 SYSTEMS*
- *SIMULTANEOUS EMULATION OF BC, UP TO 31 RTUs, AND MT*
- *MT MODE RECONSTRUCTS 1553 BUS TRAFFIC*
- *ERROR INJECTION/DETECTION CAPABILITIES*
- *USER FRIENDLY SOFTWARE*
- *OPTIONAL RT PRODUCTION TEST PLAN SOFTWARE*
- *OPTIONAL 1553A RESPONSE AND REAL-TIME DRIVER SOFTWARE AVAILABLE*

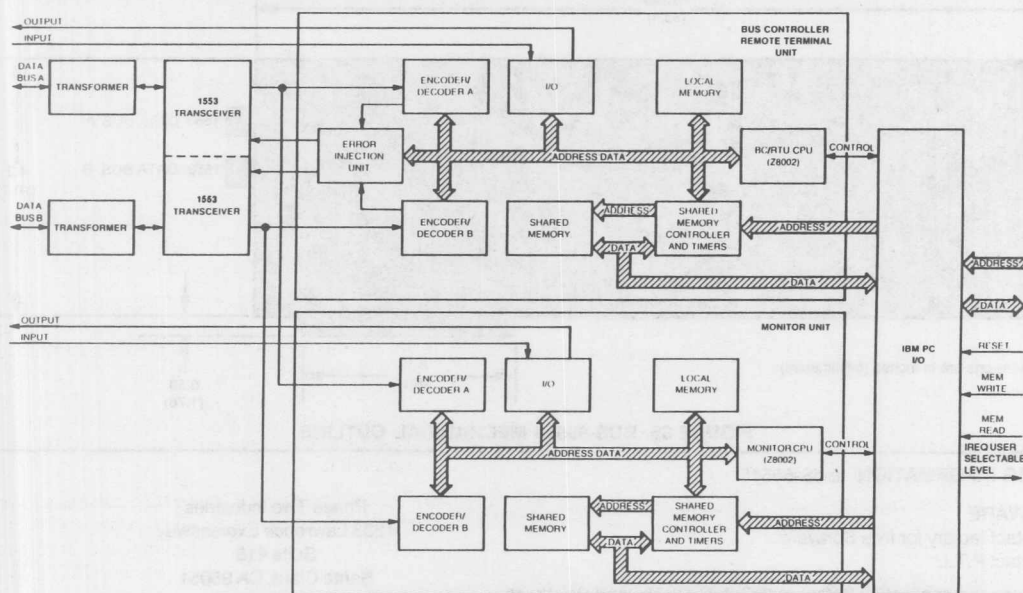


FIGURE 1. BUS-65517II BLOCK DIAGRAM

**TABLE 1. BUS-65517II REQUIREMENTS AND CAPABILITIES**

<b>HARDWARE REQUIREMENTS</b>
IBM PC/XT/AT or Compatible with 640K RAM
DDC's BUS-65517II MIL-STD-1553 Simulator and Tester Card
<b>SOFTWARE REQUIREMENTS</b>
PC DOS 2.1 or higher
DDC's BUS-65517II Software diskette
<b>AVAILABLE OPERATIONS</b>
- Tests and simulates MIL-STD-1553 BC and up to 31 RTUs.
- Provides independent MT mode operation.
- Error injection and detection capabilities.

**TABLE 2. BUS-65517II HARDWARE SPECIFICATIONS**

PARAMETER	UNITS	VALUE	
		Idle	Max*
<b>POWER SUPPLIES</b>			
+5 V Supply Current Drain	A	1.5	1.6
-5 V Supply Current Drain	mA	10	11
+12V Supply Current Drain	mA	200	520
-12 V Supply Current Drain	mA	10	11
<b>TEMPERATURE RANGE</b>			
Operating (Case)	°C	0 to 50	
Storage	°C	-65 to 150	
<b>PHYSICAL CHARACTERISTICS</b>			
Size (Full size IBM PC card; requires one full size, 8 or 16 bit slot)	in (cm)	4.5 x 13.5 x 0.44 (11.4 x 34.3 x 1.1)	

\*(100% Duty Cycle)

## GENERAL

The BUS-65517II allows an IBM PC to simultaneously simulate a MIL-STD-1553 BC, multiple (up to 31) RTUs, and an intelligent MT. The BUS-65517II may be either direct or transformer coupled to a dual redundant external 1553 bus, for operation with user provided 1553 devices. The BUS-65517II is memory mapped (uses a half segment in PC RAM) and interrupt selectable via jumpers on the board.

Full error detection features are provided in all modes of operation. In addition, user specified errors – including bit count, Manchester II errors – may be injected in both BC and any of the emulated RTU modes.

Operation of the BUS-65517II is controlled by user friendly software. The software flags the user if an attempt is made to enter an incorrect value and displays valid responses automatically. Figure 2 illustrates the BUS-65517II Menu Tree.

The three BUS-65517II operating modes are.

1. SETUP
2. RUN
3. DISPLAY COMMUNICATION STACK

Complete operating instructions are detailed in the BUS-65517II Manual.

## SETUP MODE

The SETUP menus define the BUS-65517II as a BC, one or more RTUs, and a selectable triggerable MT. No real-time activity is performed in this mode. Through menu screens, the user specifies what errors (if any) are to be injected into the messages issued by the BC, or within the response(s) (data or status words) of the emulated RTUs.

**BUS CONTROLLER MODE.** The BC mode is programmed through a series of hierarchical menus. Up to 250 different messages may be defined at one time. The user defines these messages by overriding the default values in the SETUP/BC/MESSAGE menu (shown in figure 3).

Error conditions may be injected into any of the messages by placing the cursor over the error field. Once an error has been selected, menus prompt for additional information regarding the error (number of bits, length of error, position of error, etc...).

The following errors may be injected:

### Length Errors.

Word Count: -32 to +1 words can be injected

Bit Count: +2, +1, -2, or -1 bits can be injected in any word of the message

### Encoding Errors.

Glitch: Forces the output of the Manchester Encoder to equality for the user specified time period (in 50 ns increments).

Inverse: Exchanges the output of the Manchester Encoder for the user specified time period (in 50 ns increments).

**Gap Errors.** The user can insert a gap of 3 or 4us (bus dead time) before any word of the message.

**REMOTE TERMINAL MODE.** The BUS-65517II can be programmed to emulate up to 31 unique RTU addresses. The SETUP/RT menu is shown in figure 4. The BUS-65517II dynamically examines each message and determines the appropriate response for each emulated RTU (clear response, suppress status word and set message error bit, etc...). Additionally the user can force any bit of a particular RTU's status word to be set to logic 1. All errors available in the BC mode can be injected along with the following response errors:

No response on Bus A, Bus B, or both busses.

Late response (12 to 30 μs).

Respond on the alternate bus.

**BUS MONITOR MODE.** The BUS-65517II contains an independent MT which reconstructs monitored bus traffic and flags detected errors for user analysis. Figure 5, Communications Stack, illustrates how this information is displayed.

The BUS-65517II MT mode performs three stages of MT operation. The **first stage monitors** all messages received from the bus. The **second stage stores** the selected messages in an on-card circular buffer. The **third stage transfers** the contents of the circular buffer to the Communication Stack located in the PC'S system RAM. By default, the BUS-65517II software will use all available RAM for the Communication Stack; if desired, stack size may be limited.

The first stage listens to both busses until a command is detected. It then receives exclusively from the active bus until the message is completed or invalidated. The second and third stages are programmed by the two MT menu options, SELECTION and CAPTURE.

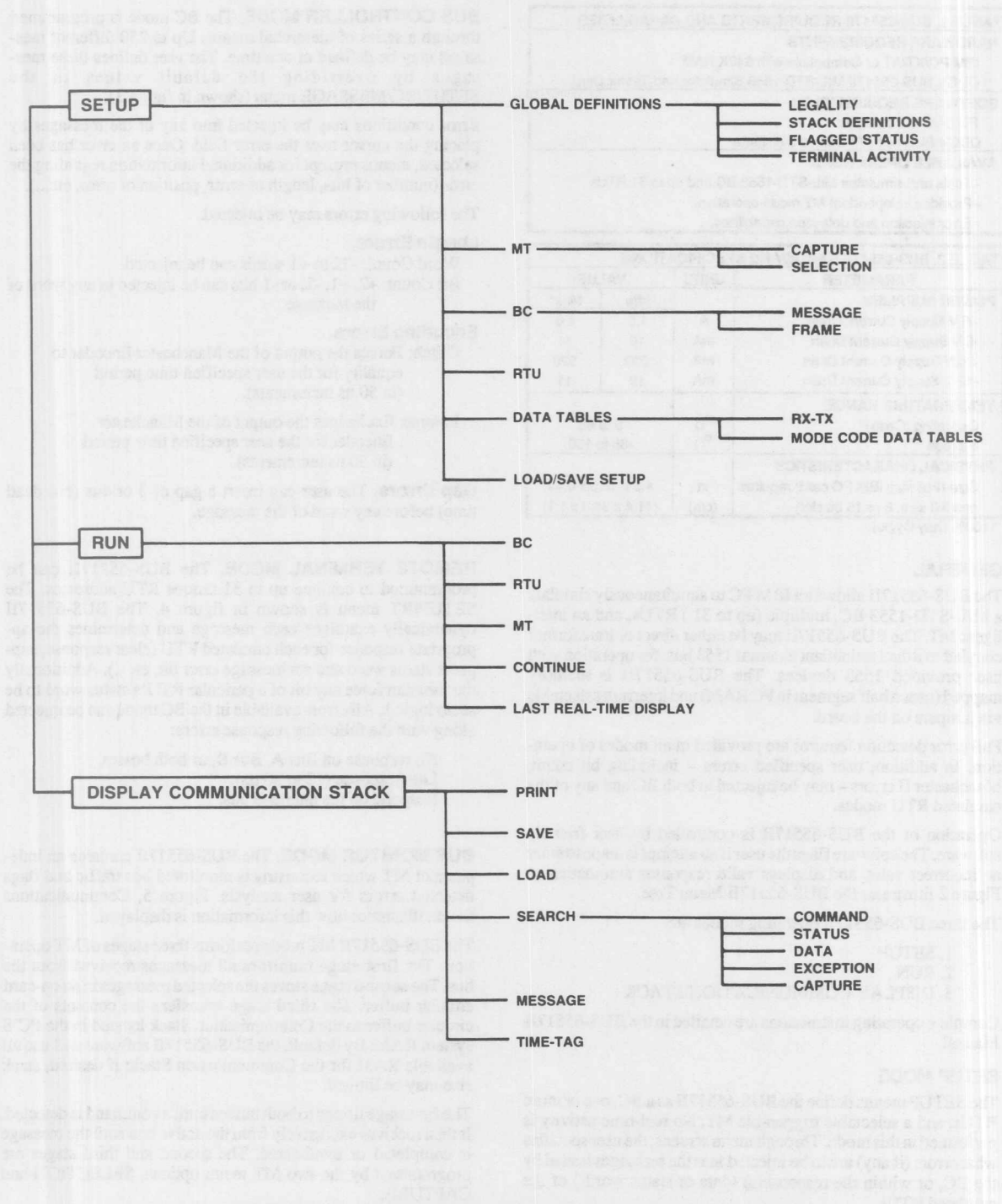


FIGURE 2. BUS-65517II MENU TREE

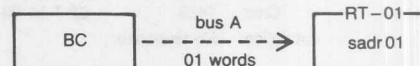
/setup/bc/message

Message - 1

error types
L - Length
E - Encoding
G - Gap
N - No error

Communication type: Receive

tadr	t/r	sadr	wcnt
01	R	01	01



time to next message: Default	data table number:	bus	error: None
95 $\mu$ sec	1	A	

FIGURE 3. SETUP/BC/MESSAGE MENU

**SELECTION** By default, the BUS-65517II monitors all 1553 bus traffic. If desired, the user can select which messages are to be stored in the Communication Stack. Messages may be selected on the basis of RT Address, T/R type, and subaddress.

**CAPTURE** By default, the BUS-65517II begins storing the selected bus traffic as soon as the user issues the RUN command. If desired, the BUS-65517II can begin monitoring only after a specific command is seen on the bus, after any exception, (invalid word, invalid response, flagged bit in status word, etc...) is detected, after a specific exception, or upon receipt of an external trigger via the BUS-65517II's D type connector. The CAPTURE condition is defined by selecting the desired condition from the CAPTURE MENU.

After executing a RUN command, the 1553 traffic may be displayed by calling an the DISPLAY COMMUNICATION STACK screen (refer to figure 5).

## SETUP GLOBAL DEFINITIONS

Global definitions are conditions common to BC, RTU, and MT. They include:

1. **Transmit Amplitude.** The transmitter amplitude of the BC and RTUs can be varied in 0.1V (max) steps from 0.1V to at least 18Vpp as measured across a 77 Ohm load attached to the BUS-65517II BNC connector. The amplitude is specified by entering a number between 0 and 255.

2. **Response Time.** This option defines the maximum time (14, 16, 18, or 20  $\mu$ s) allowed for an RTU response. If a status word is not received within the allowed time, the BC and MT will detect a No Response error.

## RUN MODE

The RUN mode causes the BUS-65517II to begin communication over the 1553 bus. The real-time display displays the 1553 bus traffic. This includes both internal emulated 1553 devices as well as traffic to and from external, user provided 1553 devices. A sample real-time display is shown in figure 6.

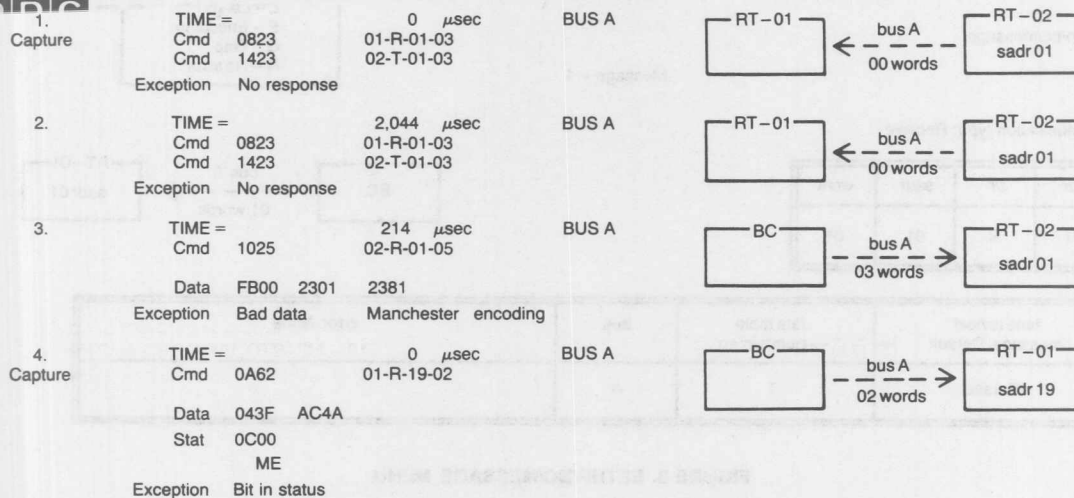
/setup/rt

Active as RT

Remote Terminal 01	
Default status:	000 000 000 00
Error type:	None
L - Length	T - Tadr
R - Response	G - Gap
E - Encoding	N - None
Bus control acceptance:	No
Delay after DBC acceptance:	40 $\mu$ sec

FIGURE 4. SETUP/RT MENU





End of tables

FIGURE 5. COMMUNICATION STACK

/run/bc

REAL TIME DISPLAY

BC RT MON running halted

invalid commands = 65504

total commands = 0,000,000,592

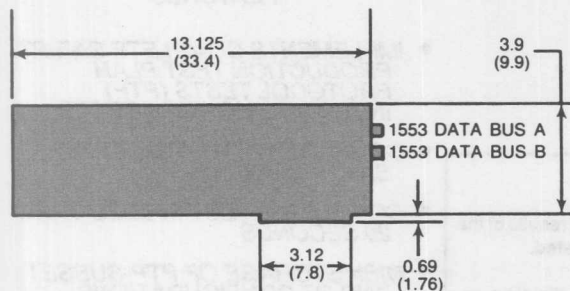
tadr	invalid data	invalid status	delayed data	resp. timing	wrong tadr	bit in status	illegal mode/cmd	total messages
00	00000	00000	00000	00001	00000	00001	00000	0,000,000,002
01	00000	00000	00000	00001	00000	00001	00005	0,000,000,032
02	00099	00000	00000	00012	00000	00000	00000	0,000,000,099
03	00000	00022	00000	00000	00000	00000	00000	0,000,000,022
04	00000	00000	00044	00000	00032	00000	00000	0,000,000,109
05	00000	00000	00000	00000	00000	00000	00000	0,000,000,333

FIGURE 6. REAL-TIME DISPLAY

TABLE 3. BUS-65517II INTERRUPT JUMPER SELECTION					
INTERRUPT	PIN NUMBERS				
	2	3	4	5	7
2	LOW	HI	HI	HI	HI
3	HI	LOW	HI	HI	HI
4	HI	HI	LOW	HI	HI
5	HI	HI	HI	LOW	HI
7	HI	HI	HI	HI	LOW

TABLE 4. BUS-65517II ADDRESS JUMPER SELECTION					
ADDRESS	PIN NUMBERS				
	19	18	17	16	15
9000	HI	LOW	LOW	HI	LOW
A000	HI	LOW	HI	LOW	LOW
B000	HI	LOW	HI	HI	LOW
C000	HI	HI	LOW	LOW	LOW
D000	HI	HI	LOW	HI	LOW

Note: Dimensions are in inches (centimeters)



**FIGURE 7. BUS-65517II MECHANICAL OUTLINE**

## ORDERING INFORMATION

**BUS-65517II** MIL-STD-1553 Simulator and Tester Card, includes menu software.

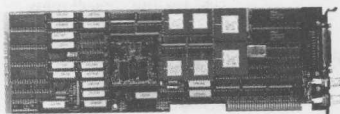
**BUS-690XXII**

Software Upgrades:

- 08 = MIL-STD-1553B Real Time Software and "C" Driver
- 09 = MIL-STD-1553A&B Real Time Software and "C" Driver
- 18 = MIL-STD-1553B Real Time Software and Pascal Driver.
- 19 = MIL-STD-1553A&B Real Time Software and Pascal Driver.
- 23 = MIL-STD-1553A&B Real Time Software, Pascal & "C" Drivers, and RT Production Test Plan Software.

Call the technical support number listed below for additional literature.

## MIL-STD-1553 RT PRODUCTION TEST PLAN PROTOCOL TESTING SOFTWARE & HARDWARE



### FEATURES

- IMPLEMENTS COMPLETE SAE RT PRODUCTION TEST PLAN PROTOCOL TESTS (PTP) INCLUDING NOTICE II TESTS
- COMPLIES WITH LATEST PTP SAE RELEASE AS4112
- COMPLETES TEST IN LESS THAN 20 SECONDS
- DISK STORAGE OF PTP-SUBSET AND RT CONFIGURATIONS
- USER FRIENDLY MENU DRIVEN DISPLAYS WITH HELP SCREENS
- RUNS ON IBM PC/XT/AT OR COMPATIBLE
- INCLUDES BUS-65517II "C" AND PASCAL LIBRARIES
- OPTIONAL DISCRETE I/O BOARD (CONTROL RT ADDRESS AND STATUS BITS)

### DESCRIPTION

The BUS-65519 is a turnkey system used to automate the protocol tests of the SAE RT Production Test Plan. A number of military contracts are imposing this test plan on MIL-STD-1553 suppliers.

With the BUS-65519, the test engineer characterizes the Unit Under Test (UUT) via the user friendly, menu driven software. Once this is done, the configuration can be saved to disk. The BUS-65519 can execute the ENTIRE production test plan in under 20 sec-

onds. A report detailing the results of the test is automatically generated.

The BUS-65519 reduces the time required to generate customize test software from an estimated 3 months, to less than 10 minutes.

The product consists of an IBM PC MIL-STD-1553 interface card, an optional parallel I/O card to generate static inputs to the UUT (see ordering information), and the menu driven software.

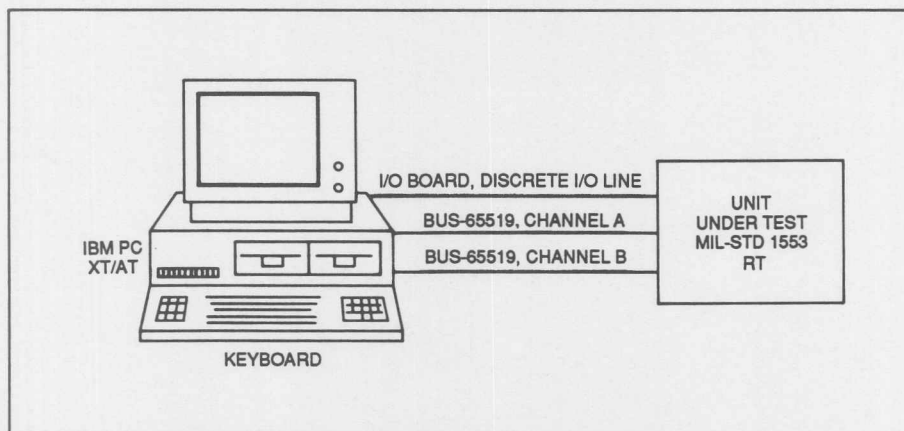


FIGURE 1. BUS-65519 OPERATING ENVIRONMENT

**TABLE 1. BUS-65519 REQUIREMENTS AND CAPABILITIES**

<b>HARDWARE REQUIREMENTS</b>
IBM PC/XT/AT or Compatible with 256 RAM
DDC's BUS-65519 BOARD & SOFTWARE
DATA TRANSLATION DT2817 DISCRETE I/O BOARD (OPTIONAL)
<b>SOFTWARE REQUIREMENTS</b>
PC DOS 3.0 or higher

## GENERAL

This data sheet contains the operating instructions for the BUS-65519 MIL-STD-1553 Protocol Software to perform the tests listed in Table 3, SAE RT Production Test Plan Section 5.2. The user can use the optional discrete I/O board to select discrete I/O signals on the unit under test.

The BUS-65519 is packaged with BUS-65517II's 1553A, 1553B, Pascal, and "C" Run-time libraries (refer to software manuals for details).

The following paragraphs describe the BUS-65519's operation.

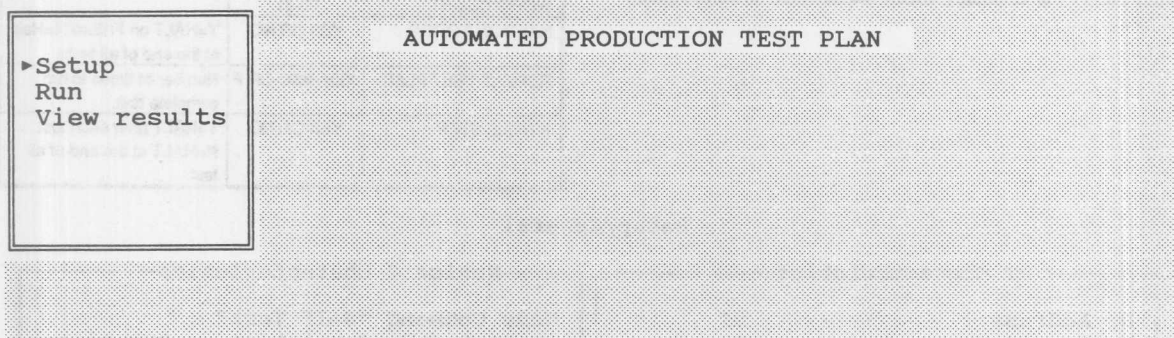
## MAIN MENU

When the BUS-65519 program is loaded, the MAIN MENU, as shown in FIGURE 2, will be displayed. All configurations editing, test execution, and result options are accessed here. (See FIGURE 3 to see the MAIN MENU structure)

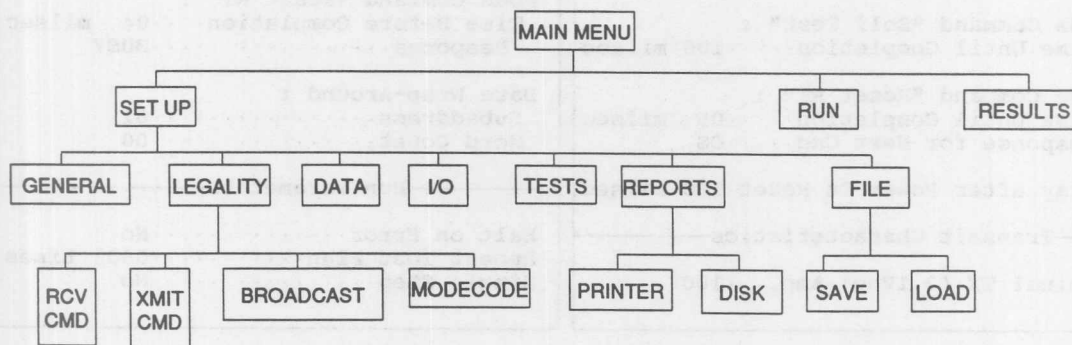
## SPECIAL FUNCTION KEYS

Special function keys are used to access the help screens, abort operation, and to exit. (See TABLE 2 for information)

TABLE 2. SPECIAL FUNCTION KEYS	
FUNCTION KEY	DESCRIPTION
ESC	EXIT SCREEN : LEAVE SCREEN AFTER CHANGES MADE
F1	HELP MENU : DISPLAY VALID VALUES FOR OPTION
F2	ABORT W/OUT UPDATE : LEAVE W/O MAKING CHANGES
F9	TOGGLE SOUND : TURN SOUND ON OR OFF
RETURN	TERMINATE FIELD ENTRY : GO TO NEXT OPTION IN THE MENU



**FIGURE 2. MAIN MENU**



**FIGURE 3. MAIN MENU STRUCTURE**

The General Setup Menu Screen permits the user to select the RT operating Characteristics and Notice 2 optional Characteristics. (See FIGURE 4)

RT OPERATING CHARACTERISTICS		
NAME	VALID VALUE	DESCRIPTION
RT ADDRESS	00-30	
NUMBER OF BUSES	01-99	
VARIABLE RT ADDRESSES	YES OR NO	
DBC ACCEPTANCE	YES OR NO	
MODE COMMAND SELF TEST TIME UNTIL COMPLETION	002-999	Time in ms which guarantees that SELF TEST was completed.
MODE COMMAND RESET RT TIME UNTIL COMPLETION	02-99 OR F	Time in ms which guarantees that RESET RT was completed.
RESPONSE FOR NEXT COMMAND	CS BUSY NR	CLEAR STATUS CS WITH BUSY BIT SET NO RESPONSE
DELAY AFTER POWER ON	001-999 OR F	Time in ms or F = Forever until KEYPRESSED
NOMINAL TX (2.1Vpp) AMP.	000-255	Calibrate the transmitter amplitude by attaching a scope to the RT.

NOTICE II OPTIONAL CHARACTERISTICS		
NAME	VALID VALUE	DESCRIPTION
MODE COMMAND SELF TEST TIME BEFORE COMPLETION	001-998	Time in ms must be less than TIME UNTIL COMPLETION.
RESPONSE	CS BUSY NR	Next message sent after TIME BEFORE COMPLETION the RT shall respond with CS, BUSY, or NR.
MODE COMMAND RESET RT TIME BEFORE COMPLETION	01-98	Time in ms must be less than TIME UNTIL COMPLETION.
RESPONSE	CS BUSY NR	Next message sent after TIME BEFORE COMPLETION the RT shall respond with CS, BUSY, or NR.
DATA WRAP AROUND SUB ADDRESS	01-30	
WORD COUNT	00-31	
HALT ON ERROR	YES OR NO	Y=HALT on Failure N=Halt at the end of all tests.
REPEAT TEST PLAN	0001-9999 OR F	Number of times to run complete test.
SINGLE STEP	YES OR NO	Y=HALT after each test N=HALT at the end of all test.

#### Setup/General

<p align="center">—RT Characteristics—</p> <p>RT Address..... 01</p> <p>Number of Buses.....02</p> <p>Variable RT Address.....Yes</p> <p>DBC Acceptance.....No</p> <p>Mode Command "Self Test" : Time Until Completion.....100 milsec</p> <p>Mode Command "Reset RT" : Time Until Completion.....05 milsec</p> <p>Response for Next Cmd.....CS</p> <p>Delay after Power On Reset.100 milsec</p> <p align="center">—Transmit Characteristics—</p> <p>Nominal TX (2.1Vpp) Amp....100</p>	<p align="center">—Notice 2 Characteristics—</p> <p>Mode Command "Self Test" : Time Before Completion....090 milsec</p> <p>Response.....BUSY</p> <p>Mode Command "Reset RT" : Time Before Completion....04 milsec</p> <p>Response.....BUSY</p> <p>Data Wrap-Around : Subaddress.....01</p> <p>Word Count.....00</p> <p align="center">—Run Parameters—</p> <p>Halt on Error.....No</p> <p>Repeat Test Plan.....0001 times</p> <p>Single Step.....No</p>
--	---

**FIGURE 4.GENERAL SETUP MENU SCREEN**  
(Default values)



**LEGALITY MENU SCREEN**

The user has a choice of 4 different types of commands to choose from: Receive command, Transmit Command, Broadcast and Mode Codes. For the first three choices, see FIGURE 5, the user may define the WORD COUNT and SUBADDRESS for those particular commands. For MODE CODE Commands, see FIGURE 6, the user may define the subaddresses for both TRANSMIT and RECEIVE Commands. The user may define CLEAR STATUS by typing a "+", MESSAGE ERROR by typing a "-" and a NO RESPONSE by typing a "." for a particular subaddress and word count.

—Legality/RT Response to Receive Commands—

	Sadr = 1	Wcnt = 0	Word Count																						
	0	4	8	12	16	20	24	28																	
S	1	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
u		+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
b		+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
a	4	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
d		+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
d	8	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
r		+	+	+	+	<div style="border: 1px solid black; padding: 5px; text-align: center;"> <b>Selection Options</b>  <hr/> '+' - Clear Status  '-' - Message Error  '.' - No Response  <hr/> F - toggles the "Fill to end of line" option  help </div>								+	+	+	+	+	+	+	+				
e		+	+	+	+									+	+	+	+	+	+	+	+				
s	12	+	+	+	+									+	+	+	+	+	+	+	+				
s		+	+	+	+									+	+	+	+	+	+	+	+				

PgDn

**FIGURE 5. LEGALITY MENU**

**NOTE: Shown for RECEIVE COMMANDS, similar menu for TRANSMIT and BROADCAST COMMANDS.**

—Legality/RT Response to Mode Commands—

	Undefined		MODE CODES																					
	0	4	8	12	16	20	24	28																
RX	-	-	-	-	-	-	-	-	+	+	+	+	+	+	+	+								
TX	+	+	+	+	+	+	+	+	-	+	+	-	-	+	+	+	+	+	+	+	+	+	+	+

	BROADCAST															
	0	4	8	12	16	20	24	28								
RX	-	-	-	-	-	-	-	-	+	+	+	+	+	+	+	+
TX	-	+	-	+	+	+	+	+	+	+	+	+	+	+	+	+

**FIGURE 6. LEGALITY MODE CODE MENU 5.**  
(Default values)

## DATA MENU SCREEN

The DATA MENU SCREEN, FIGURE 7, allows the user to define data for MODE CODE and NON-MODE CODE commands. The first three fields are what the tester sends to the UNIT UNDER TEST. For the TRANSMITTED DATA field, the user may enter data of his choice to be transmitted out on the bus.

Setup General Legality Data I/O Card Tests Reports File	Discrete Output Options	
	Automated	
	Service Request.....	Yes
	Busy.....	Yes
	Subsystem Flag.....	Yes
	Dynamic Bus Control.....	Yes
	Terminal Flag.....	Yes
	Hardware Reset.....	Yes
	Power On/Off.....	Yes
	RT Address.....	Yes
	Reset UUT to Latch RT Address..	Yes
	Delay After Changing Output....001 milsec	

Esc-Exit    F1-Help    F2-Abort    F9-Beep

**FIGURE 7. DATA MENU SCREEN**

## I/O CARD MENU

An optional I/O card can be used for selecting discrete output options, see FIGURE 8 and TABLE 3. For the discrete output options, a YES response means the output I/O card provides the variable selected output. A NO response means the user will be prompted for appropriate action. The DELAY after CHANGING OUTPUT specifies the settling time required by external hardware and ranges from 001 to 999 milliseconds. At this time, all lines are active high.

Setup General Legality Data I/O Card Tests Reports File	Data [HEX] for Mode Commands					
	Synchronize with Data					1234
	Bus A - Selective Bus Inhibit/Override					AAAA
	Bus B - Selective Bus Inhibit/Override					BBBB
	Transmitted Data					
	Word No.	Data [HEX]	Word No.	Data [HEX]	Word No.	Data [HEX]
	1	5555	12	5555	23	5555
	2	5555	13	5555	24	5555
	3	5555	14	5555	25	5555
	4	5555	15	5555	26	5555
	5	5555	16	5555	27	5555
	6	5555	17	5555	28	5555
	7	5555	18	5555	29	5555
	8	5555	19	5555	30	5555
	9	5555	20	5555	31	5555
	10	5555	21	5555	32	5555
	11	5555	22	5555		

Esc-Exit    F1-Help    F2-Abort    F9-Beep

**FIGURE 8. DISCRETE OUTPUT OPTIONS**

TABLE 3. DISCRETE I/O PIN OUT	
PIN #	DESCRIPTION
5	Dynamic Bus Acceptance
6	Sub System Flag
7	Busy
8	Service Request
9	Terminal Flag
10	Reset (Power ON)
32-36	RT Address (Pin # 32 = MSB)
37	RT Parity

### TEST MENU

This menu allows the user to select which test he would like to perform(See FIGURE 9). TABLE 4 is a complete listing of the PTP tests, by paragraph.

Tests	
5.2.1.1	RT Address
Yes 5.2.1.1.1	Valid RT Address
Yes 5.2.1.1.2	Invalid RT Address
Yes 5.2.1.2	Word Count
Yes 5.2.1.3	Subaddress
Yes 5.2.1.4	Error Injection
Yes 5.2.2.1	Dual Redundant Operation
5.2.2.2	Mode Commands
Yes 5.2.2.2.1	Dynamic Bus Control

FIGURE 9. TEST MENU WINDOW #1

**TABLE 4. TESTS INCLUDED IN PTP PROGRAM**

Tests	
5.2	Protocol Tests
5.2.1	RT Response to Command Words
5.2.1.1	RT Address
Yes 5.2.1.1.1	Valid RT Address
Yes 5.2.1.1.2	Invalid RT Address
Yes 5.2.1.2	Word Count
Yes 5.2.1.3	Subaddress
Yes 5.2.1.4	Error Injection
Yes 5.2.2.1	Dual Redundant Operation
5.2.2.2	Mode Commands
Yes 5.2.2.2.1	Dynamic Bus Control
5.2.2.2.2	Synchronize
No 5.2.2.2.2.1	Synchronize (Without Data Word)
Yes 5.2.2.2.2.2	Synchronize (With Data Word)
Yes 5.2.2.2.3	Transmit Status
Yes 5.2.2.2.4	Initiate Self-Test
Yes 5.2.2.2.5	Transmit BIT Word
5.2.2.2.6	Transmitter Shutdown and Override
Yes 5.2.2.2.6.1	Dual Redundant Shutdowns and Overrides
No 5.2.2.2.6.2	Selective Bus Shutdowns and Overrides
Yes 5.2.2.2.7	Terminal Flag Bit Inhibit and Override
Yes 5.2.2.2.8	Reset Remote Terminal
Yes 5.2.2.2.9	Transmit Vector Word
Yes 5.2.2.2.10	Transmit Last Command
5.2.2.3	Status Word
Yes 5.2.2.3.1	Service Request
Yes 5.2.2.3.2	Broadcast
Yes 5.2.2.3.3	Busy
Yes 5.2.2.3.4	Subsystem Flag
Yes 5.2.2.3.5	Terminal Flag
5.2.2.4	Broadcast Messages
5.2.2.4.1	Response to Bcst Commands
Yes 5.2.2.4.1.1	BC to RT Bcst Commands
5.2.2.4.1.2	Bcst Mode Commands
Yes 5.2.2.4.1.2.1	Bcst Synchronize (without data word)
Yes 5.2.2.4.1.2.2	Bcst Synchronize (with data word)
Yes 5.2.2.4.1.2.3	Bcst Initiate Self-Test
5.2.2.4.1.2.4	Bcst Transmitter Shutdown and Overrides
Yes 5.2.2.4.1.2.4.1	Bcst Dual Redundant Shutdowns and Overrides
No 5.2.2.4.1.2.4.2	Bcst Selective Bus Shutdowns and Overrides
Yes 5.2.2.4.1.2.5	Bcst Terminal Flag Bit Inhibit and Override
Yes 5.2.2.4.1.2.6	Bcst Reset Remote Terminal
Yes 5.2.2.4.1.3	RT to RT Bcst Commands
5.2.2.5	RT to RT Transfers
Yes 5.2.2.5.1	RT to RT Transmit
Yes 5.2.2.5.2	RT to RT Receive
Yes 5.2.2.5.3	RT to RT Timeout
Yes 5.2.2.6	Illegal Commands
A	Notice II
Yes A1	Unique Address
Yes A2	Mode Codes
Yes A3	Reset Remote Terminal
Yes A4	Initiate Self-Test
No A5	Power On Response
Yes A6	Data Wrap-Around
Yes A7	RT to RT Validation
< End of List >	

Esc-Exit F1-Help F2-Abort F9-Beep

PgUp

## REPORTS MENU

This menu sends a report to either the disk or printer. The user may specify N for NO RESULTS, F for FAILED RESULTS, or A for ALL RESULTS.

## FILE MENU

This menu allows the user to save or load a previously saved PTP-subset and RTU configuration to or from a disk. This provides the user a convenient way of setting up a variety of products to be tested.

## RUN MENU

After the user has gone through all the setup menus or selected a previous file, this selection will run all tests selected in the TEST MENU. As each test is being run, it will be displayed on the screen and if any errors occur they will also be displayed.

## RESULTS MENU

After all the tests are completed, the Results menu will display a list (see FIGURE 10) of all tests with any failures that had occurred.

```

*****
Production Tests
*****

Bus A   Bus B       Test
-----
Pass     5.2.1.1.1    Valid RT Address
Pass     5.2.1.1.2    Invalid RT Address
Pass     5.2.1.2      Word Count
Pass     5.2.1.3      Subaddress
Pass     5.2.1.4      Error Injection
Pass     5.2.2.1      Dual Redundant Operation
Pass     5.2.2.2.6.1  Dual Redundant Shutdown and Overrides
N/A      5.2.2.2.6.2  Selective Bus Shutdown and Overrides

```

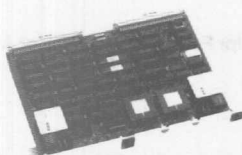
**FIGURE 10. RESULTS MENU**

## ORDERING INFORMATION

**BUS-65519** - Includes MIL-STD-1553 Tester and Production Test Plan Software.

**Optional parallel I/O Card (DT2817)** - Available from  
DATA TRANSLATION INC. 100 Locke Drive, Marlboro, MA  
01752-1192 (508) 481-3700





## MIL-STD-1553B BC/RTU/MT VME/VXI INTERFACE UNIT

### FEATURES

- VMEbus/VXIbus INTERFACE WITH INTELLIGENT 1553 BC/RT/MT
- STANDARD DOUBLE EUROCARD SIZE
- SUPPORTS ALL 1553B DUAL REDUNDANT MESSAGE FORMATS AND MODE CODES
- 8K X 16 ON-BOARD DUAL ACCESS RAM
- D08(E0), D16 DATA TRANSFERS
- A16/24, A16/32 JUMPER SELECTABLE
- ON-BOARD TIME TAG COUNTER
- DYNAMIC WRAP-AROUND BUILT-IN-TEST (BIT)
- ON-BOARD MEMORY MANAGEMENT

### DESCRIPTION

The BUS-65522 provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553B Data Bus and the parallel VMEbus and VXIbus. Software controls the BUS-65522's operation as either a 1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT).

The VME/VXI board is packaged on one double eurocard size printed circuit card. Its on-board 8K x 16 dual access RAM is double buffered, preventing partially updated data from being read by the CPU or transmitted to the 1553 Data Bus. The CPU can access any part of the shared RAM as needed.

All MIL-STD-1553 functions: address recognition, Manchester coding validation, bit count and mode code response

are provided without subsystem intervention. The BUS-65522 contains eleven VMEbus/VXIbus and 1553 command registers which allow the subsystem to configure its operation under software control.

The BUS-65522 supports four groups of vectored interrupts. One custom interrupt can be programmed by the on-board PROM. The interrupts can be software controlled as to enable/disable, priority level and 8 bit vector.

Additional features include a dynamic wrap-around Built-In-Test (BIT), on-board Time Tag counter, and software loaded board base address and BUS-65522 RT address. The BUS-65522 supports all dual redundant mode codes and message formats. Its full compliance with MIL-STD-1553B makes it an excellent choice for dynamic real time applications.

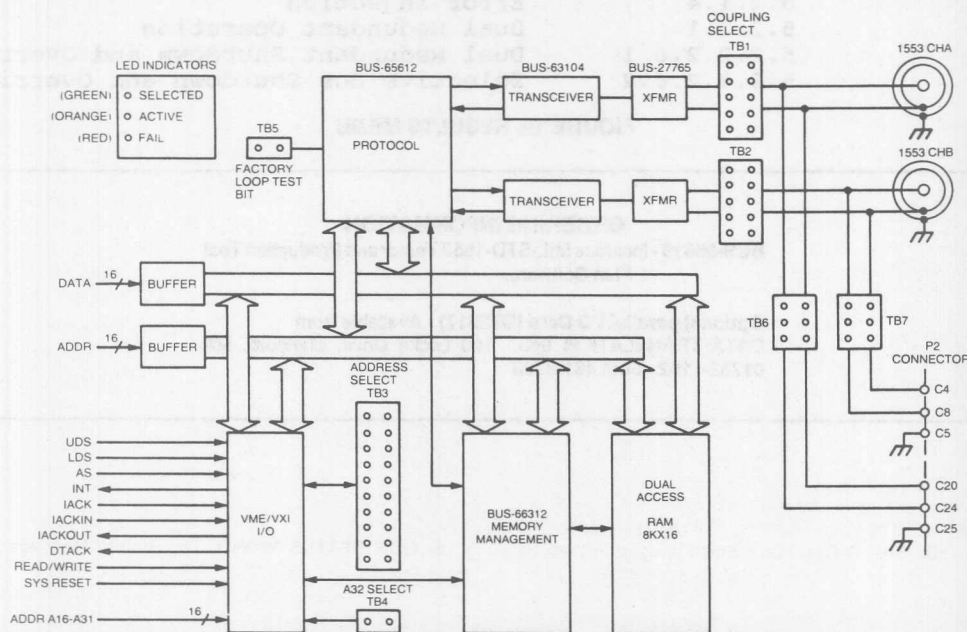


FIGURE 1. BUS-65522 BLOCK DIAGRAM

**TABLE 1. BUS-65522 & 65523 SPECIFICATIONS**

PARAMETER	VALUE	UNITS
<b>Power Supplies</b>		
+ 5V (+/-10%)	1.00	Amps, max.
- 12V-15V (+/-10%)	0.21 (100% DC) 0.06 (IDLE)	Amps, max. Amps, max.
- 12V-15V (+/-10%)	0.26 (100% DC) 0.13 (IDLE)	Amps, max. Amps, max.
<b>Temperature Range</b>		
Operating	0 TO +70	Degrees C
Storage	-65 TO +150	Degrees C
<b>Size</b>		
Double Eurocard	6.3" x 9.2" x 0.6" 16 x 23.4 x 1.1	Inches CM

## GENERAL

The BUS-65522 provides a user friendly interface between the serial MIL-STD-1553B Bus and the VME/VXI Bus. The operating modes of the BUS-65522 are controlled through the use of eleven on-board registers. 1553 message traffic is stored and retrieved using the dedicated, memory mapped, on-board 8K words of RAM. The 1553 internal registers control and operate the BUS-65522. They include the Configuration Register, Start/Reset Register, 1553 Time Tag Register, Interrupt Select Register, and RTU Address Register. The Configuration Register defines the operating mode. The Start/Reset Register generates the start and reset signals. The Interrupt Mask Register enables desired interrupts, with the interrupt priority level being software programmable by the user. The RTU Address Register is used to program the RTU address. The 1553 Time Tag Register is used to time tag messages or act as a word counter in the out mode. The VME/VXI functions are controlled by the other six registers which include the Identification Register, Device Type, STATUS Control, offset, vector/enable/level and Device Type Extension Register.

The BUS-65522's 8K x 16 high speed static RAM is shared by the CPU and the 1553 Bus with memory arbitration handled automatically by the BUS-65522.

The BUS-65522 will withhold the  $\overline{DTACK}$  signal to the CPU while a word is being transferred to or from the 1553 Bus. Since the memory arbitration is handled by simply stretching the handshake cycle, the wait state is transparent to the CPU's software. A maximum wait of 1.90  $\mu$ s may occur.

The RAM implements the Stacks and Look-Up Tables required for the different modes of operation, as well as for storing the 1553 messages. A double buffering architecture is available to prevent partially updated information from being transferred to or from the 1553 Bus. A Descriptor Stack is used in both BC and RTU modes. This stack records the status of each message, the time the message was transmitted or received, and contains either the received 1553 command, (in RTU mode), or the actual address of the data block containing the 1553 message (in BC mode). In the RTU mode, a Look-Up Table is implemented to

store the address of the data blocks to be used when receiving or transmitting messages for a particular subaddress.

The BUS-65522 may also be used as a passive MT; in this mode all messages transferred across 1553 Bus A or Bus B are captured. The BUS-65522 generates an Identification Word for each word, indicating its sync type (command or data), the 1553 channel it was received on, (A or B), whether it contained an error, (parity, incorrect bit count, etc.) and whether it was preceded by a gap of more than 2.5  $\mu$ s. If the gap was more than 2.5  $\mu$ s, the length of the gap, (in 0.5  $\mu$ s units) using 8 bit resolution is given.

## ADDRESSING THE BUS-65522 WITH A MICROPROCESSOR

The BUS-65522 contains DDC's BUS-66312 II to manage its on-board 8K x 16 RAM.

All pointers used by the BUS-66312 are assumed to be word addresses. For example, to begin Descriptor Stack B at location 1000, the user initializes Descriptor Stack Pointer B to word location 0800 (1000 divided by two).

## INDICATORS:

Green front panel led indicates that the BUS-65522 offset register has been initialized.

Orange front panel led indicates when the board is active on the MIL-STD-1553 Bus.

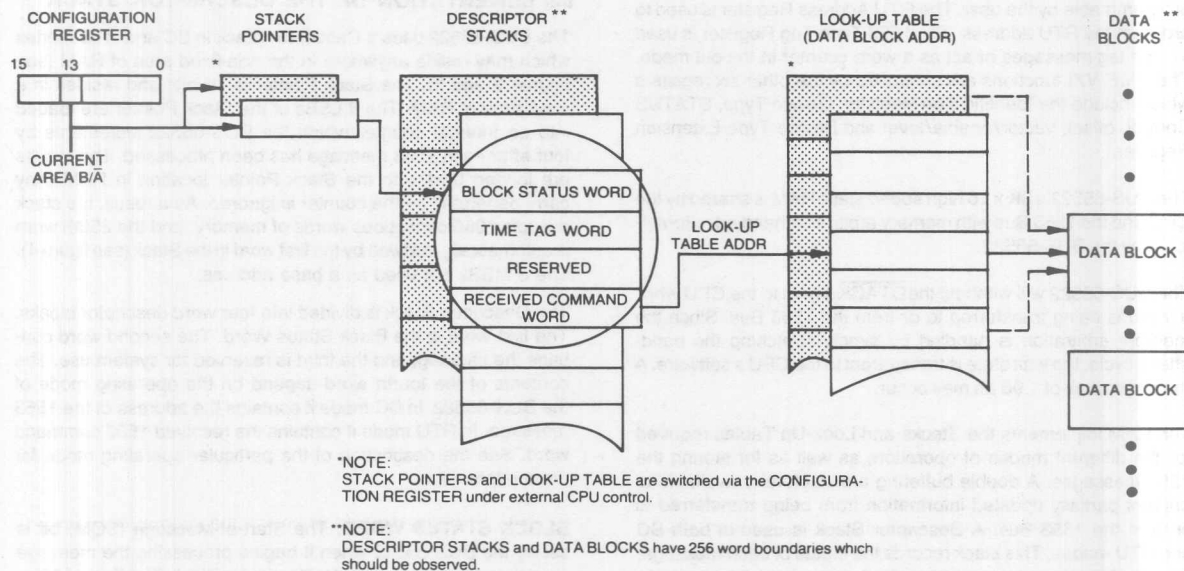
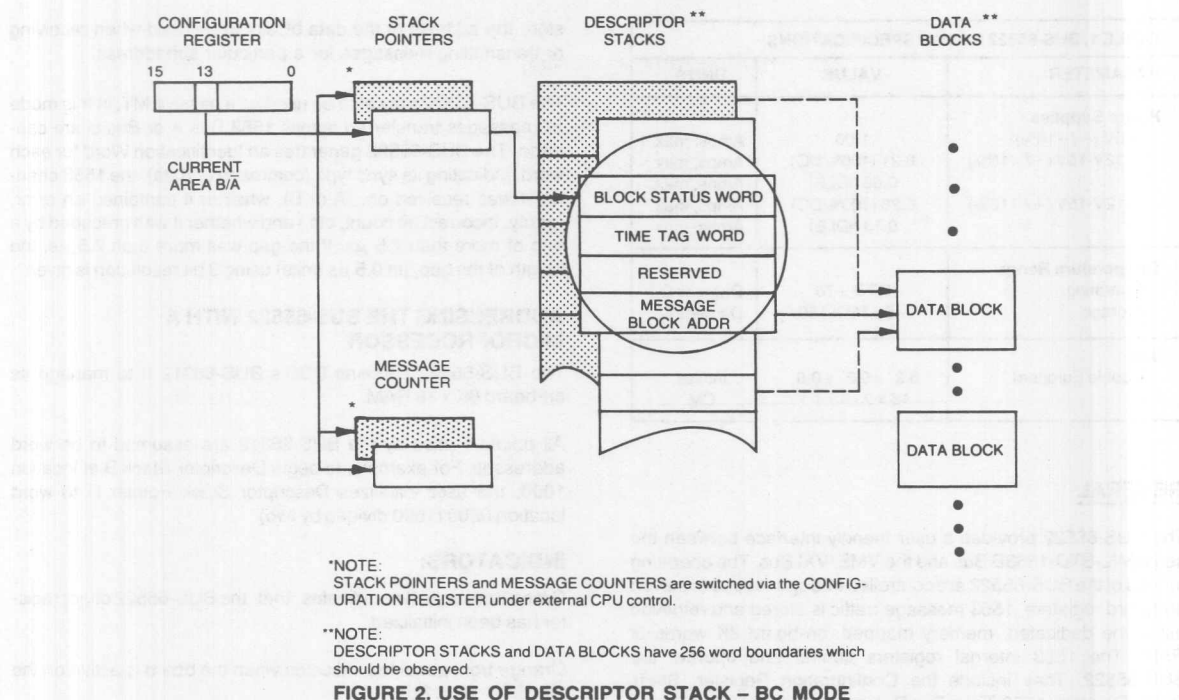
Red front panel led indicates when the BUS-65522 has failed the internal self BIT test.

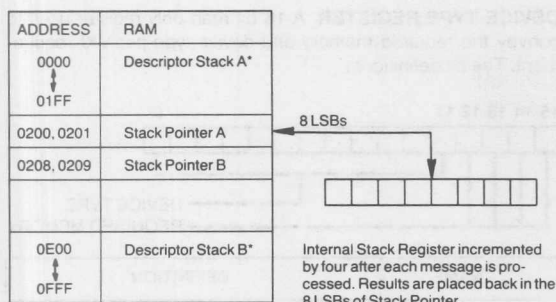
## IMPLEMENTATION OF THE DESCRIPTOR STACK

The BUS-65522 uses a Descriptor Stack in BC and RTU modes which may reside anywhere in the non-fixed area of RAM (see figures 2 and 3). The Stack Pointer is 16 bits and resides in a fixed area of RAM. The 8 LSBs of the Stack Pointer are loaded into an internal counter which the BUS-65522 increments by four after each 1553 message has been processed. The results are loaded back into the Stack Pointer location in RAM. Any carry generated by the counter is ignored. As a result, the stack occupies 256 contiguous words of memory, and the 256th word is automatically followed by the first word in the Stack (see figure 4). The 8 MSBs are used as a base address.

The Descriptor Stack is divided into four word descriptor blocks. The first word is the Block Status Word. The second word contains the time tag, and the third is reserved for system use. The contents of the fourth word depend on the operating mode of the BUS-65522. In BC mode it contains the address of the 1553 message. In RTU mode it contains the received 1553 command word. See the description of the particular operating mode for more information.

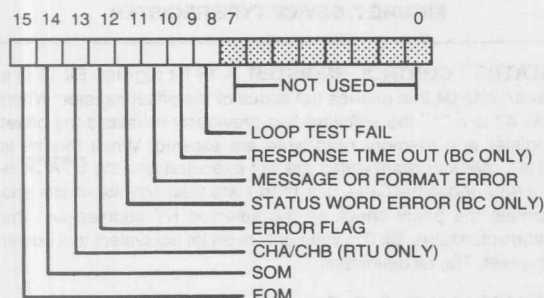
**BLOCK STATUS WORD.** The Start-of-Message (SOM) bit is set by the BUS-65522 when it begins processing the message associated with that particular Descriptor Block. The End-of-Message (EOM) bit is set and the SOM reset upon completion of the message. MESSAGE STATUS and ERROR bits are also set at that time. See figure 5 and table 2.





\*The address space listed is an example.

**FIGURE 4. IMPLEMENTATION OF DESCRIPTOR STACK**



**FIGURE 5. BLOCK STATUS WORD**

TABLE 2. BLOCK STATUS WORD BIT DEFINITIONS	
NAME	DEFINITION
EOM	End Of Message. Set at the completion of a message transfer, regardless of whether or not any errors were detected.
SOM	Start Of Message. Set at the beginning of a message transfer and reset upon completion of the message, regardless of whether or not any errors were detected.
CHA/CHB	Channel A/B. Set in RTU mode to indicate whether the message was received on 1553 bus A or B. Set to 0 in BC mode regardless of which bus is used for the message.
ERROR FLAG	Indicates an error was detected during the processing of the particular message. The particular error can be determined by examining bits 0 to 3.
STATUS SET	Set in BC mode to indicate that the received RTU status word had a status bit set or that the wrong RTU responded to the command.
FORMAT ERROR	Set when the MESSAGE ERROR flag is set in the returning RTU's status word or if any word received off the bus violated 1553B specifications (incorrect parity or Manchester sync field, incorrect number of bits, etc.). Also set in RTU mode when the BUS-65522 is acting as the receiving RTU in an RTU-RTU message transfer to indicate that the wrong RTU responded as the transmitting RTU.
RESPONSE TIMEOUT	Set in BC mode if the addressed RTU did not respond within 14 $\mu$ s of receiving a Transmit command or the last data word in a Receive command. Also set in RTU mode when the BUS-65522 is acting as the receiving RTU in a RT-RT message transfer to indicate that the transmitting RTU did not respond in time.
LOOP TEST FAIL	Set to indicate that the BUS-65522 did not pass its continuous on-line self test.

**TIME TAG:** In BC and RTU modes the contents of the 1553 Time Tag Counter is loaded into this location at the beginning of each message and updated at the end. Each of the 16 bits represent 1  $\mu$ s. See 1553 time tag/word counter register description.

## ADDRESS MODIFIERS

The address modifiers are programmed in a PAL, with the following response s:

ADDRESS MODE	MODIFIERS
A16	29, 2D
A24	3D, 3E, 39, 3A
A32	0D, 0E, 09, 0A

## INTERRUPT PROCESSING

The BUS-65522 generates an interrupt to the processor, upon receiving an interrupt acknowledge from the processor. The board will place the interrupt vector on the data bus and remove the interrupt request. Further interrupts are inhibited until the Status / Control register is read. A 1553 reset mode command or power-on condition will inhibit further interrupts. The interrupts will be enabled after the processor initiates a Status / Control register read command.

## INTERRUPT SPECIFICATION

The BUS-65522 generates four types of interrupts. These types can be individually enabled or disabled by the software with the VECTOR/ENABLE/LEVEL REGISTER. The interrupt vector, priority level, and interrupt type enable are loaded into this register. The four interrupt types are:

1553  
PROM/WORD COUNT  
BIT FAIL  
BUFFER FLIP

1553 interrupt-is generated for an error condition or end of message (EOM). The error could occur for either a format error, status bit set or no response as shown in the 1553 section.

**PROM/WORD COUNT INTERRUPT**-is used in the RT mode by programming a illegalization PROM to meet the system requirement. Parameters monitored by the PROM are subaddress, T/R bit, Word Count and valid messages. In the monitor mode of operation this interrupt is generated whenever the time tag counter crosses the internal memory 256 word boundary, indicating 256 (data & tag) words have been placed in memory.

**BIT FAIL.** This is generated whenever the internal Wraparound self-test fails.

**BUFFER FLIP.** This indicates that the requested Buffer Flip (memory swap) has been completed. This flip occurs after the 1553 message activity has ceased. See Figure 8. Bit 8.



## ILLEGALIZING PROM

The BUS-65522 has a socket for a 4K x 4 PROM (U42, PN 27341) that is used in the RT mode to illegalize commands, resetting the time tag counter, generating a custom selected interrupt and a custom selected trigger. The PROM mapping should be setup as follows:

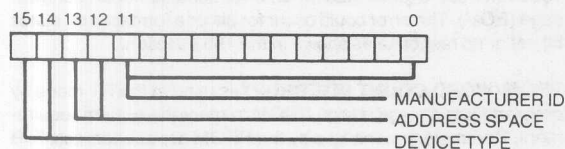
ADDRESS	OUTPUT
A0 WORD COUNT 0	00 ILLEGAL
A1 WORD COUNT 1	01 TIME TAG RESET
A2 WORD COUNT 2	02 CUSTOM INTERRUPT
A3 WORD COUNT 3	03 NOT USED
A4 WORD COUNT 4	
A5 SUB ADDRESS 0	NOTES:
A6 SUB ADDRESS 1	Maximum access time
A7 SUB ADDRESS 2	(address to data valid)
A8 SUB ADDRESS 3	is 250ns.
A9 SUB ADDRESS 4	
A10 T/R	For further information
A11 BROADCAST	refer to User's Manual.

## BUS-65522 Register Specification

TABLE 3. BUS-65522 REGISTERS			
WORD ADDRESS	BYTE	ADDRESS	DESCRIPTION
00	00	01	IDENTIFICATION
02	02	03	DEVICE TYPE
04	04	05	STATUS / CONTROL
06	06	07	OFFSET (BASE ADDRESS OF RAM)
08	08	09	VECTOR / ENABLE / LEVEL
0A	0A	0B	DEVICE TYPE EXTENSION
0C	X	0D	1553 RT ADDRESS
0E	0E	0F	1553 BC-RT TIME TAG / MT WORD COUNT
10	X	11	1553 INTERRUPT SELECT
12	12	X	1553 CONFIGURATION
14	X	X	1553 NOT USED
16	X	17	1553 START / RESET

## DEFINITIONS:

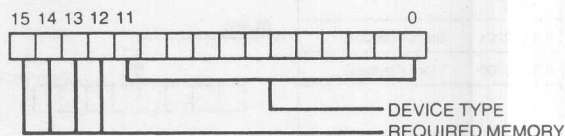
**IDENTIFICATION REGISTER.** A 16 bit read only register used to convey the device class, address space and manufacturer identification per VXI requirement. The bit definitions:



NAME	DEFINITION
DEVICE TYPE	"11" = Register
ADDRESS SPACE	00 (TB3 open A16/A24 mode selected) 01 (TB3 closed A16/A32 mode selected)
MANUFACTURER ID	1111 1110 1000 (HEX FE8) = DDC'S

FIGURE 6. IDENTIFICATION REGISTER

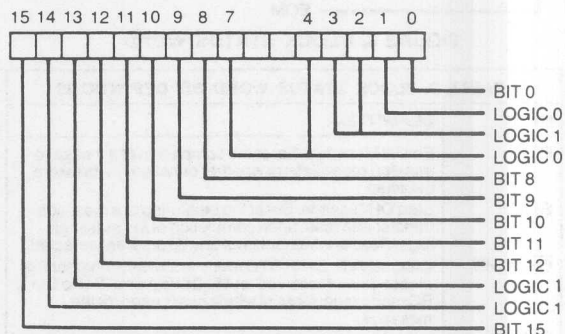
**DEVICE TYPE REGISTER.** A 16 bit read only register used to convey the required memory and device type per VXI requirement. The bit definitions:



NAME	DEFINITION
REQUIRED MEMORY	1001 (TB3 open A16/A24 mode selected) 1111 (TB3 closed A16/A32 mode selected)
DEVICE TYPE	0110 0101 0000 (HEX 620) = BUS-65522 0110 0011 0000 (HEX 630) = BUS-65523

FIGURE 7. DEVICE TYPE REGISTER

**STATUS / CONTROL REGISTER.** A 16 bit register. Bit 15 is a read/write bit that defines the status of the offset register. When this bit is a "1" the software has previously initialized the offset register and memory read/write are allowed. When this bit is reset, memory read/writes are not executed and the DTACK is not returned to the CPU. Bits 14 to 1 are read only status bits and contain the parity check on the selected RT address and the interrupts status. Bit 0 is write only reset bit equivalent to a power on reset. The bit definitions:



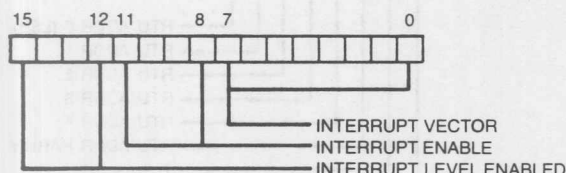
NAME	DEFINITION
BIT 15	RAM ENABLE Enables access to RAM. Writing a "1" enables access to RAM. this bit is reset upon power up or with bit 0 of the STATUS/CONTROL.
BIT 12	1553 address has odd parity
BIT 11	1553 interrupt
BIT 10	Custom interrupt
BIT 9	Loop error interrupt
BIT 8	Buffer flip interrupt
BIT 0	Don't care read. A write "1" causes a reset, same as power on reset of board.

FIGURE 8. STATUS/CONTROL REGISTER



**OFFSET REGISTER.** This is a 16 bit read/write register which defines the on board memory base address. In the A16/23 mode the upper 8 bits of the register are not used. Bits 15-0 equals the memory base address. Note: User must set Bit 15 to a logic "1" to access RAM.

**VECTOR/ENABLE/LEVEL REGISTER.** This is a 16 bit read/write register which defines the value of the interrupt vector, enable/disables the four interrupts and defines the interrupt priority level to 4, 5, 6, and 7. The bits are defined as:



NAME	DEFINITION
INTERRUPT LEVEL ENABLE	Bit 15 = "1" level 7 enabled Bit 14 = "1" level 6 enabled Bit 13 = "1" level 5 enabled Bit 12 = "1" level 4 enabled
INTERRUPT ENABLE	Bit 11 = "1" enables 1553 interrupt Bit 10 = "1" enables custom interrupt Bit 9 = "1" enables BIT interrupt Bit 8 = "1" enables buffer flip interrupt
INTERRUPT VECTOR	Bit 7 = MSB (user defined) Bit 0 = LSB

**FIGURE 9. VECTOR/ENABLE/LEVEL REGISTER**

**DEVICE TYPE EXTENSION REGISTER.** This is a 16 bit read only register that completes the device type model code. For a standard BUS-65522/23 this register is defined to be (hex 0000) 0000 0000 0000 0000. For earlier SN's the register will read:

BUS-65522 = 0010 0010 0000 0000 (HEX2200)  
BUS-65523 = 0010 0011 0000 0000 (HEX2300)

**1553 TIME TAG / WORD COUNT REGISTER.** This 16 bit read/write register is used in two different modes. In the BC or RT mode it performs as a time tag counter, that is incremented every microsecond. In the MT mode it is a word counter that increments every time a 1553 word and its identification words are placed in memory. (i.e., Every time a word pair occurs the register increments 1.)

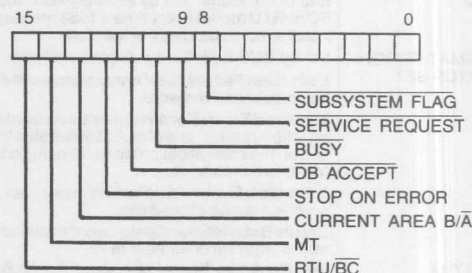
The time tag counter is reset by any of the following:

1. Write operation clears register.
2. Power on reset
3. Status control reset
4. 1553 reset, (start/reset register)
5. As programmed in the RT illegalization PROM in the RT mode of operation. ex: mode code reset.

The time tag/word counter register bit definition is as follows:

- Bit 15-0
- Time tag (RT/BC) mode  
LSB = 1 microsecond
  - Word count (MT) mode  
LSB = 2 words in memory (data & tag word)

**1553 CONFIGURATION REGISTER.** An 8 bit read/write register. The four MSB's define the mode of operation; the four LSB's control the RT status bits in the 1553 status word. Activating the SUBSYSTEM FLAG, SERVICE REQUEST, BUSY, and DB ACCEPT bits to logic "0" causes the BUS-65522 to set these bits in the 1553 status word. If BUSY is set, the status word only will be transmitted upon receipt of a transmit command, but data associated with a receive command will be placed in the RAM, see figure 10. The bits are defined as follows:



NAME	DEFINITION		
SUBSYSTEM FLAG	1553 Status Word bit.		
SERVICE REQUEST	1553 Status Word bit.		
BUSY	1553 Status Word bit.		
DB ACCEPT	1553 Status Word bit.		
STOP ON ERROR	Causes BC to stop at end of current data block if an error is detected.		
CURRENT AREA B/A	Used for Double Buffering; see description.		
RTU/BC, MT	Operating Mode	Bit 15	Bit 14
	BC	0	0
	MT	0	1
	RTU	1	0
	ILLEGAL	1	1

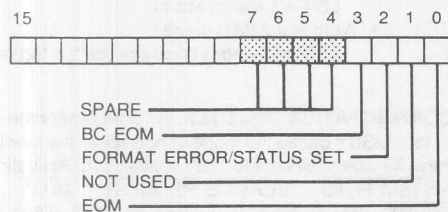
Note: A "0" in bits 9-11 activates the corresponding bit in the 1553 Status Word.

Note: A "0" in bits 9-11 activates the corresponding bit in the 1553 Status Word.

**FIGURE 10. 1553 CONFIGURATION REGISTER**

**1553 INTERRUPT SELECT REGISTER.** An 8 bit read/write register used to enable interrupt conditions. All interrupts are enabled with a logic "1". In the BC and RT modes the BUS-65522 generates an IRQ (interrupt request) for an EOM or error set condition. An IRQ is generated in the BC mode for a BC EOM indicating that all requested transfers by the BC are completed. Refer to the VECTOR/ENABLE/LEVEL REGISTER for setting

the interrupt priority level, see figure 9. The bits are defined as follows:



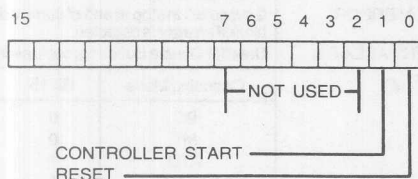
NOTE:

Spare Bits 4-7 = CPU can read or write.

INTERRUPT	DEFINITION
EOM	End of message. Set by BUS-66300 II (during BC or RTU mode) every time a 1553 message is transferred (regardless of validity).
FORMAT ERROR/STATUS SET	Set by BUS-66300 II for these conditions: <b>Loop Test Failure:</b> Last transmitted word did not match received word. <b>Message Error:</b> Received message contained an address error, one of eight 1553 status bits set, or 1553 specification violated (parity error, Manchester error, etc.). <b>Time-Out:</b> Expected transmission was not received during allotted time. <b>Status Set:</b> Received status word contained status bit(s) set or address error.
BC EOM	Bus Controller End of Message. Set by BUS-66300 II (in BC mode) when all messages have been transferred.

FIGURE 11. 1553 INTERRUPT SELECT REGISTER

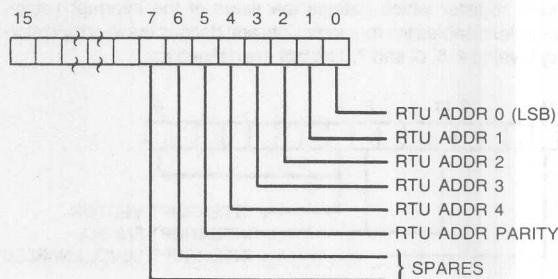
**1553 START/RESET REGISTER.** A write only two bit register used to enable or reset the terminal, see figure 12. The bits are defined as:



NAME	DEFINITION
RESET	Places BUS-65522 in the power-up condition; Configuration, Start/Reset Register, and Interrupt Mask registers are reset to "0". Does not affect RTU Address Register or the contents of RAM. It is recommended that this command be issued prior to changing the operating mode (RT-BC, BC-MT, etc.).
CONTROLLER START	Used in BC mode to begin transmission of the designated number of messages. The message count must have been previously loaded into the current area message count, using 1's complement notation. Also used in MT mode to begin reception of 1553 message traffic. (Yellow LED = in use.)

FIGURE 12. 1553 START/RESET REGISTER

**1553 RT ADDRESS REGISTER.** An internal 8 bit read/write register used to set the RT address and to enable the BUS-65522 to receive information transferred over the 1553 bus, see figure 13. The bit definitions are as follows:



NAME	DEFINITION
RTU ADDR PARITY	Odd parity bit associated with five RTU address bits. BUS-65522 will not respond to 1553 commands if the parity is incorrectly set. Set to a logic "1" if RTU Address is 0, 3, 5, or 6.
RTU ADDR 0-4	RTU address bits.

FIGURE 13. 1553 RTU ADDRESS REGISTER

## BC MODE

The BC mode is selected by setting the two MSBs of the Configuration Register to logic "0". The BUS-65522 defaults to BC mode upon power up and after receipt of a Reset signal from the CPU.

**BC INITIALIZATION.** For BC operation, the user initializes the RAM, Stack Pointers, Descriptor Stack Entries, and Message Blocks. See table 4 for a sample memory map and follow the steps in figure 14 (A), (B), and (C).

The BUS-65522 uses an indirect addressing architecture to determine which messages to send over the 1553 bus. The Stack Pointer indicates which entry in the Descriptor Stack to use, while the fourth word in the Descriptor Block indicates the location of the 1553 message (see figure 2).

Two Stack Pointers and two Descriptor Stacks are provided to allow the user to double buffer the RAM. All transfers to/from the 1553 bus are made using the "current" Descriptor Stack and Stack Pointer, as defined by the user through bit 13 of the Configuration Register.

The Descriptor Stack in BC mode occupies 256 contiguous words. It may be located anywhere in the non-fixed area of RAM as long as it begins on a 256 word boundary (i. e., HEX 0000, 0700, 1000, XX00, etc.). Each Descriptor Block is four words long; the fourth word of each block is loaded by the user with the address of the message to be transferred onto the 1553 bus.

Each data block should be formatted as shown in figure 15. The first word of the message is the Control Word (see figure 16). The BUS-65522 uses an 8 bit counter for the lower byte of the internal Address Counter. As a result, the data block may be stored anywhere in the non-fixed area of RAM, so long as the individual data block does not cross a 256 word boundary. For example, a data block should not begin at word location 04FE if the user plans on storing more than two words in the block. The first word will be stored at 04FE, the second at 04FF, and a third word would be stored at 0400 as a result of the lower byte Address Counter overflowing.

The number of messages to be transferred must be stored in the current area Message Counter location of the RAM in 1's complement (XXFE = 1 message). The user instructs the BUS-65522 to begin transferring the messages by setting bit 1 of the Start/Reset Register to logic "1". The BUS-65522 will then begin transferring the messages in the order in which their starting addresses were placed in the Descriptor Stack (see figure 17).

The BUS-65522 can be instructed to end 1553 bus transactions if any message does not transfer successfully. This is done by setting the STOP-ON-ERROR bit in the Configuration Register. An ERROR interrupt will be generated at that time if enabled by the user.

If desired, a BCEOM interrupt can be generated to notify the CPU that the BUS-65522 has completed the transfer of the requested number of messages. The CPU can also request that an EOM interrupt be generated upon completion of each individual message.

While the current group of messages is being processed, the CPU may read or write to the non-current area of RAM in order to set up the next group of messages, or to examine the results of the previous bus transfers.

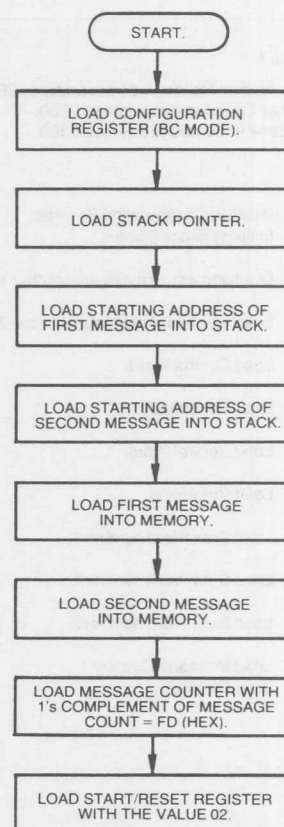
Once a block of messages has been completed, the user may swap the current and non-current areas and instruct the BUS-65522 to execute the next group of messages. This is done by toggling bit 13 of the Configuration Register and issuing a new BCSTART command.

**BC SOM SEQUENCE.** After setting the CONTROLLER START bit in the Start/Reset Register, the BUS-65522 takes the following actions:

1. Uses Stack Pointer to get the address of the current Descriptor Stack Entry.
2. Sets SOM flag in the Block Status Word to indicate a transfer operation in progress.
3. Stores the Time Tag.

4. Reads the Data Block Address from the fourth location of the Descriptor Stack and transfers the Data Block Address into an internal Address Register.
5. Begins transmission of the message onto the 1553 bus.

Note that data words are transferred to and from memory using the internal Address Register.



**FIGURE 14A.**  
BC SET-UP EXAMPLE FOR  
TWO MESSAGE TRANSFER

**BC EOM SEQUENCE:** Upon completion of a 1553 message, the BUS-65522 takes the following action:

1. Reads the Stack Pointer to get the address of the current Descriptor Stack Entry.
2. Updates the Block Status Word by resetting the SOM and setting EOM and any error bits.
3. Updates the Time Tag.

4. Increments the contents of the Stack Pointer by four and increments the Message Counter by one.
5. Additional messages are transmitted.
6. Generates a BCEOM interrupt if enabled and no further messages are to be transmitted.

Note that if an error is received and STOP ON ERROR is set, the BUS-65522 stops issuing commands over the 1553 bus. The Stack Pointer will point to the next message to be transmitted.

#### GIVEN:

All values are in HEX.

1. Stack area A is used and is located from address 0000 to address 01FF.
2. Message number 1 is located at address 0280.
3. Message number 2 is located at address 0300.

BYTE ADDRESS		CONTENTS
—12	Initialize Configuration Register.	
0200	Initialize Stack Pointer.	WORD 0000
0006	Load address of message number 1 into Stack.	WORD 0140
000E	Load address of message number 2 into Stack.	WORD 0180
0280	Load Control Word.	WORD 0080
0282	Load Command.	WORD 0C21
0300	Load Control Word.	WORD 0000
0302	Load Command.	WORD 1823
0304	Load Data Word number 1.	WORD 1111
0306	Load Data Word number 2.	WORD 2222
0308	Load Data Word number 3.	WORD 3333
0202	Load Message Counter.	WORD 00FD
—17	Start Transfer.	BYTE 02

FIGURE 14B. BC SET-UP WRITTEN IN BASIC

(CPU  
ADDRESS)

0000-0001		
	01	40
0006-0007		
	01	80
000E-0007		
	00	00
0200-0201	00	FP
0202-0203		
0280 - 0281		
	00	80
	0C	21
	*	*
	*	*
	*	*
0300 - 0301		
	00	00
	18	23
	11	11
	22	22
	33	33
	*	*
	*	*

\*Left empty for RTU's response & LOOP WORD.

FIGURE 14C.  
BC SET-UP MEMORY MAP



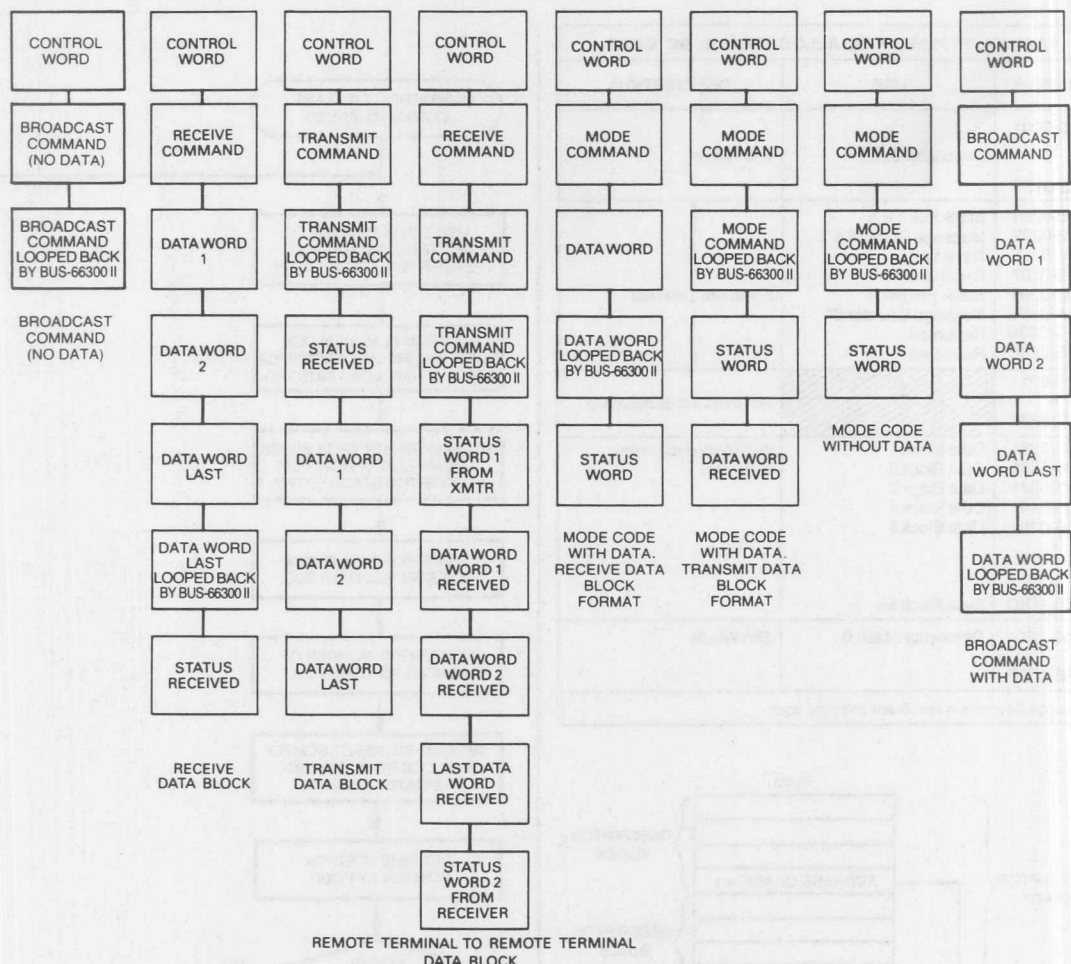
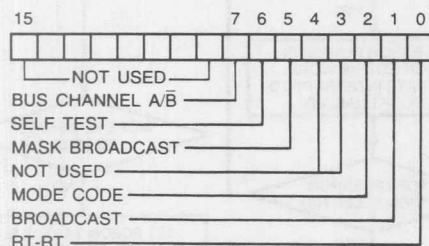


FIGURE 15. BC DATA BLOCK FORMATS



Note:

1. MASK BROADCAST XOR BROADCAST BIT in Status Word = STATUS SET ERROR.
2. When the BC expects the BROADCAST bit set in the Status Word, a logic 1 will mask the Status Interrupt Error flag.

FIGURE 16. BC CONTROL WORD

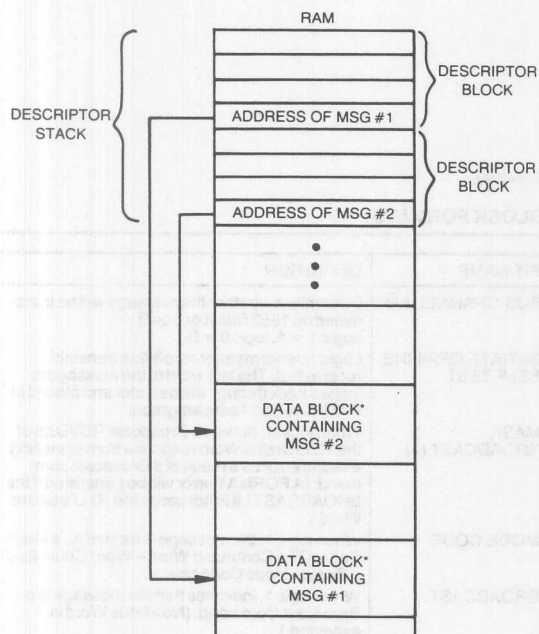
BIT NAME	DEFINITION
BUS CHANNEL A/B	Determines whether the message will be transmitted on 1553 Bus A or Bus B. Logic 1 = A, logic 0 = B.
INITIATE OFF-LINE SELF TEST	Logic 1 performs internal off-line transmit/receive test. The last word of the message is looped back through the decoder and placed in RAM. See Self Test paragraph.
MASK BROADCAST (1)	When logic 1, prevents Broadcast RCVD bit of the 1553 Status Word response from signalling a status error as a result of a Broadcast command. (A FORMAT error will be generated if the BROADCAST bit is not set on the RTU's Status Word.)
MODE CODE	When logic 1, the message is treated as a Mode Code. (The Command Word - Word Count field indicates Mode Code type.)
BROADCAST	When logic 1, indicates that the message is a Broadcast Command. (No Status Word is expected.)
RT-RT	When logic 1, the message is treated as an RT-RT transfer. (The next two words are Command Words.) Both Status Word responses are validated.



**TABLE 4. TYPICAL RAM ALLOCATION IN BC MODE**

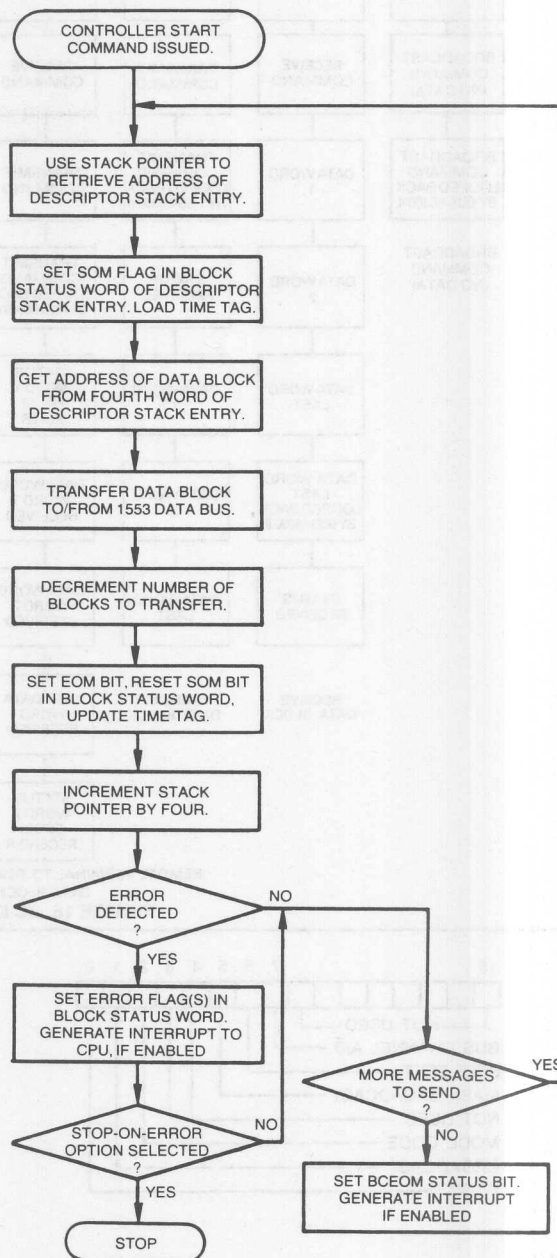
ADDRESS	USE	DESCRIPTION
0000-0001 ⋮ 01FE-01FF	Descriptor Stack A	256 Words
0200-0201 0202-0203 0204-0205 0206-0207 0208-0209 020A-020B 020C-020D 020E-020F	Stack Pointer A Message Counter A* Reserved Reserved Stack Pointer B Message Counter B* Reserved Reserved	Fixed Area of RAM
0210-0211 ⋮ 027E-027F		
0280-0281 0300-0301 0380-0381 0400-0401 0480-0481 ⋮ 1D80-1D81	Data Block 1 Data Block 2 Data Block 3 Data Block 4 Data Block 5 ⋮ Data Block 55	64 Words each in this example.
3E00-3E01 ⋮ 3FFE-3FFF	Descriptor Stack B	256 Words

\*Message Counters A and B are one byte each.



\*DATA BLOCKS NEED NOT BE CONTINUOUS AND MAY BE OF WHATEVER LENGTH IS SUFFICIENT TO HOLD THE PARTICULAR MESSAGE

**FIGURE 17. ORDERING MESSAGES IN BC MODE**



**FIGURE 18. BC SEQUENCE OF OPERATION  
(UNDER BUS-65522 CONTROL)**

## RTU MODE

The RTU mode is selected by issuing a RESET command and setting bits 15 and 14 of the 1553 Configuration Register to logic "1" and "0", respectively. The RTU Address of the BUS-65522 is defined by loading the desired value into the RTU Address Register. Note that bit 5 of the RTU Address Register must be programmed to implement odd parity.

**RTU INITIALIZATION.** For RTU operation, the user initializes the RAM, Stack Pointer, Look-Up Tables, and data to be transmitted to the BC. Table 5 lists a sample memory map for the RTU mode. The user follows the steps shown in Figure 19, RTU Initialization.

The BUS-65522 uses an indirect addressing architecture to determine where to store or retrieve the data required to service the commands received from the BC. The Stack Pointer indicates which block in the Descriptor Stack to use. The fourth word of the Descriptor Stack is used to store the received command word.

The T/R bit and the subaddress field of the command word will then be used to generate a pointer into the Look-Up Table, which contains the starting address of the data block to be used for transmitting or receiving information for the particular subaddress.

Two Stack Pointers, two Descriptor Stacks, and two Look-Up Tables are provided to allow the user to double buffer the RAM. All transfers to and from the 1553 Bus are made using the current Stack and Look-Up Tables as defined by the user through bit 13 of the Configuration Register.

The Stack Pointer should be initialized by the CPU with the starting address of the Descriptor Stack. This pointer must contain a word address (i.e., if the Stack is to begin at HEX (0400), the Stack Pointer should be initialized to 0200).

In the RTU mode, the Descriptor Stack occupies 256 contiguous words. It may be located anywhere in the non-fixed area of RAM, beginning a 256 word boundary (i.e., HEX 0000, 0700, 1000, XX00, etc.).

The Look-Up Table is loaded by the user with the addresses of the data blocks to be used for receiving or transmitting data from the particular subaddress. The first 32 words of each Look-Up Table should contain the word address of the data blocks to be used when receiving data. The next 32 words should contain the address to be used when transmitting data from the various subaddresses.

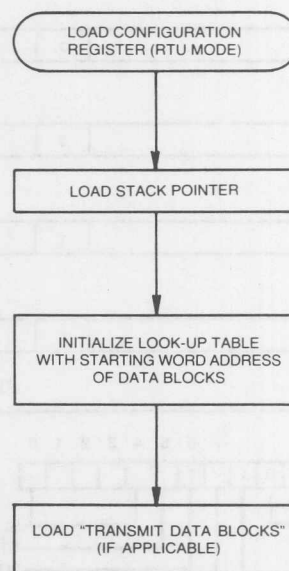
The Look-Up Table is sequentially ordered so that the first location refers to T/R = 0, Subaddress = 00000. The second location refers to T/R = 0 and Subaddress = 00001. The last location within the Look-Up Table refers to T/R = 1 and Subaddress = 11111 (see figures 20 and 21).

**RTU SOM SEQUENCE.** When a 1553 command is received, the BUS-65522 saves the command received in an internal register. Figure 22 illustrates the RTU Sequence of Operation once a 1553 command word is received. Once the command word is received, the BUS-65522 performs the following steps:

1. Reads the Stack Pointer to get the address of the current Descriptor Stack Entry.
2. Stores an SOM flag in the Block Status Word to indicate a transfer operation in progress.
3. Stores the Time Tag.
4. Stores the Command Word received.
5. Reads a Block address from the Look-Up Table using the T/R bit and the subaddress from the Command Word; transfers the Block address into an internal address register.

**RTU EOM SEQUENCE.** At the end of a 1553 message (valid or invalid), the BUS-65522 performs the following steps:

1. Updates the Block Status Word by resetting the SOM and setting the EOM and any error bits.
2. Updates the Time Tag.
3. Increments the Stack Pointer by four.
4. Generates an Interrupt if enabled.



**FIGURE 19. RTU INITIALIZATION  
(UNDER USER CONTROL)**

TABLE 5. TYPICAL RAM ALLOCATION IN RTU MODE

WORD ADDRESS	USE	DESCRIPTION
0000-0001 ⋮ 01FE-01FF	Descriptor Stack A	256 Words
0200-0201 0202-0203 0204-0205 0206-0207 0208-0209 020A-020B 020C-020D 020E-020F	Stack Pointer A Reserved Reserved Reserved Stack Pointer B Reserved Reserved Reserved	Fixed Area of RAM
0210-0211 ⋮ 027E-027F		Unused in this example.
0280-0281 ⋮ 02FE-02FF	Look-Up Table A	Fixed Area of RAM

TABLE 5. TYPICAL RAM ALLOCATION IN RTU MODE (Cont'd)

WORD ADDRESS	USE	DESCRIPTION
0300-0301 03FE-033F 0340-0341 037E-037F	Data Block 1 Data Block 2	32 Words in this example.
0380-0381 ⋮ 03FE-03FF	Look-Up Table B	Fixed Area of RAM
0400-0401 ⋮ 1EC0-1EC1 1EE0-1EEF	Data Block 3 ⋮ Data Block 97	
2F00-2F01 ⋮ 2FFE-2FFF	Descriptor Stack B	256 Words

COMMAND WORD RECEIVED

RTADR	T/R	SUBADDR	WORD COUNT
-------	-----	---------	------------

LOOK-UP POINTER

	T/R	Subaddress	0
Base Address (A or B)	X	XXXXX	0

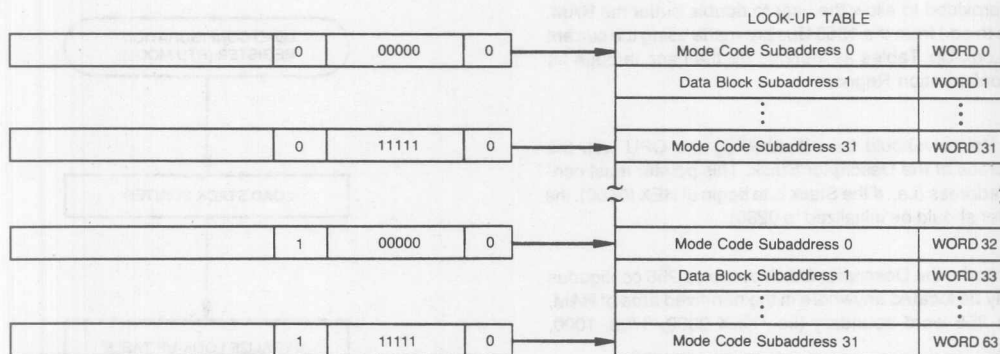


FIGURE 20. LOOK-UP TABLE SET-UP

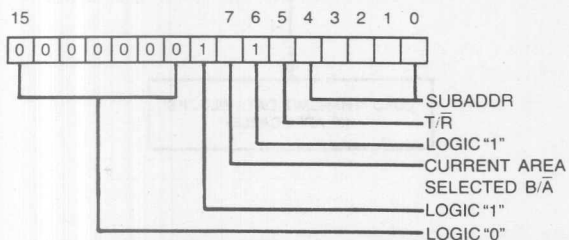


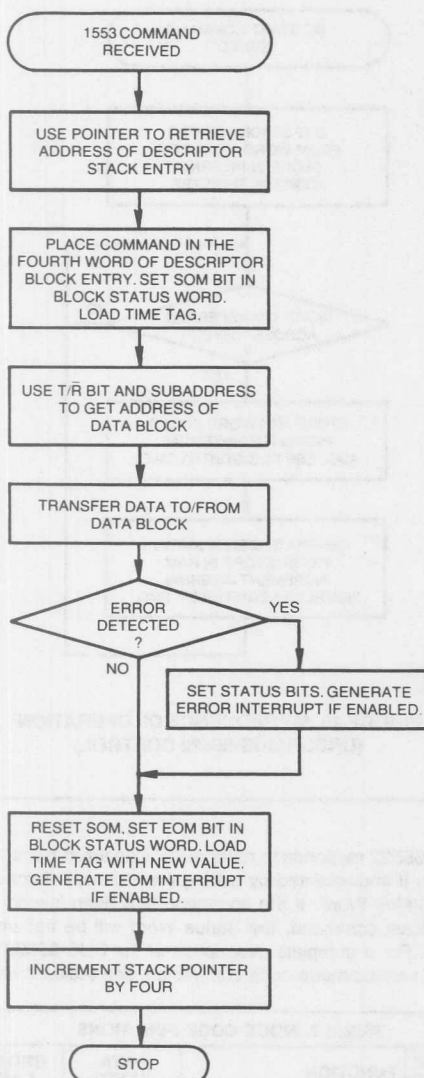
FIGURE 21. LOOK-UP TABLE POINTER

## MT MODE

The MT mode is selected by setting bit 15 of the Configuration Register to logic "0" and bit 14 to a logic "1".

**MT INITIALIZATION.** For MT operation, the user initializes the RAM as shown in table 6 and follows the steps shown in figure 23. MT Initialization.

The entire RAM is used as the MT stack. The user instructs the BUS-65522 where to store the first Identification Word by loading the starting word address in word 100 HEX of RAM.



**FIGURE 22. RTU SEQUENCE OF OPERATION (UNDER BUS-65522 CONTROL)**

To initiate reception of the 1553 bus traffic, the user issues a CONTROLLER START command by setting bit 1 of the Start/Reset Register to a logic "1". This causes the BUS-65522 to load the contents of either Stack Pointer A or B (as selected by the Configuration Register) into an internal address register. Once a word is received from the 1553 bus, the BUS-65522 stores this word at the address indicated by the internal address register. The contents of this register are then incremented by two to point to the next word in RAM.

The BUS-65522 generates an Identification Word for the received word and stores it in the RAM location indicated by the internal address register. The Address Register is again in-

cremented, in preparation for storing the next 1553 word. The RAM automatically wraps around from 2FFE-2FFF.

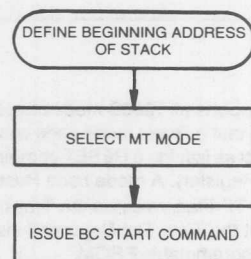
The Identification Word is generated by the BUS-65522 in order to provide the CPU with additional information regarding the received 1553 word (see figure 24).

The CPU can read the 1553 time tag/word count register to determine the number of data words and identification words received.

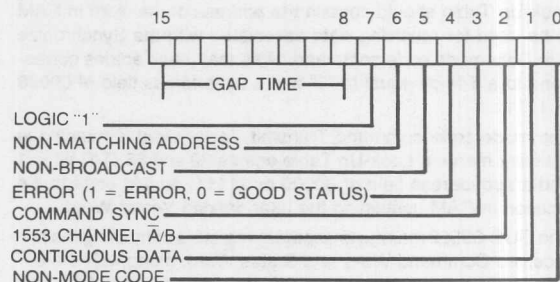
**TABLE 6. TYPICAL RAM ALLOCATION IN MT MODE**

WORD ADDRESS	DESCRIPTION
0000-0001	First Received 1553 Word
0002-0003	First Identification
0004-0005	Second Received Word
0006-0007	Second Identification
...	...
3FFE-3FFF	Word stored at 3FFE-3FFF followed by word stored at 0000.
...	...
0200-0201	Stack Pointer* A (Fixed area of RAM)
0208-0209	Stack Pointer* B (Fixed area of RAM)

\*Stack Pointers are read by the BUS-65522 upon executing a BCSTART command. It is overwritten by data in the course of acting as a MT.



**FIGURE 23. MT INITIALIZATION (UNDER USER CONTROL)**



Note: Each bit of the GAP TIME field represents 0.5  $\mu$ s.



NAME	DEFINITIONS
BIT 0	Non-Mode Code – Set to logic 1 if preceding 1553 word was a valid word, contained a command sync, and the subaddress field was any value other than 00000 or 11111. Set to '0' otherwise.
BIT 1	Contiguous Data – Logic "1" indicates that data received is contiguous and therefore associated with a message being received. Logic "0" = gap.
BIT 2	1553 Channel $\bar{A}/B$ – indicates which Bus the data was received on.
BIT 3	Command Sync – this will differentiate data from that of Command/Status sync types. Logic "1" = Command Sync.; "0" = Data Sync.
BIT 4	ERROR – this bit will be a logic 1 for an Error or 0 for a valid word received.
BIT 5	Non-Broadcast – Set to logic '1' if associated 1553 word was a valid word, contained a command sync, and the 5 MSB's (the RTU address) was any value other than 11111. Set to '0' otherwise.
BIT 6	THIS RT – Set to a logic '0' if the associated 1553 word was a valid word, received with a command sync and the 5 MSB's (the RTU address) match the RTU address defined for the device.
BIT 7	logic '1'
BIT 8-15	Gap time – Bit 15 (MSB) indicates the amount of gap time should Bit 1 indicate non contiguous data. Resolution is 0.5 $\mu$ s per LSB.

FIGURE 24. MT IDENTIFICATION WORD

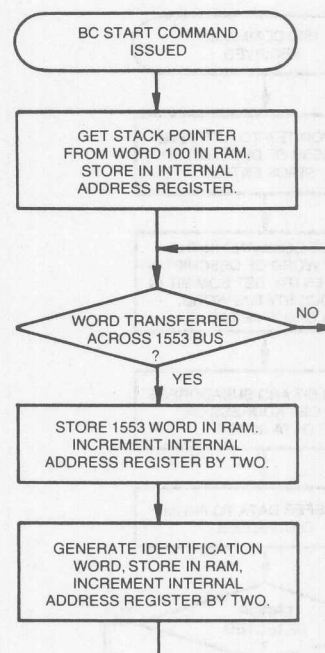


FIGURE 25. MT SEQUENCE OF OPERATION (UNDER BUS-65522 CONTROL)

## MODE CODES

The BUS-65522 supports all 1553B mode codes for dual redundant systems. Note that a Reset mode code command does not have the same effect as issuing a RESET command (setting bit 1 of the Start/Reset Register). A mode code Reset command will override the Inhibit TF Flag, override the Transmitter Shutdown condition, and reset the Time Tag Register if instructed to do so through the user programmable PROM.

A mode code with an associated data word and a  $T/\bar{R}$  bit set to "0" is handled the same as a receive operation. In the RTU mode, the  $T/\bar{R}$  bit and the subaddress field are used as pointers into the Look-Up Table. Thus, the 1st and 31st entries of the Look-Up Table should contain the address of the word in RAM to be used for receiving data associated with the Synchronize with Data mode code command. Note that these entries correspond to a  $T/\bar{R}$  bit equal to "0" and a subaddress field of 00000 or 11111.

The mode code command Transmit Vector word is handled in a similar manner. Look-Up Table entries 32 and 63 ( $T/\bar{R}$  bit = 1 and a subaddress field of 00000 or 11111) should point to the location in RAM containing the user defined Vector Word.

The BUS-65522 maintains separate registers containing the last received Command Word and Status Word, along with the BIT Word. It will automatically transmit these words to the BC when it receives a mode code command instructing it to do so.

The BUS-65522 responds to reserved or illegalized mode code commands if implemented by setting the Message Error bit in its 1553 Status Word. If the command had been issued as a non-broadcast command, the Status Word will be transmitted to the BC. For a complete description of the BUS-65522's response to various mode code commands, see tables 7 and 8.

TABLE 7. MODE CODE FUNCTIONS

T/R BIT	MODE CODE	FUNCTION	DATA WORD	BROADCAST
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	Yes
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag	No	Yes
1	00111	Override Inhibit Terminal Flag	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	10000	Transmit Vector Word	From Memory	No
0	10001	Synchronize with Data	To Memory	Yes
1	10010	Transmit Last Command	From Internal Register	No
1	10011	Transmit Bit Word	From Internal Register	No



TABLE 8. MODE CODES

## DYNAMIC BUS CONTROL (00000)

### MESSAGE SEQUENCE = DBC \* STATUS

The BUS-65522 responds with status. If the subsystem wants control of the bus, it must set DBACC within 2.5 $\mu$ s after NBGRT.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

## SYNCHRONIZE WITHOUT DATA WORD (00001)

### MESSAGE SEQUENCE = SYNC \* STATUS

The BUS-65522 responds with status. If sent as a broadcast, the broadcast receive bit will be set and status response suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

## TRANSMIT STATUS WORD (00010)

### MESSAGE SEQUENCE = TRANSMIT STATUS \* STATUS

The status and BIT word registers are not altered by this command and contain the resulting status from the previous command.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

## INITIATE SELF-TEST (00011)

### MESSAGE SEQUENCE = SELF-TEST \* STATUS

The BUS-65522 responds with a status word. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Short-loop test is initiated on the status word transmitted. If the test fails, an RT fail flag is generated.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).
5. **Faulty Test.** Bits set: terminal flag (SW), A/B Loop Test Fail, Current 1553 Bus (A or B) Loop Test Fail (BIT Word).

## TRANSMITTER SHUTDOWN (00100)

### MESSAGE SEQUENCE = SHUTDOWN \* STATUS

This command is only used with dual redundant bus systems. The BUS-65522 responds with status. At the end of the status transmission, the BUS-65522 inhibits any further transmission from the dual redundant channel. Once shutdown, the transmitter can only be reactivated by Override Transmitter Shutdown or RESET RT commands.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

\* = Status response time

#### **OVERRIDE TRANSMITTER SHUTDOWN (00101)**

##### **MESSAGE SEQUENCE = OVERRIDE SHUTDOWN \* STATUS**

This command is only used with dual redundant bus systems. The BUS-65522 responds with status. At the end of the status transmission, the BUS-65522 re-enables the transmitter of the redundant bus. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

##### **ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

#### **INHIBIT TERMINAL FLAG BIT (00110)**

##### **MESSAGE SEQUENCE = INHIBIT TERMINAL FLAG \* STATUS**

The BUS-65522 responds with status and inhibits further internal or external setting of the terminal flag bit in the status register. Once the terminal flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT command. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

##### **ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

#### **OVERRIDE INHIBIT TERMINAL FLAG BIT (00111)**

##### **MESSAGE SEQUENCE = OVERRIDE INHIBIT TERMINAL FLAG \* STATUS**

The RTU responds with status and reactivates the terminal flag bit in the status register. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

##### **ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

#### **RESET REMOTE TERMINAL (01000)**

##### **MESSAGE SEQUENCE = RESET REMOTE TERMINAL \* STATUS**

The BUS-65522 responds with status and internally resets. Transmitter shutdown, BIT word, mode commands, and inhibit terminal flag commands will be reset. If the command was broadcast, the broadcast received bit is set and the status word is suppressed.

##### **ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

#### **RESERVED MODE CODES (01001-01111)**

##### **MESSAGE SEQUENCE = RESERVED MODE CODES \* STATUS**

The BUS-65522 responds with status. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.

##### **ERROR CONDITIONS**

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), Illegal Mode Code (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

\* = Status response time

TABLE 8. MODE CODES (CONT'D)

## TRANSMIT VECTOR WORD (10000)

### MESSAGE SEQUENCE = TRANSMIT VECTOR WORD \* STATUS VECTOR WORD

The BUS-65522 transmits a status word followed by a vector word. The contents of the vector word (from the subsystem) are enabled onto DB0-DB15 with BUSREQ after the command transfer (same as data word in a normal transmit command).

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, (BIT Word).

## SYNCHRONIZE WITH DATA WORD (10001)

### MESSAGE SEQUENCE = SYNCHRONIZE DATA WORD \* STATUS

The data word received following the command word is transferred to the subsystem. The status register is then enabled and its contents transferred onto the data bus and transmitted. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), Low Word Count (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), T/R Error, High Word Count (BIT Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), High Word Count, T/R Error (BIT Word).

## TRANSMIT LAST COMMAND (10010)

### MESSAGE SEQUENCE = TRANSMIT LAST COMMAND \* STATUS LAST COMMAND

The status and BIT word registers are not altered by this command. The SW contains the status from the previous command. The data word transmitted contains the previous valid command (providing it was not another TRANSMIT LAST COMMAND).

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

## TRANSMIT BIT WORD (10011)

### MESSAGE SEQUENCE = TRANSMIT BIT WORD \* STATUS BIT WORD

The BUS-65522 responds with status followed by the BIT word. When activated, BITEN allows the subsystem to latch the BIT word on the parallel data bus. The BIT word is not altered by this command; however, the next SW will reflect errors in this transmission.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bit set: message error (SW).
3. **T/R bit Set to Zero.** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. **Zero T/R bit and Broadcast Address.** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. **Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

\* = Status response time

TABLE 8. MODE CODES (CONT'D)

## SELECTED TRANSMITTER SHUTDOWN (10100)

### MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA \* STATUS

The data word received is transferred to the subsystem and status is transmitted. No other action is taken by the BUS-65522. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Intended for use with RTs with more than one dual redundant channel.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count (BIT Word).

## OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101)

### MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA \* STATUS

The data word received after the command word is transferred to the subsystem. No other action is taken by the BUS-65522. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

#### ERROR CONDITIONS

1. **Invalid Command.** No response, command ignored.
2. **Command Not Followed by Data Word.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
4. **Command T/R bit Set to One.** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. **Command T/R bit Set to One and Broadcast Address.** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count, T/R Error (BIT Word).

## RESERVED MODE CODES

### MESSAGE SEQUENCE = RESERVED MODE CODE (T/R = 1) \* STATUS

#### RESERVED MODE CODE (T/R = 0) \* STATUS

The BUS-65522 responds with status. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

#### ERROR CONDITIONS (T/R = 1)

1. **Invalid Command.** No response, command ignored.
2. **Command Followed by Data Word.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

#### ERROR CONDITIONS (T/R = 0)

1. **Invalid Command.** No response, command ignored.
2. **Command not Followed by Contiguous Data Word.** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
3. **Command Followed by too many Data Words.** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

\* = Status response time



## SELF TEST

The BUS-65522 performs an automatic self test each time a 1553 message is processed. The last word transferred onto the 1553 bus for each message is "looped back" from the transmitter to receiver. An on-line comparison of the transmitted word and the received looped back word is then performed. If a discrepancy is detected, the Error bit in the Block Status Word is set, the Terminal Flag bit is set in the 1553 Status Word, and an error interrupt is generated to the CPU, if enabled.

In the BC mode, the looped back word is placed in the next sequential location of the message block in the on-board RAM, where it is available for the CPU to inspect. See the data formats in figure 15 for specific 1553 message types.

The BUS-65522 maintains a separate BIT (Built-In-Test) register which contains information regarding the last message transfer (see figure 26). In RTU mode, the contents of this register are automatically passed to the BC in response to a Transmit BIT Word mode code command.

The Initiated [off-line] self-test can be executed only when the BUS-65522 is configured as a Bus Controller. Set the Wrap-Around Test bit within the BC Control Word (logic '1') and initiate any standard message transfer. This inhibits the 1553 transceivers and initiates the wrap-around test (i.e., internal 1553 encoder output is fed back into the decoder - the word is then written into memory). See BC Operation and Figure 14, BC Control Word for more detail.

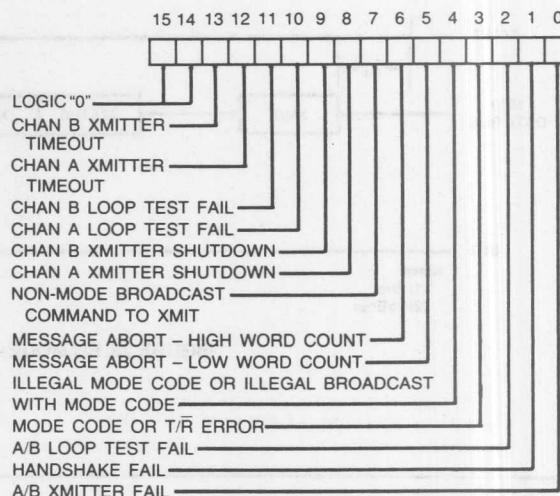


FIGURE 26. BUILT-IN-TEST (BIT) WORD

## BUS-65515 BC AND RTU MODE TIMING

Table 9 defines the times and lists the units for the following 11 timing diagrams.

TIME	DEFINITION	MIN	MAX	UNITS
$T_{st}$	Start timing (start to data on 1553)	3	4	$\mu S$
$T_{ei}$	EOM/Error Interrupt	5	7	$\mu S$
$T_{bi}$	BC EOM Interrupt	10	12	$\mu S$
$T_{ebo}$	EOM/Error Timeout Interrupt	19	21	$\mu S$
$T_{gp}$	Intermessage Gap (Mid parity to mid sync)	12	12	$\mu S$
$T_{gpto}$	Intermessage Gap (Timeout) (Mid parity to mid sync)	24	26	$\mu S$
$T_{rsp}$	Response Time (Mid parity to mid sync)	10	12.5	$\mu S$
$T_{ero}$	RT/RT Timeout Interrupt	19.5	20.5	$\mu S$

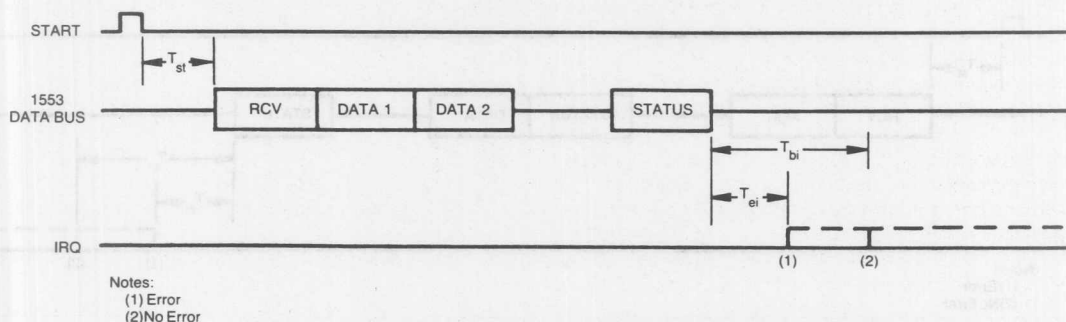


FIGURE 27. BC MODE - RECEIVE COMMAND



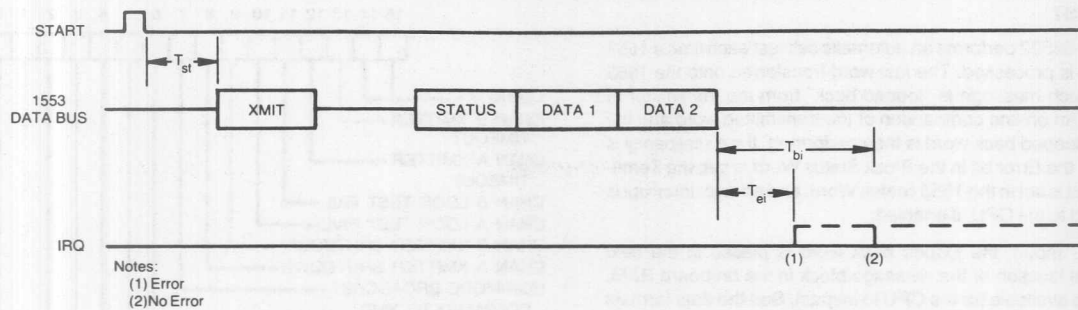


FIGURE 28. BC MODE - TRANSMIT COMMAND

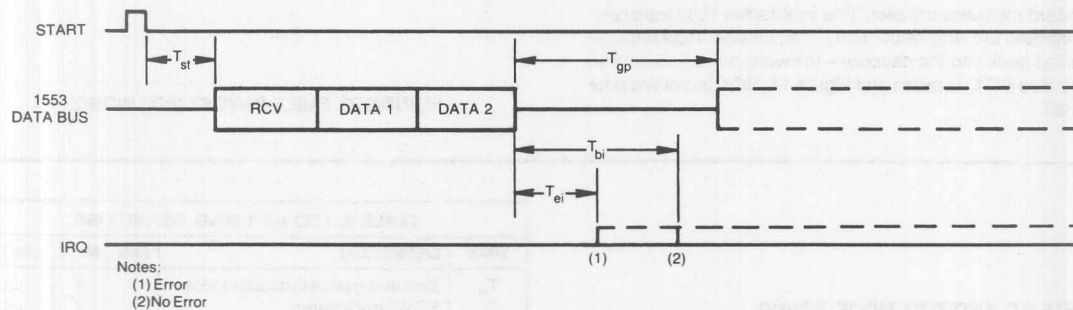


FIGURE 29. BC MODE - BROADCAST

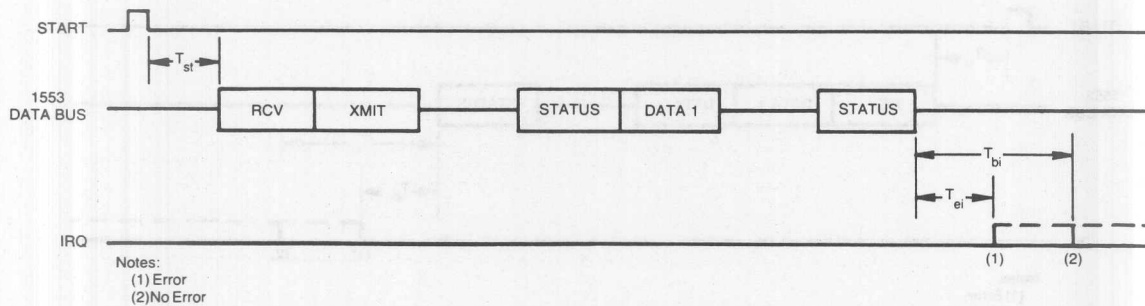


FIGURE 30. BC MODE - RTU TO RTU TRANSFER

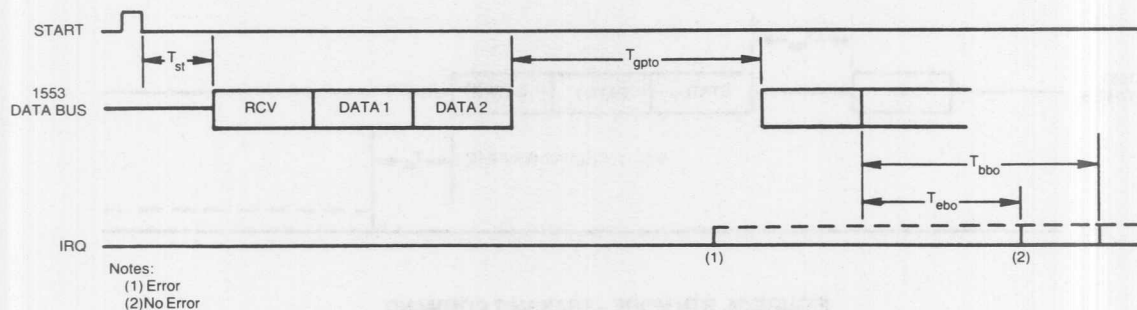


FIGURE 31. BC MODE - TIMEOUT

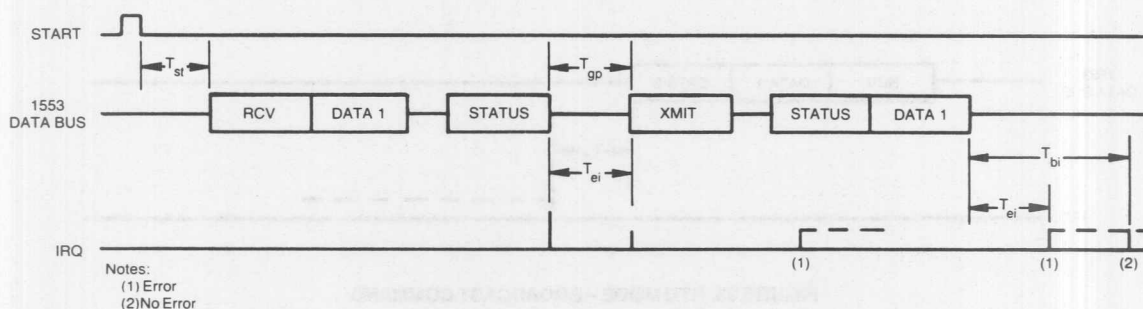


FIGURE 32. BC MODE - TWO COMMANDS

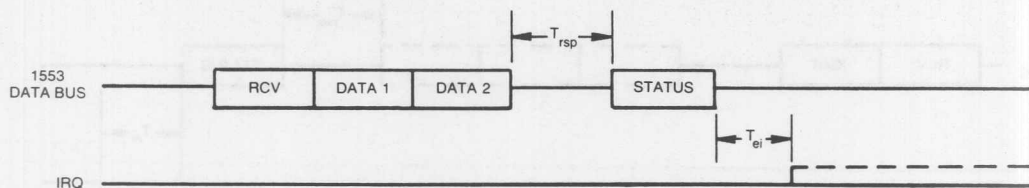


FIGURE 33. RTU MODE - RECEIVE COMMAND

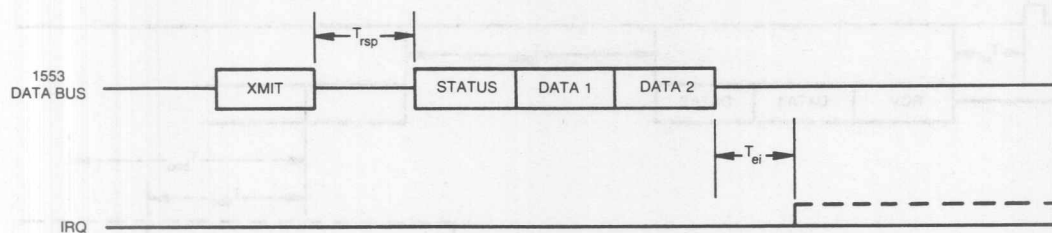


FIGURE 34. RTU MODE - TRANSMIT COMMAND

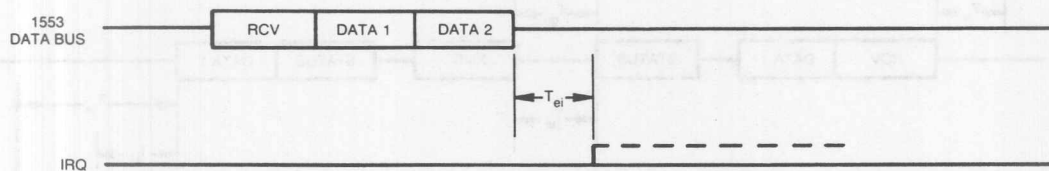


FIGURE 35. RTU MODE - BROADCAST COMMAND

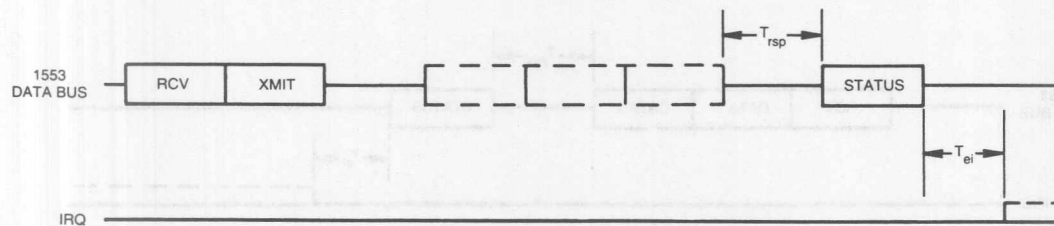


FIGURE 36. RTU MODE - RT/RT RECEIVE

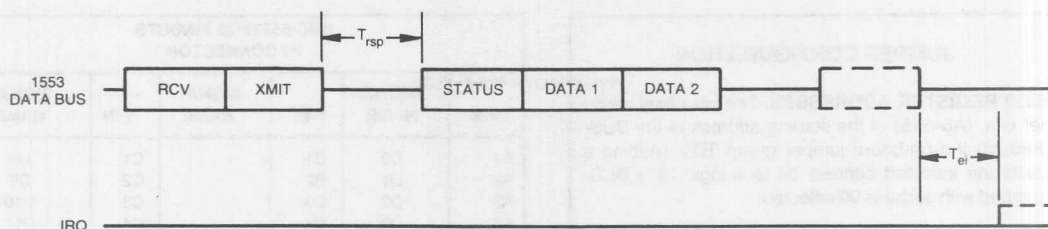


FIGURE 37. RTU MODE-RT/RT TRANSMIT

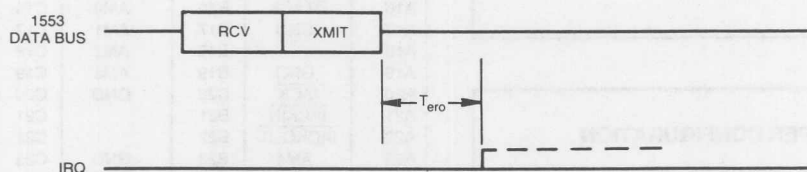


FIGURE 38. RTU MODE - RT/RT TIMEOUT

## INSTALLATION

**1553 COUPLING.** The BUS-65522 can be direct coupled or transformer coupled to the 1553 bus. The user selects the type of coupling desired through the on-board jumper groups TB1 and

TB2. The BUS-65522 comes equipped with two Bulkhead (front panel) connectors, Trompeter part no. BJ77 and mating connector Trompeter Cable Plug, part no. PL-75N.

Transformer coupled connections are also possible on the P2 connector, see TB6 and TB7 jumpers.

### TB1 JUMPER CONFIGURATION

**1553 CHANNEL A.** Connections selected by jumpers at TB1 BUS-65522 shipped with:

- (1) Transformer coupling selected.
- (2) Frame floating.

TB1-1	DC COUPLED +
TB1-2	XFM COUPLED +
TB1-3	XFM COUPLED -
TB1-4	DC COUPLED -
TB1-5	FRAME TO GROUND

### TB2 JUMPER CONFIGURATION

**1553 CHANNEL B.** Connections selected by jumpers at TB2 BUS-65522 shipped with:

- (1) Transformer coupling selected.
- (2) Frame floating.

TB2-1	DC COUPLED +
TB2-2	XFM COUPLED +
TB2-3	XFM COUPLED -
TB2-4	DC COUPLED -
TB2-5	FRAME TO GROUND

# BUS-65522 AND BUS-65523

## TB3 JUMPER CONFIGURATION

**BUS-65522 REGISTER ADDRESSES.** The user may select the upper bits, (A6-A15) of the starting address of the BUS-65522 through the on-board jumper group TB3. (Adding a jumper sets the selected address bit to a logic "0".) BUS-65522 shipped with address 00 selected.

TB3-1	ADDRESS A6
TB3-2	ADDRESS A7
TB3-3	ADDRESS A8
TB3-4	ADDRESS A9
TB3-5	ADDRESS A10
TB3-6	ADDRESS A11
TB3-7	ADDRESS A12
TB3-8	ADDRESS A13
TB3-9	ADDRESS A14
TB3-10	ADDRESS A15

## TB4 JUMPER CONFIGURATION

**32 ADDRESS SPACE SELECTION.** Adding a jumper to TB4 selects 32 Bit address bus. Removing the jumper selects 24 Bit address bus.

## TB5 FACTORY LOOP TEST BIT

No Jumper = Normal operation  
With Jumper = Factory loop test enabled

## TB6 (P2) OPTIONAL 1553 P2 COUPLING (CHANNEL B)

TB6-1	BUS B + P2 (C4)
TB6-2	BUS B - P2 (C8)
TB6-3	SHIELD P2 (C5)

## TB7 (P2) OPTIONAL 1553 P2 COUPLING (CHANNEL A)

TB7-1	BUS A + P2 (C24)
TB7-2	BUS A - P2 (C20)
TB7-3	SHIELD P2 (C25)

## BUS-65522/23 PINOUTS P1 CONNECTOR

PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
A1	D0	B1		C1	D8
A2	D1	B2		C2	D9
A3	D2	B3		C3	D10
A4	D3	B4		C4	D11
A5	D4	B5		C5	D12
A6	D5	B6		C6	D13
A7	D6	B7		C7	D14
A8	D7	B8		C8	D15
A9	GND	B9		C9	GND
A10		B10		C10	
A11	GND	B11		C11	
A12	DS1	B12		C12	SYSRST
A13	DS0	B13		C13	
A14	WRITE	B14		C14	AM5
A15	GND	B15		C15	A23
A16	DTACK	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	AS	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	IACK	B20	GND	C20	A18
A21	IACKIN	B21		C21	A17
A22	IACKOUT	B22		C22	A16
A23	AM4	B23	GND	C23	A15
A24	A7	B24	IRQ7	C24	A14
A25	A6	B25	IRQ6	C25	A13
A26	A5	B26	IRQ5	C26	A12
A27	A4	B27	IRQ4	C27	A11
A28	A3	B28		C28	A10
A29	A2	B29		C29	A9
A30	A1	B30		C30	A8
A31	-12V	B31		C31	+12V
A32	+5V	B32	+5V	C32	+5V

## BUS-65522/23 PINOUTS P2 CONNECTOR

PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
A1		B1	+5V	C1	
A2		B2	GND	C2	
A3		B3		C3	
A4		B4	A24	C4	BUS B POS
A5		B5	A25	C5	BUS B SHIELD
A6		B6	A26	C6	
A7		B7	A27	C7	
A8		B8	A28	C8	BUS B NEG
A9		B9	A29	C9	
A10		B10	A30	C10	
A11		B11	A31	C11	
A12		B12	GND	C12	
A13		B13	+5V	C13	
A14		B14		C14	
A15		B15		C15	
A16		B16		C16	
A17		B17		C17	
A18		B18		C18	
A19		B19		C19	



## BUS-65522 AND BUS-65523

BUS-65522/23 PINOUTS (CONT)					
P2 CONNECTOR					
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
A20		B20		C20	BUS A NEG
A21		B21		C21	
A22		B22		C22	
A23		B23		C23	
A24		B24		C24	BUS A POS
A25		B25		C25	BUS A SHIELD
A26		B26		C26	
A27		B27		C27	
A28		B28		C28	
A29		B29		C29	
A30		B30		C30	
A31		B31	GND	C31	
A32		B32	+5V	C32	

**1553 FRONT PANEL CONNECTORS** (Trompeter BJ77 mates with PL75-Bayonet) reference J1 & J2 connectors.

## J1

Center Conductor – BUS A POS  
Ring – BUS A NEG  
Frame – Shield

## J2

Same as J1 for 1553 Bus B Channel 1.

## ORDERING INFORMATION

BUS-65522

- Power Supply Option:  
2 =  $\pm 12\text{V}$  to  $\pm 15\text{V}$  1553B  
3 =  $\pm 12\text{V}$  to  $\pm 15\text{V}$  supplies (MACAIR)

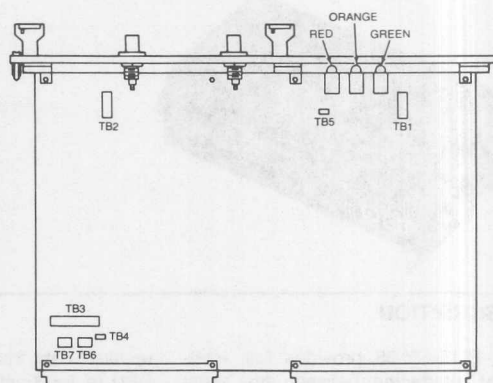


FIGURE 39. JUMPER CONNECTIONS

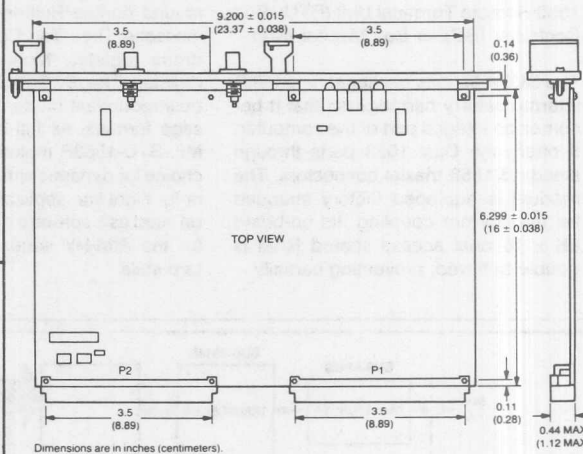
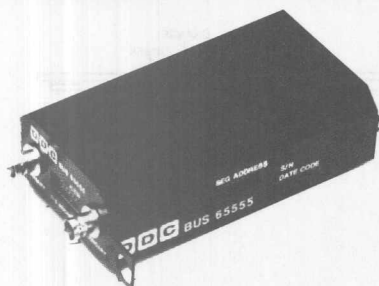


FIGURE 40. MECHANICAL OUTLINE



## MIL-STD-1553 RTU/BC/MT MODULE FOR GRiD<sup>®</sup> RUGGEDIZED LAPTOP PC

### FEATURES

- MIL-STD-1553B RTU/BC/MT INTERFACE FOR GRiD 1520, 1530, AND 1535 SERIES RUGGEDIZED LAPTOP PC'S
- SMALL SIZE & LOW POWER
- SUPPORTS ALL 1553B DUAL REDUNDANT MESSAGE FORMATS AND MODE CODES, OPTIONAL ILLEGIZATION PROM
- DYNAMIC WRAP-AROUND ON-LINE BUILT-IN-TEST
- ON-BOARD TIME TAG COUNTER & MT WORD COUNTER
- DEDICATED 8K x 16 DUAL ACCESS RAM
- SOFTWARE I/O REGISTERS
- MEMORY MAPPED INTERFACE
- SOFTWARE PROGRAMMABLE RTU ADDRESS AND DATA ALLOCATIONS
- LEVEL 5, INTERRUPT PROVIDED

### DESCRIPTION

The BUS-65555 provides full, intelligent interfacing between the serial dual redundant MIL-STD-1553B Data Bus and the rugged GRiD 1520, 1530, and 1535 series laptop XT/AT<sup>®</sup> compatible computers. Software controls the BUS-65555's operation as either a 1553 Remote Terminal Unit (RTU), Bus Controller (BC), or Bus Monitor (MT).

The BUS-65555 is packaged in a GRiD internal battery cartridge so that it becomes an integral part of the computer. It offers the Dual 1553 ports through standard 1553 triaxial connectors. The module is equipped factory strapped for transformer coupling. Its on-board 8K x 16 dual access shared RAM is double buffered, preventing partially

updated data from being read by the CPU or transmitted to the 1553 Data Bus. The base address of the registers and the onboard shared RAM is user selectable by DIP switches.

Additional features include a wrap-around on-line Built-In-Test, on-board message Time Tag Counter, RTU address register, Monitor word count register. The BUS-65555 supports all dual redundant mode codes and message formats. Its full compliance with MIL-STD-1553B makes it an excellent choice for dynamic simulation in the lab or for flight line applications. It can also be used as a software development tool for the AIM-HY series MIL-STD-1553 terminals.

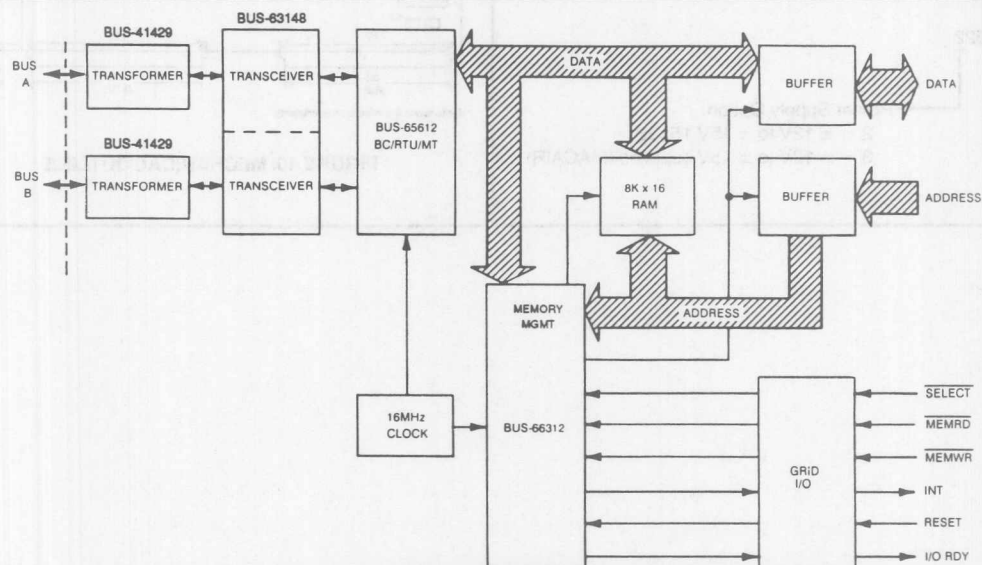


FIGURE 1. BUS-65555 BLOCK DIAGRAM

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© GRiD and GRiDCASE are registered trademarks of GRiD Systems Corporation.

**TABLE 1. BUS-65555 SPECIFICATIONS**

Specifications at nominal power supply voltages and 25°C.

PARAMETERS	UNIT	VALUE
LOGIC	V	2.4
V <sub>OH</sub>	V	0.4
V <sub>OL</sub>	μA	40
I <sub>IH</sub>	mA	1.6
I <sub>IL</sub>		2
V <sub>IH</sub>	V	0.6
V <sub>IL</sub>	V	
<b>POWER SUPPLIES</b>		
Voltage, Current Drain	V, Amps	+5.0 +10% ,1.70 max
<b>TEMPERATURE RANGE</b>		
Operating (Case)	°C	0 to +70
Storage	°C	-65 to +150
<b>PHYSICAL CHARACTERISTICS</b>		
Size	in (cm)	2.9 x 1.45 x 5.5 (7.4 x 3.7 x 13.97)

**Table 3. SEGMENT ADDRESS SWITCH ASSIGNMENT**

SWITCH	ADDRESS
SW-1	A19 (MSB)*
SW-2	A18 *
SW-3	A17
SW-4	A16
SW-5	A15 (LSB)
SW-6	N.A.

\* selected for memory mapping  
C000. A15 assignment selects  
segment C000 or C800.

**TABLE 2. REGISTERS/DECODER ADDRESS DEFINITION**

OFFSET BYTE ADDRESS IN HEX	DEFINITION	R/W	CLEARED BY RESET COMMAND
:4000	Interrupt Mask Register	R/W	YES
:4001	Illegal	—	—
:4002	Illegal	—	—
:4003	Configuration Register	R/W	YES
:4004	Illegal	—	—
:4005	Illegal	—	—
:4006	Start/Reset Register	W	—
:4007	Illegal	—	—
:4008	RTU Address Register	R/W	NO
:4009	Illegal	—	—
:400A	Time Tag Register (byte 0)*	R	YES
:400B	Time Tag Register (byte 1)*	R	YES
:400C	Interrupt Reset Command Register	W	YES
:400D	Illegal	—	—
:400E	External EOM Command Register	W	NO
:400F	Illegal	—	—

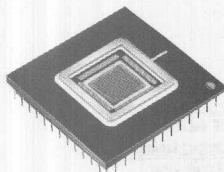
\* in MT mode this becomes a 16 bit word count register.

## CONTACT FACTORY FOR:

- 1) Interactive Menu Driven Software
- 2) Operations Manual

## ORDERING INFORMATION

**BUS-65555**



**CONTACT FACTORY  
FOR MORE  
INFORMATION**

## MIL-STD-1553 BUS CONTROLLER REMOTE TERMINAL AND BUS MONITOR

### DESCRIPTION

The BUS-65612 is a 16 MHz single chip dual redundant MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), and Bus Monitor (MT). Packaged in a Pin Grid Array (PGA), the BUS-65612 performs all the functions required to interface a MIL-STD-1553 dual redundant serial data bus transceiver, such as DDC's BUS-63125, and a subsystem parallel three-state data bus.

Using a single DDC custom monolithic SOS IC, the BUS-65612 features pin-for-pin and functional BUS-65600 compatibility, user initiated self-test, and low power consumption.

Compatible with most microprocessors, the BUS-65612 provides a 16 bit three-state parallel data bus and uses direct memory access (DMA type) handshaking for subsystem transfers.

All message transfer timing, DMA, and control lines are provided internally; thereby reducing the subsystem overhead associated with message transfers.

The BUS-65612 implements all dual redundant MIL-STD-1553 mode codes. In addition, any mode code may (optionally) be illegalized through the use of an external PROM. Complete error detection is provided by the BUS-65612 for BC and RTU operation. Error detection includes: response time-out, inter-message gaps, sync, parity, Manchester, word count, and bit count. The BUS-65612 is fully compliant with MIL-STD-1553 and operates over the full military temperature range of -55°C to +125°C - making it an excellent choice for MIL-STD-1553 applications.

### FEATURES

- COMPLETE BC, RTU, OR MT OPERATION
- 16 MHz SINGLE CHIP BUS-65600 REPLACEMENT
- CMOS-SOS TECHNOLOGY
- PGA PACKAGES
- IMPLEMENTS ALL DUAL REDUNDANT MODE CODES
- SELECTIVE MODE CODE ILLEGALIZATION AVAILABLE
- BC CHECKS STATUS WORD FOR CORRECT ADDRESS AND SET FLAGS
- DMA HANDSHAKING FOR SUBSYSTEM MESSAGE TRANSFERS
- CONTINUOUS ON-LINE AND INITIATED BUILT-IN-TEST

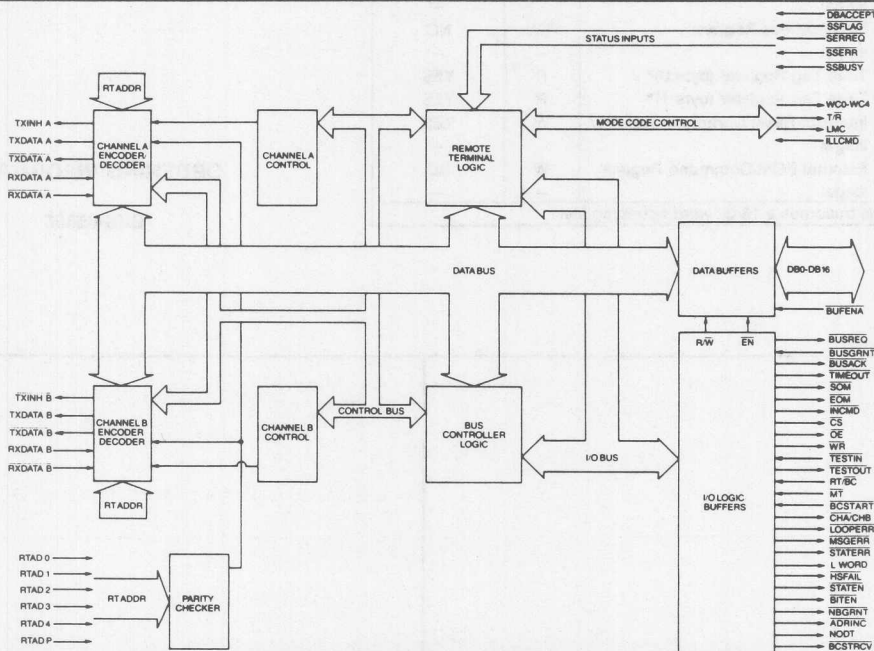


FIGURE 1. BUS-65612 BLOCK DIAGRAM

TABLE 1. BUS-65612 PIN FUNCTIONS (PGA)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
A01	TIM2	C05	ARX
A02	ANBRQ	C06	TESTENA
A03	PCLK	C07	VSS
A04	ARX	C08	RTAD1
A05	BRX	C09	VDD
A06	PARENA	C10	BRO
A07	RTADPAR	C11	NW
A08	RTAD3	C12	LMC
A09	RTAD0	C13	SA3 MC3
A10	CLKRST	D01	DB10
A11	ND	D02	DB12
A12	VW	D03	DB15
A13	VA	D11	RTFAIL
B01	VDD	D12	SA2 MC2 B8
B02	LOOPERR	D13	SA0 MC0 B6
B03	RTPARERR	E01	DB08
B04	TEST1	E02	DB09
B05	BRX	E03	DB11
B06	BROENA	E11	SA1 MC1 B7
B07	RTAD4	E12	WC4 CWC4 B5
B08	RTAD2	E13	WC3 CWC3 B4
B09	CLK	F01	DB05
B10	TIM1	F02	DB06
B11	MC	F03	DB07
B12	CMD	F11	WC2 CWC1 B3
B13	SA4 MC4	F12	WC1 CWC1 B2
C01	DB13	F13	WC0 CWC0 B1
C02	DB14	G01	DB02
C03	TD	G02	DB04
C04	BNRBQ	G03	DB03

TABLE 1. BUS-65612 PIN FUNCTIONS (PGA) (Continued)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
K03	ATX	N01	VSS
K11	BUFENA2	N02	TS0
K12	BUSGRNT	N03	LWORD
K13	ILLCMD	N04	OE
L01	BTX	N05	CS
L02	CYCENA	N06	INCMD
L03	MT	N07	ERROR
L04	TEST2	N08	ADRINC
L05	R/W	N09	BUSACK
L06	SOM	N10	BUSREQ
L07	EOM	N11	T/R
L08	CMDTRF	N12	GBR
L09	BITEN	N13	VSS
L10	STATEN	G11	WCMUXENA
L11	CSTINH	G12	VDD
L12	WRMASK	G13	SAMUXENA
L13	RESET	H01	DB01
M01	ATX	H02	DB00
M02	TS1	H03	TIMEOUT
M03	HSFAIL	H11	SVCQST
M04	STATSET	H12	SEL2
M05	WR	H13	SSFLAG
M06	INCMD	J01	TACT
M07	ME	J02	CHB/A
M08	DTSTR	J03	ATXINH
M09	TIMERR	J11	RTFLAG
M10	DBACC	J12	ADBC
M11	NBGRNT	J13	SSBUSY
M12	RT/BC	K01	BTXINH
M13	BUFENA1	K02	BTX

## ORDERING INFORMATION

BUS-65612-883B

Reliability Grade:

883B = Fully compliant with MIL-STD-883.

B = Screened to MIL-STD-883 without  
QCI testing

Blank = Standard DDC procedures

Packaging: PGA (Pin Grid Array)

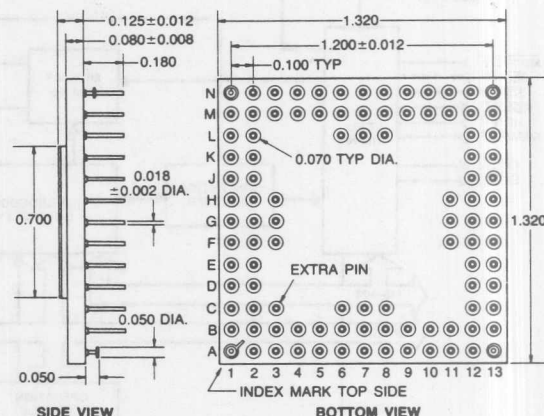
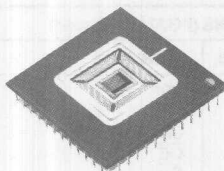


FIGURE 2. BUS-65612 MECHANICAL OUTLINE (PGA)



## MIL-STD-1553 TO MICROPROCESSOR INTERFACE UNIT



**REFER TO BUS-61553 FOR  
MEMORY MANAGEMENT  
DESCRIPTION AND TIMING.**

### DESCRIPTION

DDC's BUS-66312 MIL-STD-1553 to Microprocessor Interface Unit simplifies the CPU to 1553 Data Bus interface while offloading the CPU. It is packaged in a small PGA hermetically sealed.

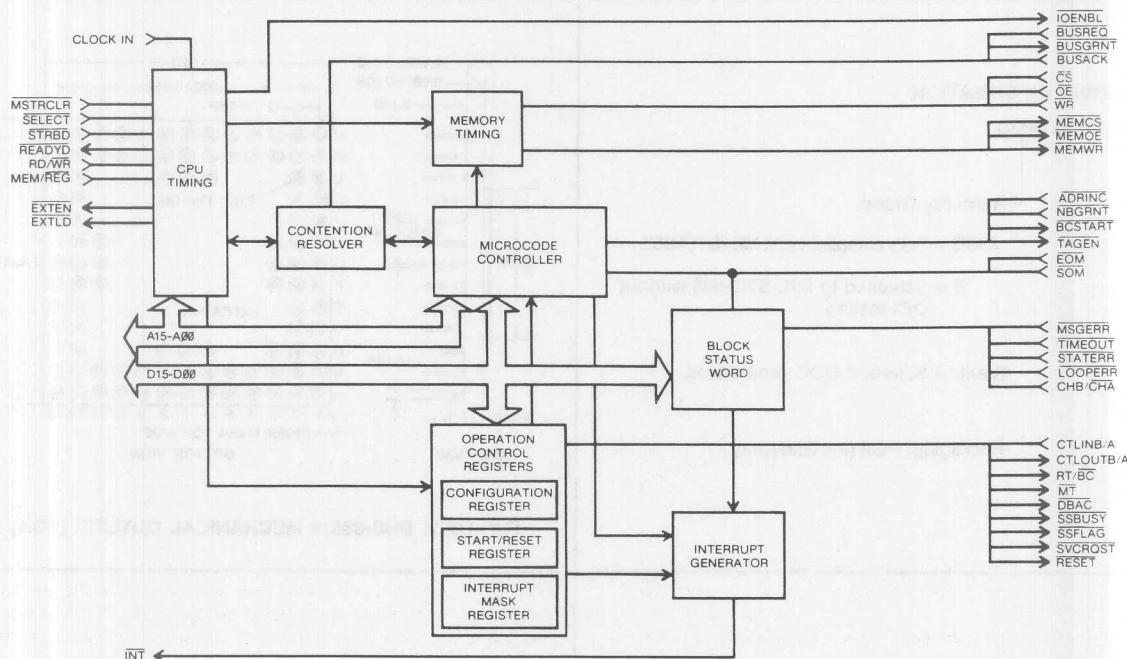
The BUS-66312 is designed to be used as an intermediary between the CPU and a MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU) or Bus Monitor (MT). The BUS-66312 provides a method for using a RAM accessible to both the CPU and the 1553 terminal. By using this shared RAM for operation, the CPU can transmit or receive 1553 traffic simply by accessing the shared memory.

The BUS-66312 allows all 1553 message transfers to be entirely memory or

I/O mapped. Thus the CPU's interface to this device is simple and hardware and software interfacing is minimal. The BUS-66312 supports 1553 interface devices such as DDC's BUS-65149 dual Universal RTU or the BUS-65612 dual BC, RTU, and MT. By operating autonomously, the BUS-66312 reduces CPU overhead for maintaining the 1553 interface. Available screened to MIL-STD-883, the BUS-66312 is ideal for demanding military and industrial microprocessor to 1553 interface applications. The BUS-66312 operates over the full military -55°C to +125°C temperature range.

### FEATURES

- COMPATIBLE WITH MIL-STD-1750 CPUs
- COMPATIBLE WITH MOTOROLA, INTEL, AND ZILOG CPUs
- COMPATIBLE WITH DDC BUS-65612 BC/RTU/MT AND BUS-65149 UNIVERSAL RTU
- MINIMIZES CPU OVERHEAD
- SIGNAL CONTROLS FOR SHARED MEMORY IMPLEMENTATION
- TRANSFERS COMPLETE MESSAGES TO SHARED MEMORY
- PROVIDES MEMORY MAPPED 1553 INTERFACE
- IBM PC® DEVELOPMENT CARD (BUS-65515) AVAILABLE



**FIGURE 1. BUS-66312 BLOCK DIAGRAM**

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**TABLE 1. BUS-66300 II SPECIFICATIONS**  
 Specifications at nominal power supply voltages.

PARAMETER	UNITS	VALUE
<b>Logic</b>		
$I_{IH}$ (With $V_{IH} = 2.7V$ )	$\mu A$	$\pm 10$
$I_{IH(1)}$ (With $V_{IH} = 2.7V$ )	$\mu A$	-630
$I_{IL}$ (With $V_{IL} = 0.0V$ )	$\mu A$	$\pm 10$
$I_{IL(1)}$ (With $V_{IL} = 0.0V$ )	$\mu A$	-700
$I_{OH}$	mA	4.0 min
$I_{OL}$	mA	4.0
$V_{IH}$	V	2.0
$V_{IL}$	V	0.8
$V_{OH}$	V	3.7
$V_{OL}$	V	0.4
<b>Clock</b>	MHz	12
<b>Power Supplies</b>		
Voltage	V	$5.0 \pm 10\%$
Current Drain	mA	10 typ
<b>Temperature Range</b>		
Operating (Case)	$^{\circ}C$	-55 to +125
Storage	$^{\circ}C$	-65 to +150
<b>Physical Characteristics</b>		
<b>Size</b>		
(78 pin DIP)	in (mm)	2.1 x 1.87 x 0.25 (53 x 47.5 x 6.4)
(82 pin flatpack)	in (mm)	2.1 x 1.87 x .25 (55.6 x 40.6 x 3.71)
<b>Weight</b>		
(78 pin DIP)	oz(g)	1 (28)
(82 pin flatpack)	oz(g)	1 (28)
Notes:		
(1) Values for 78 pin DIP pins 1, 2, 6, 10, 41, and 52; and 82 pin flatpack pins 2, 3, 4, 12, 20 and 25.		

## GENERAL

Many system designers do not want to halt their CPU's current operation in order to respond to an interrupt from a **BUS-65612** or **BUS-65149** in the time required to avoid a handshake failure (1.5 to 2.33 $\mu s$ ). The **BUS-66312** was designed to solve this problem by performing the required handshaking to the 1553 interface device, storing or retrieving the message(s) from a user supplied RAM and notifying the CPU that a 1553 transaction has occurred. The CPU uses this RAM to read the received data as well as to store messages to be transmitted onto the Bus. The **BUS-66312** arbitrates the access to the shared RAM between the 1553 front end and the CPU.

The **BUS-66312** can be used to implement BC, RTU, or MT operation and can be either memory mapped or I/O mapped to CPU address space. Registers internal to the **BUS-66312** control its operation.

In addition, the **BUS-66312** can access up to four external, user supplied registers. These registers can be used to define the RTU Address of the device or capture the Built-In-Test (BIT) Word from the 1553 interface device.

The **BUS-66312** can address up to 64K words of RAM. The RAM selected must be a non-latched static RAM capable of meeting the timing constraints of the **BUS-66312**. The RAM is used by the **BUS-66312** to implement Stacks and Look-Up Tables as well as to store 1553 messages. A double buffering architecture is provided to prevent incomplete or partially updated information from being transmitted onto the 1553 Data Bus.

The specific allocation of the RAM depends upon the operating mode selected by the CPU. Details are provided in the BC, RTU, and MT sections.

The **BUS-66312** requires an external, user supplied clock (8 to 16MHz max.). The waveforms provide in this data sheet are calculated based on a clock frequency of 12MHz. When using a 12MHz clock, a static RAM with a maximum 55ns access time is recommended.

## COMPATIBLE MICROPROCESSOR TYPES

The **BUS-66300 II** may be used with most common microprocessors, including, but not limited to, the Motorola 68000 family, the Intel 8080 family, Zilog Z8000 products, and the available MIL-STD-1750 processors. It can also implement byte transfers with a minimal amount of external circuitry. Consult the factory for details.

Interfacing the **BUS-66312** to the 1553 Data Bus requires external circuitry such as DDC's **BUS-65612** (BC/RTU/MT), **BUS-63125-641** (dual transceiver), and **BUS-25679** (transformer).

## MEMORY MANAGEMENT

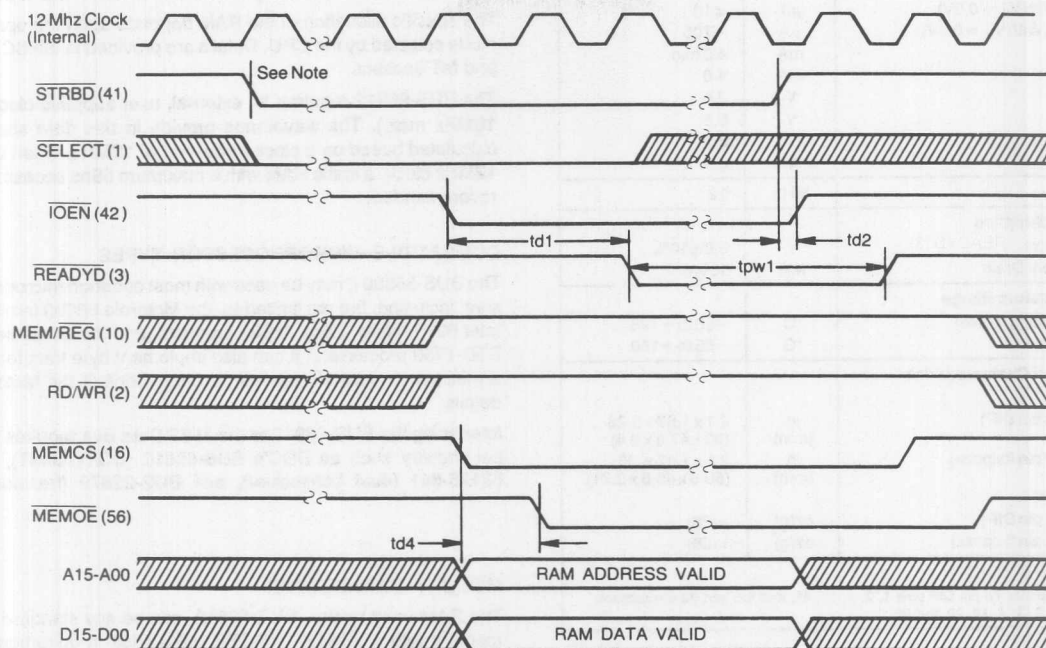
The RAM used by the **BUS-66312** can be any standard static memory with a WRITE STROBE pulse width requirement less than 55ns. The RAM area is broken down into pointers, look-up tables, and data blocks. All 1553 operation control is accomplished through the RAM, including fault monitoring and data block transfers.

For most applications, a 4K x 16 memory is sufficient to store the number of messages, but the **BUS-66312** can access up to 64K words.

**DOUBLE BUFFERING.** A Double Buffering system is available to prevent partially updated data blocks from being read by the CPU or transferred onto the 1553 Data Bus. To use Double Buffering the CPU must divide the RAM into two areas: "current" and "non-current." Two Stack Pointers, Descriptor Stacks, and Look-Up Tables are required to be used by the CPU.

The 1553 device has access only to the current area of RAM, and will use the current Descriptor Stack and Look-Up Table. While the 1553 device is processing messages using the current area pointers, the CPU can be setting up the next set of messages in the non-current area of RAM.

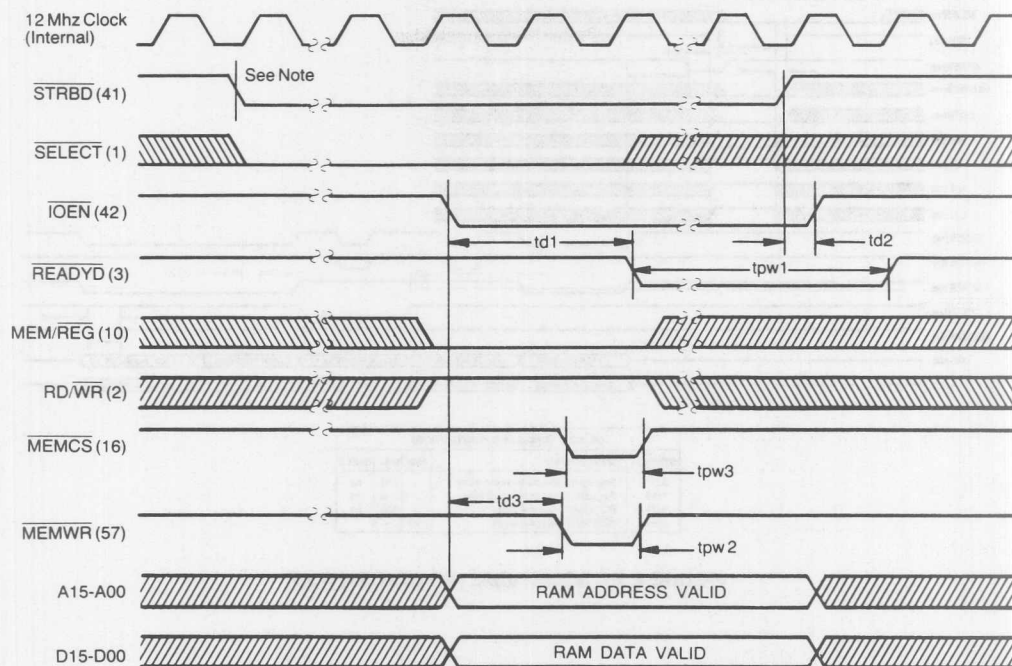
Once an EOM or BCEOM occurs, the CPU can swap the current and non-current areas by toggling bit 13 of the Configuration Register (see register section for description). The 1553 device will then have access to the new current area. Meanwhile, the CPU can begin processing the data received during the previous transfer or can begin setting up the next set of 1553 messages.



Note:  
STRBD to IOEN (low) delay is two clock cycles. If contention occurs,  
delay is two clock cycles following release of bus.

CPU READS FROM RAM				
SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td1	READYD low delay (CPU Handshake)	—	200	ns
td2	IOEN high delay (CPU Handshake)	—	20	ns
tpw1	READYD pulse width (CPU Handshake)	70	—	ns
td4	CPU MEMOE low delay	—	115	ns

FIGURE 2. CPU READS FROM RAM TIMING

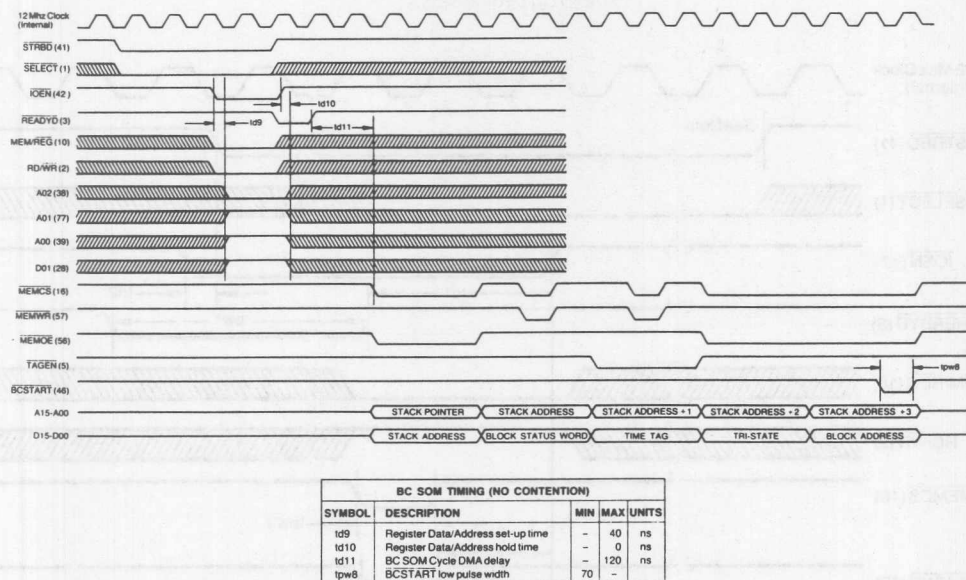


**Note:**

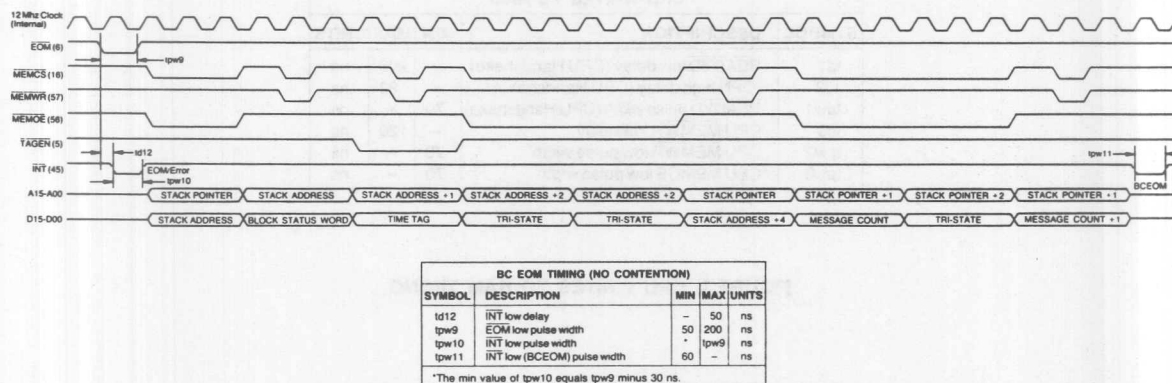
STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus.

CPU WRITES TO RAM					
SYMBOL	DESCRIPTION	MIN	MAX	UNITS	
td1	READYD low delay (CPU Handshake)	—	200	ns	
td2	IOEN high delay (CPU Handshake)	—	20	ns	
tpw1	READYD pulse width (CPU Handshake)	70	—	ns	
td3	CPU MEMWR low delay	—	120	ns	
tpw2	CPU MEMWR low pulse width	70	—	ns	
tpw3	CPU MEMCS low pulse width	70	—	ns	

**FIGURE 3. CPU WRITES TO RAM TIMING**

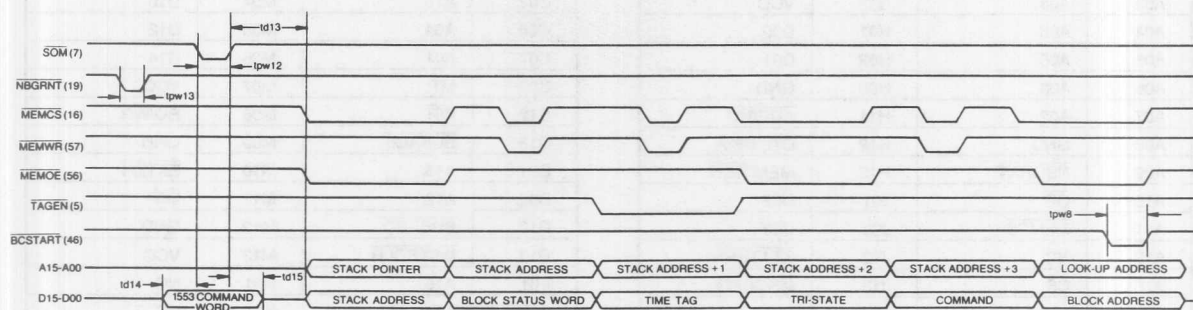


**FIGURE 4. BC SOM TIMING (NO CONTENTION)**



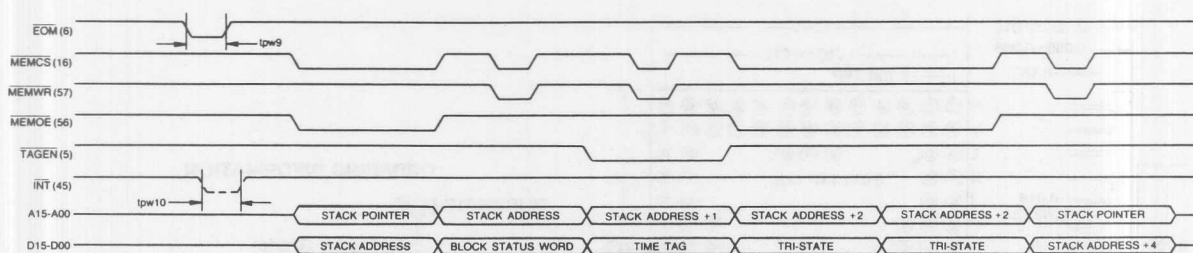
**FIGURE 5. BC EOM TIMING (NO CONTENTION)**





RTU SOM TIMING (NO CONTENTION)				
SYMBOL	DESCRIPTION	MIN	MAX	UNITS
Id13	RTU SOM Cycle DMA delay	-	200	ns
Id14	1553 Command Word set-up time	60	-	ns
Id15	1553 Command Word hold time	60	-	ns
tpw8	BCSTART low pulse width	70	-	ns
tpw12	SOM low pulse width	50	200	ns
tpw13	NBGRNT low pulse width	50	200	ns

FIGURE 6. RTU SOM TIMING (NO CONTENTION)



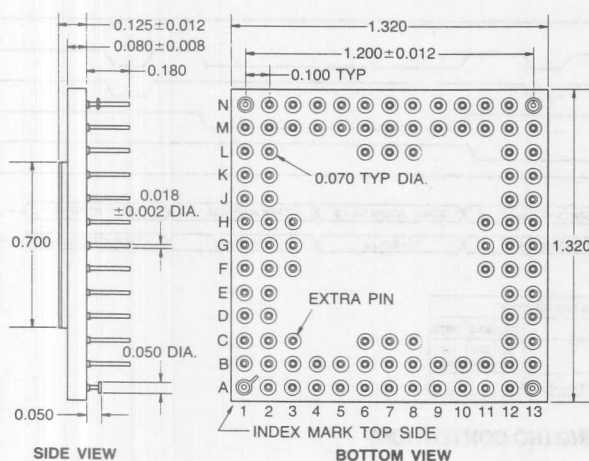
RTU EOM TIMING (NO CONTENTION)				
SYMBOL	DESCRIPTION	MIN	MAX	UNITS
tpw9	EOM low pulse width	50	200	ns
tpw10	INT low pulse width	*	tpw9	ns

\*The min value of tpw10 equals tpw9 minus 30 ns.

FIGURE 7. RTU EOM TIMING (NO CONTENTION)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
A01	NC	G11	GND
A02	A09	G12	CTLOUTB/ $\bar{A}$
A03	A08	G13	VCC
A04	A06	H01	D00
A05	A05	H02	D01
A06	A03	H03	GND
A07	A02	H11	ADRINC
A08	GND	H12	CTLINB/ $\bar{A}$
A09	NBGRNT	H13	MEM/REG
A10	$\bar{OE}$	J01	D02
A11	MEMCS	J02	D03
A12	NC	J12	STATERR
A13	$\bar{CS}$	J13	MSGERR
B01	NC	K01	D04
B02	GND	K02	D05
B03	NC	K12	SOM
B04	A07	K13	RESET
B05	GND	L01	VCC
B06	VCC	L02	D07
B07	A00	L06	D13
B08	ADDRDIR	L07	DDIR
B09	MEMWR	L08	IOENBL
B10	MEMOE	L12	EOM
B11	NC	L13	BCSTART
B12	GND	M01	D06

PIN NO.	FUNCTION	PIN NO.	FUNCTION
B13	BUSGRNT	M02	GND
C01	A11	M03	D08
C02	A10	M04	D10
C06	A04	M05	D12
C07	A01	M06	D14
C08	MT	M07	VCC
C12	WR	M08	RD/WR
C13	BUSACK	M09	GND
D01	A13	M10	EXTEN
D02	A12	M11	INT
D12	BUSREQ	M12	GND
D13	MSTRCLR	M13	VCC
E01	A15	N01	NC
E02	A14	N02	NC
E12	LOOPERR	N03	D09
E13	TIMEOUT	N04	D11
F01	SSBUSY	N05	GND
F02	DBAC	N06	D15
F03	RTU/BC	N07	SELECT
F11	CLOCKOUT	N08	STRBED
F12	CLKSEL	N09	READYD
F13	CLOCKIN	N10	EXTLD
G01	SSFLAG	N11	CHB/CHA
G02	VCC	N12	TAGEN
G03	SVCQST	N13	NC



## ORDERING INFORMATION

BUS-66312-883B

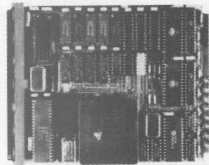
Reliability Grade:

883B = Fully compliant with MIL-STD-883

B = Screened to MIL-STD-883 but without QCI testing.

Blank = Blank = 0° to 70° C

FIGURE 8. BUS-66312 MECHANICAL OUTLINE



## MIL-STD-1750A CPU SEM E CARD WITH MIL-STD-1553 RTU/BC/MT

### DESCRIPTION

The BUS-67007, Microcomputer SEM E card, provides a general purpose, single chip, 16 bit CMOS microprocessor designed for high performance floating point and integer arithmetic, with extensive real time environment support conforming to the MIL-STD-1750A instruction set architecture. The PACE 1750A microcomputer and on-board 32K x 16 of EPROM offers the user an embedded system controller that can be used as a generic 1750A processor with a full, intelligent dual redundant MIL-STD-1553 RTU/BC/MT terminal. Its RS-422 port facilitates software development and system integration.

The BUS-67007 is packaged on a standard SEM E card with a 150 pin connector. Its on-board 8K x 16 SRAM

supports the 1750A CPU. The separate internal 8K x 16 dual access shared RAM of the BUS-61555 AIM-HY supports the 1553B messages, preventing partially updated data from being read by the CPU or transmitted to the 1553 Data Bus. The AIM-HY off-loads the microprocessor from the tasks of 1553 communication protocol and offers the host additional RAM for program or data.

The card is equipped with 8 L.E.D.'s which gives visual BIT feedback as to the CPU self-test, unrecoverable errors, software errors, RS-422 status, EPROM status, SRAM status, 1553 terminal self-test status, and the CPU watch-dog timer status. The BUS-67007, requires 5 volt DC power, with a total power dissipation under 5 watts.

### FEATURES

- MIL-STD-1750A CPU CARD (PACE MICROPROCESSOR) AND MIL-STD-1553 TERMINAL (BUS-61555, 5V AIM-HY)
- 16K WORDS RAM, 32K WORDS EPROM ON CARD
- RS-422 PORT FOR SOFTWARE DEVELOPMENT AND DEBUG
- VISUAL BIT (8 L.E.D.s)
- LOW POWER, < 5 WATTS, +5 VDC

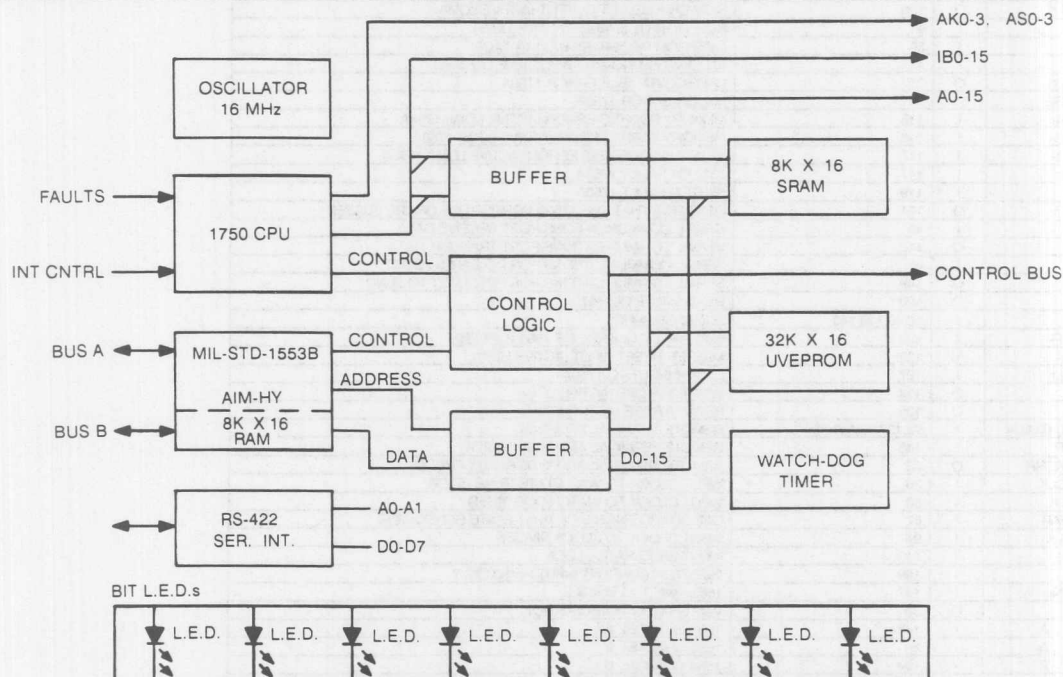


FIGURE 1. BUS-67007 BLOCK DIAGRAM

TABLE 1. PIN-OUTS

SIGNAL NAME	TYPE	PIN NUMBER	DESCRIPTION
IB0 - IB15	I/O	6,56,7,57,8,9,59,60,11,61, 12,62,17,63,125,126	INFORMATION BUS MULTIPLEXED ADDRESS AND DATA. USED AS DATA BUS OFF MODULE (IB0 = MSB) TRI-STATE
A0 - A15	O	139,138,24,74,25,75,26,76,20, 70,21,71,22,72,23,73	ADDRESS BUS (A15 = MSB) TRI-STATE
AK0 - AK3 A50 - A53	O	105,106,107,108 111,112,113,114	EXTENDED ADDRESS BUS TRI-STATE
PA0 - PA7 PB0 - PB7 PC0 - PC2	I/O	34,33,32,31,81,82,83,84 48,49,131,100,99,98,47 146,44,45,97	PARALLEL I/O PA0 - PB7 CAN BE DEFINED AS INPUT OR OUTPUT BY 8 BITS. PC0 - PC2 OUTPUT ONLY
16CLKOUT		85	16 MHz CLOCK OUTPUT
1.8MOUT		86	BAUD RATE CLOCK OUTPUT
100KHZ		27	100KHz OUTPUT
8MCLK-1MCLK		128,28,78,79	8,4,2,1 MHz CLOCK OUTPUTS (SYNCHRONOUS)
IOINT1,JOINT2		14,13	I/O INTERRUPTS
INT2 - INT5	I	66,65,16,64	GENERAL INTERRUPTS
POINT		122	POWER DOWN INTERRUPT
CONREQ-	I	2	CONSOLE REQUEST ACTIVE LOW
BSGNT-	I	3	INDICATES THAT THIS 1750A MAY USE THE BUS
M IO	O	4	INDICATES MEMORY OR I/O ACCESS
RDYD	I	5	INDICATES DATA CYCLE IS READY TO TERMINATE
RDYA	I	55	INDICATES ADDRESS CYCLE IS READY TO TERMINATE
D I	O	54	INDICATES A DATA OR INSTRUCTION ACCESS
TRGRST-	O	53	PULSED RESET FROM 1750A PROGRAM CONTROL (ACTIVE LOW)
BSLOCK-	I/O	52	INDICATES THAT THE BUS CANNOT BE ACCESSED (ACTIVE LOW)
SNEW	O	51	INDICATES AN OPCODE FETCH FROM 1750A
RESET-	O	104	SYSTEM RESET OUTPUT (ACTIVE LOW)
DAEN-	I	69	TRI-STATE CONTROL FOR DATA BUS (ACTIVE LOW)
STRBD-	O	58	DATA STROBE (ACTIVE LOW)
STRBA	O	67	ADDRESS STROBE (ACTIVE HIGH)
LR W	O	68	LATCHED READ WRITE CONTROL
ANALOG GND	I	15	ANALOG GROUND
-15VDC	I	38	ANALOG INPUT SUPPLY -15VDC
+15VDC	I	133	ANALOG INPUT SUPPLY +15VDC
UNUSED	NA	129,130	
CSRAMO-	O	37	RAM CHIP SELECT OUTPUT (ACTIVE LOW)
CSRAMI-	I	88	RAM CHIP SELECT INPUT (ACTIVE LOW)
LROMCS-	I	90	LOW BYTE ROM CHIP SELECT INPUT (ACTIVE LOW)
HROMCS-	I	142	HIGH BYTE ROM CHIP SELECT (ACTIVE LOW)
CSROM-	O	136	ROM CHIP SELECT OUTPUT (ACTIVE LOW)
OE-	I	91	ROM OUTPUT ENABLE (ACTIVE LOW)
VPP	I	89	UVEPROM PROGRAMMING VOLTAGE
A14IN	I	41	ALLOWS EEPROM TO BE USED IF DESIRED
ERROR1	O	35	UNRECOVERABLE ERROR 1750A
ERROR2	O	77	MAJOR ERROR 1750A
MPERR-	I	115	MEMORY POINTER ERROR (ACTIVE LOW) 1750A
MPAERR-	I	116	MEMORY PARTY ERROR (ACTIVE LOW) 1750A
XAERR-	I	117	EXTERNAL ADDRESS ERROR (ACTIVE LOW) 1750A
SFLT0	I	117	SYSTEM FAULT 1750A
SFLT1	I	119	SYSTEM FAULT 1750A
BSREQ-	O	121	INDICATES THAT THE 1750A DESIRES USE OF THE BUSES
REC	I	46	SERIAL COMMUNICATIONS PORT RECEIVE DATA
XMIT	O	148	SERIAL COMMUNICATIONS PORT TRANSMIT DATA
CTS	I	46	SERIAL COMMUNICATIONS PORT CLEAR TO SEND
RTS	O	149	SERIAL COMMUNICATIONS PORT REQUEST TO SEND
R W	O	120	READ WRITE OUTPUT
GND	I	10,40,110,140	LOGIC GROUND
BUFDIR-	I	123	EXTERNAL CONTROL OF 1553 BUFFERS
RESIN-	I	132	MASTER RESET INPUT (ACTIVE LOW)
CPUCLK	I	127	CLOCK INPUT TO 1750A
WE-	O	134	WRITE STROBE (ACTIVE LOW)
RD-	O	135	READ STROBE (ACTIVE LOW)
RTAD0-RTAD4	I	92,137,42,141,93	REMOTE TERMINAL ADDRESS
RTADP	I	145	REMOTE TERMINAL ADDRESS PARITY
RTPARERR-	O	96	REMOTE TERMINAL ADDRESS PARITY ERROR
WAITCLK	I	36	INPUT CLOCK TO WAIT STATE GENERATOR
WDCLK	I	80	INPUT CLOCK TO WATCH-DOG TIMER
EXTWAIT	I	87	OFF BOARD ENABLE OF WAIT STATE GENERATOR
16MCLK	I	94	INPUT CLOCK TO CLOCK DIVIDER
1.8MIN	I	143	INPUT BAUD RATE CLOCK
INJIN	I	109	INJECTOR CURRENT INPUT F9450 ONLY
TAGEN-	I	147	1553 TIME TAG ENABLE
WD	O	30	WATCH-DOG TIMER OUTPUT
DATA A	I	144	1553 CHANNEL A
DATA A-	I	39	1553 CHANNEL A
DATA B	I	124	1553 CHANNEL B
DATA B-	I	43	1553 CHANNEL B
VCC	I	1,50,101,150	LOGIC SUPPLY +5VDC

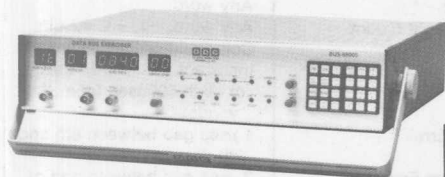
Table 2. VISUAL BIT  
L.E.D.s

FUNCTION	COLOR
CPU SELF-TEST	GREEN
ERROR CODE 1	RED
ERROR CODE 2	RED
RS-422 STATUS	GREEN
EPROM STATUS	GREEN
SRAM STATUS	GREEN
1553 STATUS	GREEN
WATCH-DOG	GREEN

## ORDERING INFORMATION

BUS-67007

## MIL-STD-1553 DATA BUS EXERCISER



**IMPROVED POWER SUPPLY  
CONTACT FACTORY**

### DESCRIPTION

The BUS-68005 is a low cost portable instrument for testing and troubleshooting MIL-STD-1553A and 1553B systems. It provides full function simulation of Remote Terminal Unit (RTU) and Bus Controller (BC) operation. The BUS-68005 implements the protocol tests of the proposed SAE AE-9A Production Test Plan for Remote Terminals. These tests include RT Address, Word Count, Subaddress, Error Injection, Dual-Redundant Operation, Mode Commands, Status Word, Broadcast Messages, and RT to RT Transfers. BUS-68005 offers simple and flexible operation including either local programming via the front panel 24 pad keyboard and 10 character

alphanumeric display, or remote programming via an 8 bit parallel I/O port, RS-232, or IEEE-488 interfaces. The IEEE-488 interface is a Direct Memory Access (DMA) port, allowing for real-time operation. Additional features include error generation and error detection, single, repeat, or halt-on error operation modes, variable response time, variable message gap, variable transmitter amplitude, a real-time monitor port, programmable response time-out, and built-in self test. Its compact size, 3.47" x 14.5" x 17.0", and price/performance makes it a leader for test applications requiring BC and RTU simulation.

### FEATURES

- IMPLEMENTS PROTOCOL TESTS OF SAE AE-9 PROPOSED PRODUCTION TEST PLAN
- 1553A OR 1553B SYSTEM TESTS
- SIMULATES:  
BUS CONTROLLER  
MULTIPLE REMOTE TERMINALS
- REAL-TIME MONITOR OUTPUT
- ALL PARAMETERS MANUAL AND REMOTE PROGRAMMABLE:  
KEYBOARD/DISPLAY  
IEEE-488 WITH DMA  
RS-232  
8 BIT PARALLEL
- ERROR GENERATION/DETECTION
- VARIABLE TRANSMITTER
- LOW COST

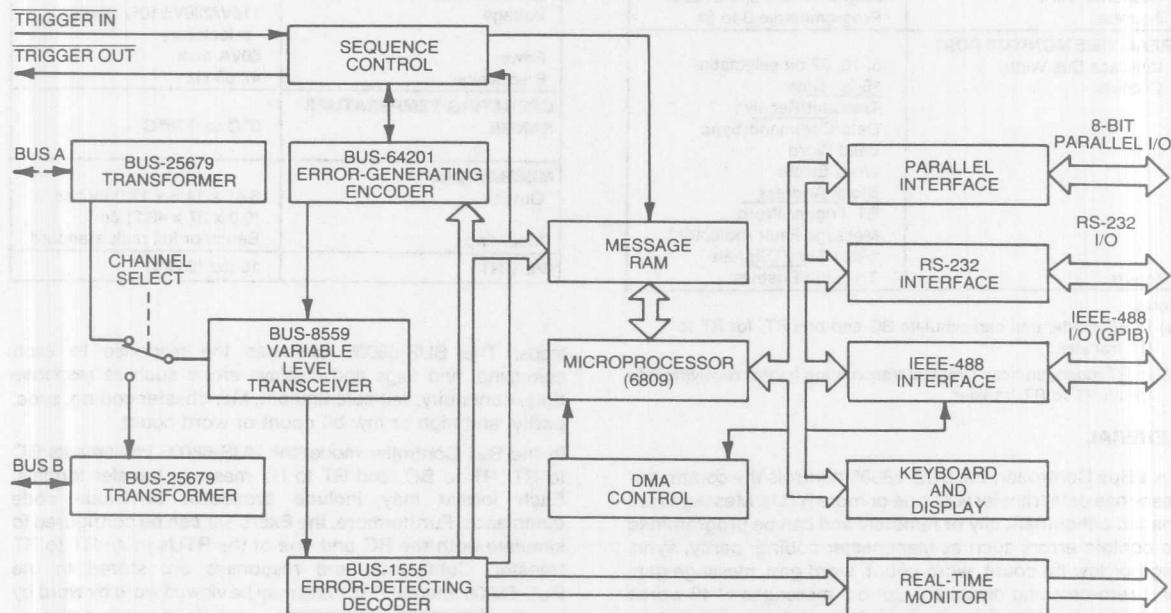


FIGURE 1. BUS-68005 BLOCK DIAGRAM



PARAMETER	VALUE
<b>DATA BUS INTERFACE</b>	
Channels	2 (user selectable)
Coupling	Direct (front panel) or stub (rear panel)
Transmitter	
Output Voltage	Programmable: 0 to 9.75Vpp nominal with 1 part in 256 resolution
Rise/Fall Time	200±20ns
Output Noise	10mVpp max (differential)
Receiver	
Input Voltage	40Vpp max (differential)
Input Impedance	4K $\Omega$ min (differential)
Threshold Level	1Vpp typ (direct coupled)
CMRR	40db min
<b>BUS CONTROLLER MODE</b>	
Message Formats (1)	RT to BC, BC to RT, RT to RT (with Mode Code and Broadcast)
Message Repetition	Single, Repeat, or Halt after a programmable number (1 to 99) of Errors
Messages Per Frame	Programmable 1 to 8
Words Per Message	Programmable 1 to 49
Intermessage Gap	Programmable 7 to 2047 $\mu$ sec
Frame Time	Programmable 2 to 500 ms
<b>REMOTE TERMINAL MODE</b>	
Message Formats (2)	RT to BC, BC to RT, RT to RT with Mode Code and Broadcast
Message Repetition	Single (1 to 8 messages) or Continuous
Simulated RTUs	Programmable 1 to 8
Response Time	Programmable 6 to 31 $\mu$ sec.
Address	Programmable 0 to 31
<b>REAL-TIME MONITOR PORT</b>	
Interface Bus Width	8, 16, 32 bit selectable
Outputs	16-Bit Data Transmit/Receive Data/Command Sync Valid Word Word Errors Block Address RT Trigger Word Message Fault Indicator "Real-Time" Signals Tri-State Enables
Inputs	

Notes:

- (1) In BC mode, unit can simulate BC and one RT, for RT to RT transfer.
- (2) In RT mode, unit can simulate transmitting and/or receiving RTs for an RT to RT transfer.

## GENERAL

As a Bus Controller, the BUS-68005 controls the command/response data transfer with one or more RTUs. Messages are loaded either manually or remotely and can be programmed to contain errors such as Manchester coding, parity, sync, high or low bit count, word count, word gap, message gap, and zero-crossing deviation. Up to 8 messages of 49 words each may be loaded at one time. Intermessage gap can be selected from 7 to 2047 microseconds, in 1 microsecond

<b>ERRORS GENERATED</b>	
Manchester Error	Any bit position
Parity Error	Any word
High or Low Bit Count	Any word, -1, +1, +2 bits
Sync Type Error	Command or Data Word
Sync Field Error	Incorrect first, third, fourth or sixth 500nsec time "window"
Word Gap Error	1 $\mu$ sec gap between 8th and 9th data bits
Message Gap Error	2 $\mu$ sec gap between end of current word to start of next word
Zero-Crossing Deviation Error	"Start of bit" time to "mid-bit" zero crossing: selectable 312.5, 375, 625, 687.5ns, any (single) data bit position
High or Low Word Count	Any message
Response Time Error	Any message
Format Error	Incorrect T/R bit any message
<b>ERRORS DETECTED</b>	
Manchester Error	
Parity Error	
Bit Count Error	
Word Count Error	
Sync Type Error	
Response Timeout	Programmable, 5 to 32 $\mu$ sec
Early Response Error	Less than 4 $\mu$ sec, per MIL-STD-1553B
Transmitter Timeout	800 $\mu$ sec
<b>REMOTE INTERFACES</b>	
8-Bit Parallel (3-State)	
IEEE-488 (DMA Port)	Standard on BUS-68005
RS-232	
<b>AC POWER INPUT</b>	
Voltage	115V/230V±10% (switch selectable)
Power	60VA max
Frequency	47-63 Hz
<b>OPERATING TEMPERATURE RANGE</b>	
	0°C to +70°C
<b>MECHANICAL</b>	
Outline	3.47 x 14.5 x 17.0 inches (9.0 x 37 x 43.2) cm
Mounting	Bench or full rack, standard
<b>WEIGHT</b>	18 lbs (8.2kg)

steps. The BUS-68005 evaluates the response to each command, and flags and displays errors such as response time, continuity, fail-safe timeout, Manchester coding, sync, parity, and high or low bit count or word count.

In the Bus Controller mode, the BUS-68005 implements BC to RT, RT to BC, and RT to RT message transfer formats. Each format may include broadcast or mode code commands. Furthermore, the Exerciser can be configured to simulate both the BC and one of the RTUs in an RT to RT transfer. Commands and responses are stored in the BUS-68005 internal RAM, and may be viewed word by word by means of the 10 character front panel alphanumeric display or the remote I/O ports.

As a Remote Terminal Unit, the BUS-68005 receives, validates, and stores data bus commands containing its (programmable) addresses. Up to 8 RTUs can be simulated at one time. Each simulated RT address may be mapped to one or more Exerciser memory blocks, allowing the Exerciser to transmit or receive multiple messages for the same RT in real-time. It responds to commands with status and data, as appropriate. Note that Status Words default to Clear Status via internal software, they may also be user programmed. Response time can be programmed from 6 to 31 microseconds, in 1 microsecond steps. Up to 8 messages of 49 words each may be stored at one time in the BUS-68005 internal RAM. These messages may be accessed via the keyboard for viewing on the front panel alphanumeric display.

In the Remote Terminal Unit mode, the BUS-68005 evaluates each command, and flags and displays errors, such as format, response timeout, fail-safe timeout, Manchester coding, parity, sync, and high or low bit count or word count.

The Exerciser also includes a real-time monitor output port. In addition to providing a 16-bit parallel representation of each 1553 word as it is transmitted or received in real-time, this port also provides indications of sync type, data direction, word errors, RT/Monitor "trigger" word flag, Exerciser message block number, and many other signals that may be used in various testing situations. The real-time monitor port may be utilized as either a passive monitor interface or as a high-speed parallel "window" to the BUS when the Exerciser is operating in either BC or RT mode.

Another feature included to support "real-time" operation is DMA capability for the IEEE-488 (GPIB) interface. This provides a direct, high-speed parallel link between a host computer with a DMA GPIB and the Exerciser's "message" and "trigger" RAMS.

The BUS-68005 is packaged in a 3.47 x 14.5 x 17.0 inch enclosure with a handle that can be used as a tilt-stand. It operates from either 115VAC or 230VAC 47-63Hz power. With its flexible manual or remote programmability and its error generation and detection, the BUS-68005 is ideal for simulation of Bus Controllers or Remote Terminal Units for bench, field, or factory test applications.

## SET-UP PROCEDURE

In order to insure correct operation of the BUS-68005, the following step-by-step set-up procedure is recommended:

- (1) Set the VOLTAGE SELECT switch on the rear panel of the BUS-68005 to the correct line voltage (115VAC or 230VAC) and connect the line cord to connector J1.
- (2) Figure 2(a) shows The BUS-68005 connections per MIL-STD-1553 and figure 2(b) illustrates non-system type testing. For MIL-STD-1553 applications, connect the triax cable(s) to Channel A and Channel B connectors (CH. A and CH. B on the front and rear panels). Direct coupled data bus connections are made to the front panel connectors and stub coupled data bus connections are made to the rear panel. For non-system type testing, a 35 Ohm resistor across the DATA and DATA\* terminals may be used.

- (3) Connect J2 (Parallel I/O), J3 (RS-232), and/or J4 (IEEE-488) remote interface cables to the rear panel connectors. Set I/O SELECT switch S8.
- (4) Connect REAL-TIME MONITOR/TRIGGER cable to J15.
- (5) Plug in the line cord and set the POWER switch to ON.
- (6) Observe the front panel display indications:

DISPLAY	LED'S	INTERVAL
RANDOM	RANDOM	1 second
BLANK	OFF	1 second
88 88 8888 88	ON	1 second
PASS	OFF	1 second
— — — — XX *		1 second
IT 01 0840 00	DEFAULT	FIXED

\*indicates software revision level

The BUS-68005 performs a complete internal self-test upon power turn-on. First, the front panel display and LEDs are checked, then a wraparound test is performed which checks 1553 encoder, decoder, PROM, and RAM.

After the PASS indication appears, the display and LEDs show the power-on default state of the BUS-68005. The LEDs show Local operation in the BC mode, with "Single" Frame Operation. The display shows Block 1, with Transmit Direction, Word 1, default command word, and no errors injected. The default command word (0840) is a receive command for 32 words to RTU address #1 and subaddress #2.

In the event that the power-on self-test yields a failure, the display will be fixed with a FAIL indication and a two digit error code. The meaning of the error codes is as follows:

ERROR CODE	FAILURE
40	Encoder/decoder wraparound test
20	RT trigger RAM test
10	Message RAM test
08	RPOM #4 checksum
04	PROM #3 checksum
02	PROM #2 checksum
01	PROM #1 checksum

Troubleshooting procedures are detailed in the BUS-68005 Instruction Manual. Also included is an internal diagnostic software routine for use in the event of a failure of the encoder/decoder wrap-around test. If it is desired to isolate the source of the self-test failure, or to program the BUS-68005 after a self-test failure has occurred, the CLR key must be depressed to reset the instrument.

## MANUAL PROGRAMMING

Manual programming of the BUS-68005 Exerciser is a straightforward operation that is illustrated in Figure 3, Flow Diagram.

A functional description of each programming key is listed in Table 2. Table 3 lists the message formats and their corresponding two digit entries, which are used as part of the CNTL FRMT key entry sequence programming. Table 4, Transmitted Word Errors, is a chart indicating how to program the 8-bit "Error" byte, (PROG key entry) and the 8-bit "Error Modifier" byte (ER BP key entry) in order to induce various word error conditions. Table 5 is a chart of error codes, which are displayed on the front panel as part of the READ key sequence when checking the BUS-68005 internal memory. Figure 5, Timing Diagram (BC Mode) shows a typical message block and frame repetition.

## BUS-68005 OPERATION UNDER HOST COMPUTER CONTROL

All BUS-68005 functions controlled by the front panel may be programmed from a host computer using any of the three remote I/O interfaces. The BUS-68005 remote I/O command set is divided into three major subgroupings. This allows the user to mix or match, depending on application, between ease of programmability and maximum throughput speed. The three major subgroupings are as follows:

- (1) Low Speed Commands. A set of 33 commands each containing a two-letter ASCII mnemonic, and, for 15 commands, either alpha, HEX, or decimal ASCII data. The Low Speed commands provide full control of all BUS-68005 functions and user-friendly interactive operation using a dumb RS-232 CRT terminal.
- (2) High Speed Commands. A set of four commands each containing a single character ASCII mnemonic. In two of the commands, the character is followed by parameters and data formatted in binary bytes. Two commands provide run/halt control for the BUS-68005 1553 processor. The other two provide a pseudo (software) DMA mechanism for transferring blocks of message data between the host computer (using any I/O port) and the BUS-68005 message RAM.

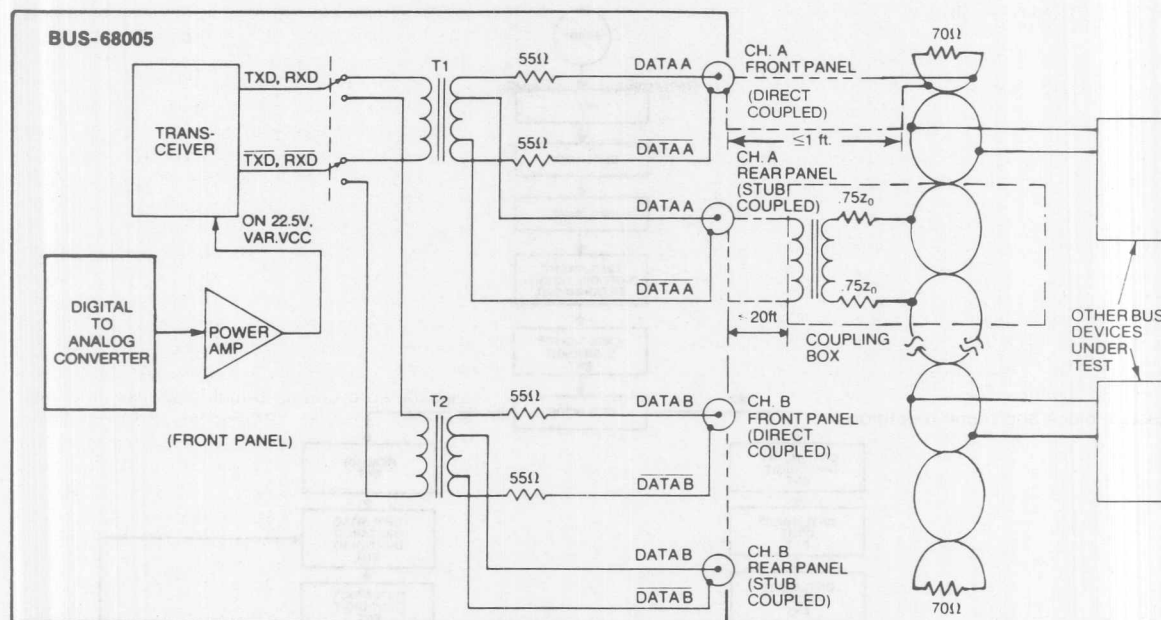
Using the IEEE-488 (GPIB) interface, the total time required to invoke a high-speed GO! command, defined as the time from the start of the GPIB handshake sequence to the start of BC transmission on the 1553 Bus, is approximately 2.5 ms.

- (3) IEEE-488 DMA Commands. Two commands which use the BUS-68005 IEEE-488 port's DMA capability. The host computer can directly access memory and registers in the BUS-68005's 1553 processor; this allows the I/O data path to bypass the BUS-68005's internal microprocessor. The only part of a DMA input or output command string that is handled as programmed I/O is the first five bytes of each command. The bytes are used for specifying data direction, starting address and byte count for the BUS-68005 DMA controller. Using DMA, it is possible to write and read messages and control data to memory and the BUS-68005 registers which control functions such as: transmitter amplitude, mode, RT address, response time-out, and run/halt control. All parameters unique to individual messages such as data word count, format, response time, inter-message gap time, (BC mode), and block linking information (RT mode) may be written to the first word location (control word) of each message block. Words to be transmitted and received on the 1553 bus are stored in the subsequent contiguous locations in the message block. The BUS-68005 DMA operations are implemented as half burst transfers. That is, following the DMA command header, the specified number of bytes are written to or read from the BUS-68005 64K address space. There is also an embedded DMA timeout mechanism that prevents the instrument from locking-up in the event of any incomplete DMA transfer burst.

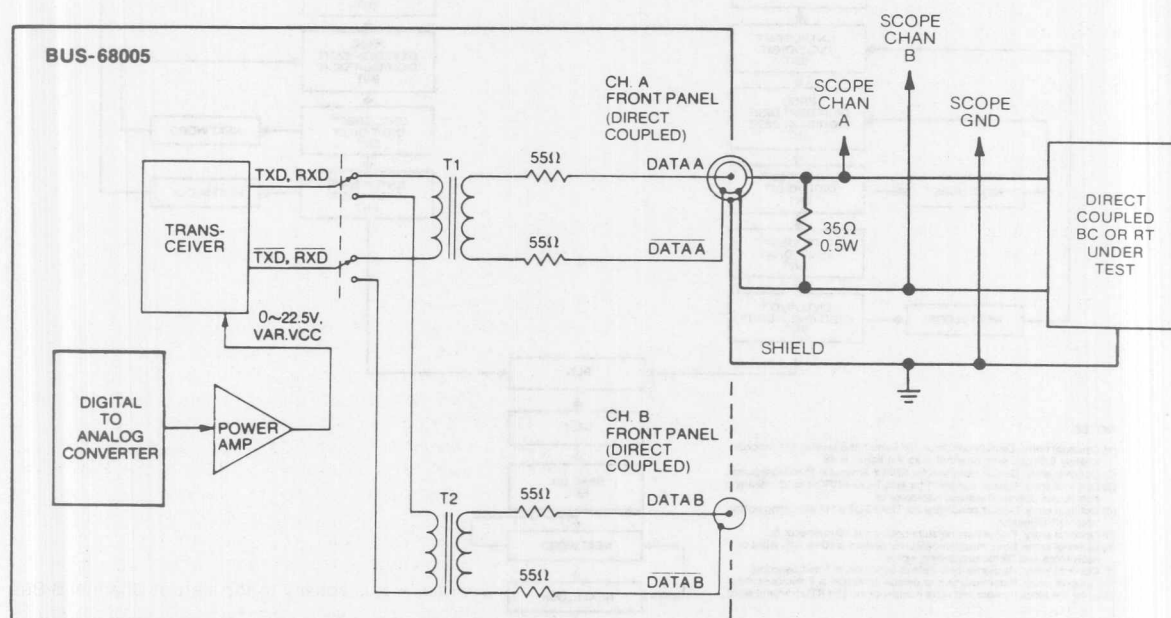
The timing for the IEEE-488 DMA transfer burst is 1.2ms Header time (per input or output burst), plus approximately 8.5 $\mu$ s per byte for input data, or 3.5 $\mu$ s per byte for output data. Assuming a 600KHz GPIB controller, this results in total byte transfer times of 10 $\mu$ s for input data and 5 $\mu$ s for output data.

## BUS SWITCHING TEST

Two 68005's may be used to perform the "Bus Switching" test for dual redundant remote terminals, as required by the SAE-9A Production Test Plan. By means of the simple three-wire interface illustrated in figure 4, it is possible to synchronize the start of bus activity for the two instruments. Under either keyboard or remote I/O control, the delay time interval from the start of Channel A Bus activity to the start of Channel B Bus activity (or vice-versa) may be programmed to be anywhere in the range from 0 to 2040 microseconds, in 1 microsecond steps. By using a simple three-wire interface shown in figure 4 (a) and 4 (c), it is possible to synchronize the start of bus activity for the two instruments. Under either keyboard or remote I/O control, the delay time interval from the start of Channel A Bus activity to the start of Channel B Bus activity (or vice-versa) may be programmed to be anywhere in the range from 0 to 2040 microseconds in 1 microsecond steps. It is also possible to implement the Bus Switching Test by using one BUS-68005 and one BUS-68015 Noise Tester, shown, in figure 4 (b).

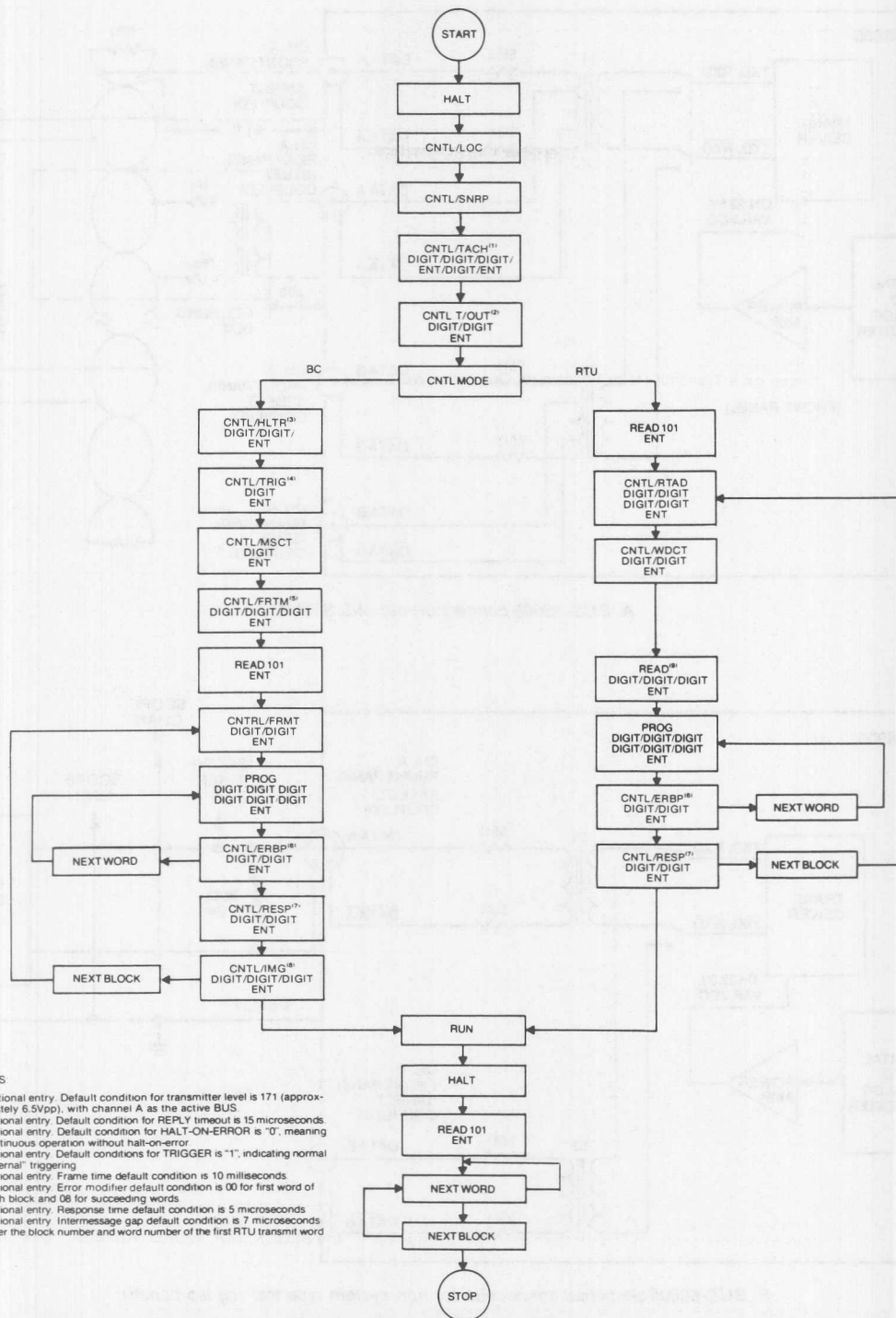


A. BUS-68005 connection per MIL-STD-1553.



B. BUS-68005 simplified connection for non-system type test (eg lab bench).

**FIGURE 2. BUS-68005 INTERCONNECTION DIAGRAM**



**NOTES**

- (1) Optional entry. Default condition for transmitter level is 171 (approximately 6.5Vpp), with channel A as the active BUS.
- (2) Optional entry. Default condition for REPLY timeout is 15 microseconds.
- (3) Optional entry. Default condition for HALT-ON-ERROR is "0", meaning continuous operation without halt-on-error.
- (4) Optional entry. Default conditions for TRIGGER is "1", indicating normal "internal" triggering.
- (5) Optional entry. Frame time default condition is 10 milliseconds.
- (6) Optional entry. Error modifier default condition is 00 for first word of each block and 08 for succeeding words.
- (7) Optional entry. Response time default condition is 5 microseconds.
- (8) Optional entry. Intermessage gap default condition is 7 microseconds.
- (9) Enter the block number and word number of the first RTU transmit word.

**FIGURE 3. MANUAL PROGRAMMING FLOW DIAGRAM**



**TABLE 2. KEYBOARD AND DISPLAY FUNCTIONS**

KEY SEQUENCE	FUNCTION	DISPLAY/INDICATION
CNTL LOC	Sets Local mode of Exerciser control.	LOCAL indicator lights
CNTL MODE	Selects BC or RT with alternating activation of MODE key.	BC or RT indicator lights in coincidence with the MODE key's state.
CNTL SN RP	Selects single or repeat mode of operation with alternating activation of SN RP key.	SINGLE or REPEAT indicator lights in coincidence with the SN RP key's state.
CNTL FRMT DIGIT DIGIT ENT	Information transfer format for a given block is selected with 2 (HEX) digits. See table 3.	The 4-digit (HEX) display will indicate the one or two-digit format.
CNTL RTAD D or E or C 0 or 1 DIGIT DIGIT DIGIT ENT	Used only in RTU mode. The RT address for a given message block is programmed. The 1st digit Enables (E) or Disables (D) the current block or disables all eight message block (C). The 2nd digit specifies whether to trigger on a Transmit (1) or Receive (0) Command Word. The 3rd and 4th digits specify the 2-digit (decimal) RT address (00 to 31). The 5th digit specifies the number of "linked to" memory blocks. This allows the Exerciser to respond by transmitting/receiving from a specified sequence of memory blocks, each successive time that a command is directed to a given RT address.	The 4-digit (HEX) DATA selection of the 16-BIT DATA field will show entered RT address information. The first digit of the ERROR CODE field will indicate the number of the "linked to" memory block.
CNTL RESP DIGIT DIGIT	Simulated RT response time is entered as 2-digits (decimal). The allowable range for response time is from 5 to 32 $\mu$ sec.	The 4-digit (HEX) data section of the 16-BIT DATA will indicate the 1 or 2-digit response time in microseconds.
CNTL IMG DIGIT DIGIT ENT	Used only in the BC mode. The Intermessage Gap time preceding a given message block is entered as 3 (decimal) digits. Allowable range is from 7 to 2047 $\mu$ sec. See Figure 4, Block/Frame Timing Diagram.	The 4-digit (HEX) data section of the 16-BIT DATA field will indicate 2 or 3 (decimal) digit Intermessage Gap time in microseconds.
CNTL WD CT DIGIT DIGIT ENT	The data word count for a given message block is entered as 2 (decimal) digits. For RT mode, this parameter must be programmed. For BC mode, word count defaults to the correct value if unspecified. Allowable range for Word Count is from 0 to 45 words.	The 4 digit (HEX) data section of the 16-BIT DATA field will indicate the 1 or 2-digit data word count.
CNTL ER BP DIGIT DIGIT ENT	The "Error Modifier" information for word gap, message gap, zero-crossing deviation, Manchester and sync field errors are entered as 2 (HEX) digits. Refer to Table 4 for "Error Modifier" Coding.	The Block and Word number are displayed in their normal positions. The 1 or 2-digit (HEX) error modifier code will appear in the 4-digit (HEX) data section of the 16-BIT DATA field.
CNTL FR TM DIGIT DIGIT DIGIT	Used in BC mode only. The Frame Time or overall repetition time for a series of messages to be executed is entered as 3 (decimal) digits. The allowable range for Frame Time is 2 to 500msec. See Figure 4, Block/Frame Timing Diagram.	The 4-digit (HEX) data section of the 16-BIT DATA field will display the entered data.
CNTL PRNT	A user friendly message, conveying all information about the current message block is outputted via the instrument's RS-232 port. It may be displayed on a CRT or a hard copy may be printed if configured with the I/O port.	No change from previous indication.
CNTL MS CT DIGIT ENT	The number of message (blocks) to be processed is specified. The allowable message count is 1 to 8. "Message Count" indicates the number of blocks per frame in the BC MODE, and the total number of messages to be processed for "single" RT mode.	The 4-digit (HEX) data section of the 16-BIT DATA field will display the entered Message Count information.
CLR	Clear function (terminates data or parameter entry). Also used to enable instrument operation in the event of Self-Test failure at power turn-on.	The display reverts back to its previous state.
NEXT WORD	The current WORD NUMBER field (within the current block) is incremented by one. If the current word is the last word in the block, the next word becomes the first word of the current block. NEXT WORD is also used in conjunction with the PROG key.	The next (or first) word in the message block is displayed in the BLOCK, DIR, WORD NUMBER, 16-BIT DATA, and ERROR CODE fields.

**TABLE 2. KEYBOARD AND DISPLAY FUNCTIONS (CONTINUED)**

KEY SEQUENCE	FUNCTION	DISPLAY/INDICATION
NEXT BLOCK	The BLOCK field is incremented to the next highest block or to block 1 if the current block number is 8. The Word Number field then displays the first word of the new current block.	The first word of the new current block is displayed in the BLOCK, DIR, WORD NUMBER, 16-BIT DATA, and ERROR CODE fields.
PROG DIGIT : DIGIT NEXT WORD DIGIT : DIGIT ENT	The data contents and error codes of the current word, or successive words within a message block are programmed. Multiple words are separated by a NEXT WORD key entry. ENT terminates entry of the string of words. If the entry code for a given string is four (HEX) digits or less, the string represents right justified data only, with the Error Code field defaulting to 00. If programmed, the 5th and the 6th (HEX) digits represent the right justified Error Code field for that word.	The block number, DIR, WORD NUMBER, 16-BIT DATA and ERROR CODE fields for each word will be displayed as entered.
READ DIGIT DIGIT DIGIT ENT	The READ command reviews a specific block and word. The block number is specified by the 1st digit entered. The word number within the block specified by the 2nd digit (right justified) or 2nd and 3rd digit entered.	The appropriate word is displayed from the selected Block Number, including DIR bit, WORD NUMBER, 16-BIT DATA and ERROR CODE. The DIR field is decoded as follows:  T: Transmit Word R: Receive Word P: Word Pending Reception -: Unused Word Location
CNTL SELF TEST	Causes the instrument to perform its internal self-test. This test exercises PROM, Message and RT Trigger RAMS, and performs a wraparound test of MIL-STD-1553 encoder/decoder circuitry. Following self-test, the instrument re-initializes to its power turn-on state: Bus Controller mode, Local, Single Frame, and Single Block.	In sequence: (1) All LEDs blank (1 second) (2) All LEDs light (1 second) (3) PASS or FAIL is displayed in the 4-digit (HEX) data section of the 16-BIT DATA field. If FAIL is displayed a 2-digit "Fail Code" is displayed in the ERROR CODE field.
CNTL TA CH DIGIT DIGIT DIGIT ENT ENT	Relative transmitter amplitude is programmable in the range from 0 to 255, corresponding to approximately 0 to 9.75Vpp, direct-coupled across 35 Ohms.	"TA" will be displayed in the "Block/Direction" field. The 4-digit (HEX) data section for the 16-BIT DATA field will indicate the 1, 2, or 3-digit relative transmitter amplitude as entered.
CNTL TA CH ENT A or B ENT	The active BUS channel is selected as either channel A or channel B.	"Ch" will be displayed in the "BLOCK/DIR" field. "-A" or "-B" will be displayed in the "WORD NO." field as programmed.
CNTL HLTER DIGIT DIGIT ENT	The "HALT-ON-ERROR" parameter is entered as a 2-digit decimal number from 0 to 99. An entry of 0 specifies continuous operation without halt-on-error. An entry of 1 to 99 indicates to halt following the occurrence of the specified number of errors. (BC mode only.)	"HE" will be displayed in the "BLOCK/DIR" field. The 4-digit (HEX) data selection of the 16-BIT DATA field will display the entered data.
CNTL T/OUT DIGIT DIGIT ENT	The RT response timeout interval (MIL-STD-1553B definition) is programmable over the range from 5 to 32 microseconds, in 1 microsecond steps.	"TO" will be displayed in the "BLOCK/DIR" field. The 4 digit (HEX) data selection of the 16-BIT DATA field will display the entered data.
CNTL TRIG 1 or E ENT	In order to enable "External" triggering (usually from another BUS-68005) of the Exerciser to synchronize the start of BC transmission, specify "E". To enable normal "internal" triggering, specify "1".	"TG" will be displayed in the "BLOCK/DIR" field. "1" or "E", as programmed, will be displayed in the last digit of the 16-BIT DATA field.

**TABLE 3. MESSAGE FORMAT [CNTL/FRMT] KEY ENTRIES**

FORMAT	MODE	FORMAT	SIMULATION
00 <sup>(1)</sup>	BC RTU	RT to BC or BC to RT RT to BC or BC to RT	BC RTU
01 <sup>(2)</sup>	BC RTU	RT to RT RT to RT	BC RTU(TX)
02 <sup>(2)</sup>	BC RTU	RT to RT RT to RT	BC and RTU(TX) RTU(TX) and RTU(RX)
03 <sup>(2)</sup>	BC RTU	RT to RT RT to RT	BC and RTU(RX) RTU(RX)
04	BC RTU	MODE CODE MODE CODE	BC RTU
08	BC RTU	BROADCAST BROADCAST	BC RTU(RX)
09	BC RTU	BROADCAST and RT to RT BROADCAST and RT to RT	BC RTU(TX)
0A	BC RTU	BROADCAST and RT to RT BROADCAST and RT to RT	BC and RTU(TX) RTU(TX) and RTU(RX)
0B	BC RTU	BROADCAST and RT to RT BROADCAST and RT to RT	BC and RTU(RX) RTU(RX)
0C	BC RTU	BROADCAST and MODE CODE BROADCAST and MODE CODE	BC RTU(RX)
10 <sup>(3)</sup>	BC RTU	T/R FORMAT REVERSAL ERROR T/R FORMAT REVERSAL ERROR	BC RTU
20 <sup>(4)</sup>	BC	SELF TEST	NONE

Notes:

(1) In the BC mode, the T/R bit of the Command Word determines whether the BUS-68005 transmits or receives data. In the RTU mode the T/R bit of the programmed 5 (decimal) digit CNTL/RT AD word determines whether the BUS-68005 transmits or receives data.

(2) In an RT to RT message format, when the BUS-68005 is in the RTU mode, the T/R bit of the programmed 4 (decimal) digit CNTL/RT AD word must be set to logic "0" (Receive).

(3) In the BC mode, the Bus-68005 transmits the Command Word and then acts as if the opposite T/R bit condition were true. In the RTU mode, the BUS-68005 receives the Command Word and then acts as if the opposite T/R bit condition were true.

(4) In the BC mode only, a wraparound self-test will be implemented on message block no. 1. The transmitter is inhibited and the encoder drives the decoder directly. The last data word received is stored in BUS-68005 memory.

**TABLE 4. TRANSMITTED WORD ERROR ENTRIES**

"ERROR" BYTE ["PROG" KEY ENTRY]							"ERROR MODIFIER" BYTE ["ER BP" KEY ENTRY]							INDUCED WORD ERROR CONDITION
40	20	10	08	04	02	01	40	20	10	08	04	02	01	
0	0	0	0	0	0	0	X	X	X	X	X	X	X	Normal Word (No Errors)
0	0	0	0	0	0	1	0	X	0	X	X	X	X	Long Word: 1 extra bit
0	0	0	0	0	0	1	0	X	1	X	X	X	X	Long Word: 2 extra bits
0	0	0	0	0	1	0	0	X	X	X	X	X	X	Short Word: 1 missing bit
0	0	0	0	1	0	0	0	X	X	(MEP-1)*				Manchester encoding error in specified data bit position Parity Error
0	0	0	1	0	0	0	X	X	X	X	X	X	X	Parity Error
0	0	1	0	0	0	0	X	0	0	X	X	X	X	SYNC $\left\{ \begin{array}{l} \overline{11}0000 \text{ (C/S); } 00\overline{1111} \text{ (D)} \\ \overline{1111}00 \text{ (C/S); } 0000\overline{11} \text{ (D)} \end{array} \right.$
0	0	1	0	0	0	0	X	0	1	X	X	X	X	FIELD $\left\{ \begin{array}{l} \overline{1111}00 \text{ (C/S); } 0000\overline{11} \text{ (D)} \\ 0\overline{11}000 \text{ (C/S); } 000\overline{11}00 \text{ (D)} \end{array} \right.$
0	0	1	0	0	0	0	X	1	0	X	X	X	X	ERRORS $\left\{ \begin{array}{l} 0\overline{11}000 \text{ (C/S); } 000\overline{11}00 \text{ (D)} \\ \overline{111}00\overline{1} \text{ (C/S); } \overline{1}00\overline{111} \text{ (D)} \end{array} \right.$
0	1	0	0	0	0	0	X	X	X	X	X	X	X	Manchester encoding error in parity bit position
1	0	0	0	0	0	0	X	X	X	X	X	X	X	Inverted sync type error
0	0	0	0	0	0	1	1	X	X	X	X	X	X	Word gap error: 1 $\mu$ sec gap between 8th and 9th data bits
0	0	0	0	0	1	0	1	X	X	X	X	X	X	Message gap error: 2 $\mu$ sec gap between current word and next word
0	0	0	0	1	0	0	1	0	0	(ZCDEP-1)*				Zero-Crossing $\left\{ \begin{array}{l} 187.5 \text{ nsec early} \\ 125.0 \text{ nsec early} \\ 125.0 \text{ nsec late} \\ 187.5 \text{ nsec late} \end{array} \right.$
0	0	0	0	1	0	0	1	0	1	(ZCDEP-1)*				Deviation Error
0	0	0	0	1	0	0	1	1	0	(ZCDEP-1)*				in first half of
0	0	0	0	1	0	0	1	1	1	(ZCDEP-1)*				specified bit time

Notes: (1) When programming from a remote host computer, the Error Byte is programmed as the 5th and 6th HEX digits for the current word in a "program" (PG) command per table 9.

(2) When programming from a remote host computer, the Error Position Byte is programmed as the two digit HEX parameter in an "error position" (EP) command per table 9.

(3) X indicates don't care.

(4) \*Indicates that the Manchester encoding error or zero-crossing deviation error will occur in the data bit position specified as one greater than the number indicated by the 08, 04, 02, and 01 bits of the Error Modifier Byte.

TABLE 5. DISPLAYED ERROR CODES [RECEIVED WORDS]	
DISPLAY ERROR CODE	ERROR
01	Long Word
02	Short Word
04	Manchester Error
08	Parity Error
10	Message Error
20	Early Response Error
40	Incorrect Sync Type

TABLE 6. FRONT PANEL INDICATOR FUNCTION	
INDICATOR	FUNCTION
LOCAL	Indicates that the Local mode of Exerciser control has been selected.
REMOTE	Indicates that the Remote mode of Exerciser control has been selected.
BC	Indicates that the Bus Controller mode of Exerciser operation has been selected.
RT	Indicates that the Remote Terminal mode of Exerciser operation has been selected.
SINGLE	Indicates that the Single mode of Exerciser operation has been selected.
REPEAT	Indicates that the Repeat mode of Exerciser operation has been selected.
ON-LINE	Indicates that the Exerciser is ready to receive (RT mode) or is transmitting in the Repeat mode (BC mode).
LINE ACTIVE	Indicates that there is activity on the selected 1553 data bus.
BUS FAULT	Indicates an error in the word or message received from the 1553 data bus.
REPLY T/OUT	Indicates that a response timeout fault or "early response" error has occurred.
XMTR T/OUT	Indicates that a 800 $\mu$ s terminal fail-safe timeout fault has occurred.

## IEEE-488 STANDARD

Table 7 lists the subset of IEEE-488-1978 standard supported by the BUS-68005. The serial poll status byte and service request conditions for the BUS-68005 are defined in table 8.

TABLE 7. IEEE-488-1978 INTERFACE FORMAT	
SH1	Full Source Handshake Capability.
AH1	Full Acceptor Handshake Capability.
T6	Basic Talk capabilities with Serial Poll and untalk if my listen address.
SR1	Full Service Request Capability.
RL1	Full Remote Local Capability including Lockout.
DC1	Full Device Clear Capability.
DT1	Full Device Trigger Capability.
CO	No Controller Capability.

TABLE 8. GPIB SERVICE REQUEST INFORMATION	
SERIAL POLL STATUS BYTE	
BIT	BIT INFORMATION
7 (MSB)	Input buffer (Queue) full.
6	RQS (Request for Service).
5	RS-232 error.
4	DMA Timeout.
3	High-speed I/O error.
2	Self-test failure.
1	Error in input command string.
0 (LSB)	1553 message sequence completed.
SERVICE REQUEST CONDITIONS:	
1. Input buffer (queue) full.	
2. Error in input command string.	
3. 1553 message sequence complete.	
4. DMA Timeout.	

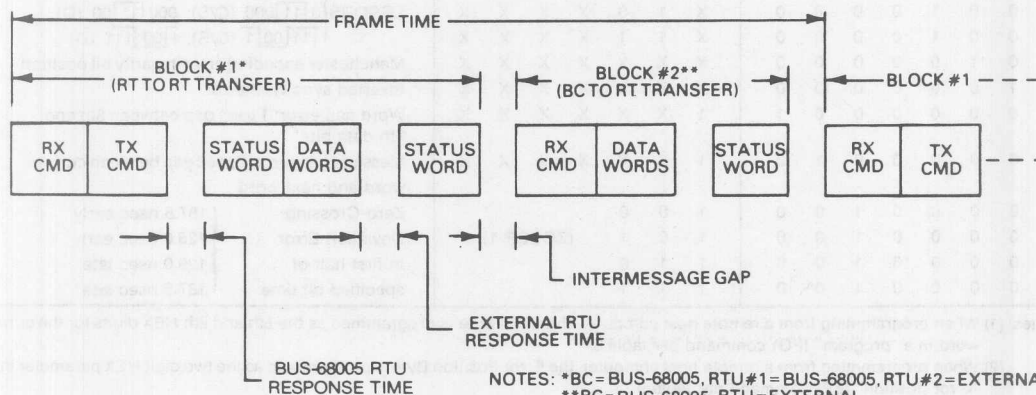
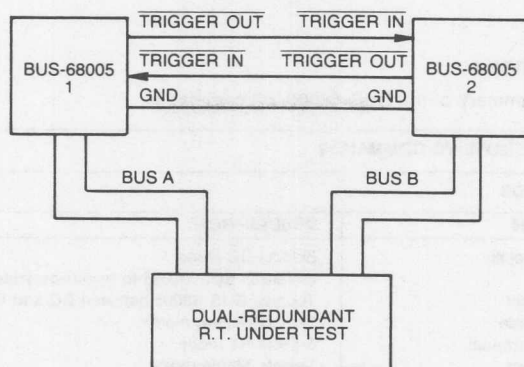
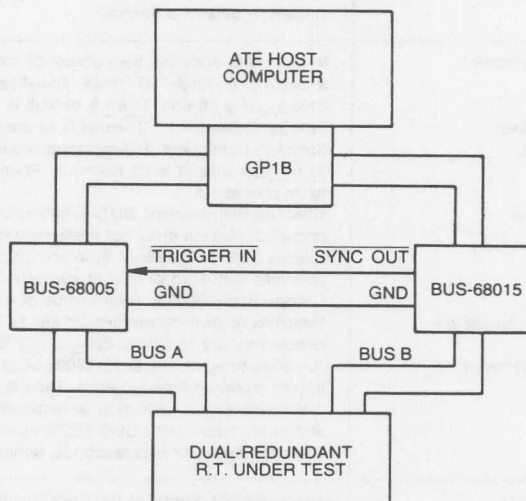


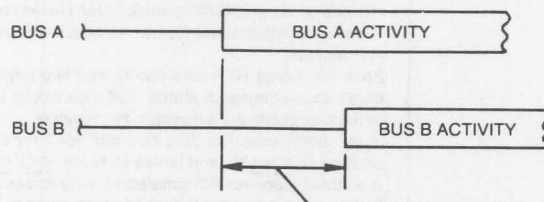
FIGURE 4. TIMING DIAGRAM [BC MODE]



(A) BUS SWITCHING TEST USING TWO BUS-68005s



(B) BUS SWITCHING TEST USING ONE BUS-68005 AND ONE BUS-68015



BUS A TO BUS B DELAY TIME INTERVAL PROGRAMMABLE, IN  $1\mu\text{sec}$  STEPS BY MEANS OF "INTERMESSAGE GAP TIME" PARAMETER. THE RANGE FOR THE DELAY TIME INTERVAL IS 0 TO  $\pm 2040\mu\text{sec}$  USING TWO BUS-68005s. THE DELAY TIME INTERVAL USING ONE BUS-68005 AND ONE BUS-68015 IS 0 TO  $-993, +1047\mu\text{sec}$ .

(C) BUS SWITCHING TEST TIMING

FIGURE 5. BUS SWITCHING TEST FOR DUAL REDUNDANT RTUs



## COMMAND DEFINITIONS

Table 9 provides a summary of the BUS-68005 I/O commands.

TABLE 9. BUS-68005 REMOTE I/O COMMANDS			
LOW SPEED COMMANDS			
	COMMAND	FUNCTION	DESCRIPTION
Set-Up/ Mode Control	BC	Bus Controller	Selects BC Mode.
	IN	Initialize	Initializes BUS-68005 to power-on state.
	MO	Mode Select	Toggles BUS-68005 between BC and RT modes; default is BC.
	RP	Repeat Mode	Selects Repeat mode.
	RT	Remote Terminal	Selects RT mode.
	SN	Single Mode	Selects Single mode.
	SR	Single/Repeat Select	Toggles BUS-68005 between Single and Repeat modes of operation; default is Single.
	TGt:	Trigger Mode Select	Selects Internal (I) or External (E) triggering of BUS-68005 message sequence; default is Internal.
Instrument Parameters	BFn:	Blocks per Frame	In BC mode, specifies the number of messages to be processed per frame sequence. In single RT mode, specifies the number of messages to process before going off-line. $1 \leq n \leq 8$ ; default is 1.
	CHc:	Channel Select	Selects Channel A or Channel B as the active bus channel; default is A.
	FTff:	Frame Time	Specifies frame time (BC message sequence repetition time) in milliseconds. $2 \leq ff \leq 500$ ; default is 10. Minimum Frame Time equals number of messages to be processed.
	HEee:	Halt-on-Error	Specifies halt-on-error. BUS-68005 halts BC operation after ee errors have occurred. Halt-on-error not implemented if ee=0. $00 \leq ee \leq 99$ ; default is 00.
	NB	Next Block	Causes BUS-68005 Block Pointer (1,2...8) to be incremented. Current word becomes first word of next block; default is block 1.
	RDnn:	Read	Causes BUS-68005 to return value of word nn of block b.
	TAaaa:	Transmitter Amplitude	Specifies relative transmitter amplitude from 0 to 10Vpp, approx. direct coupled across 35 Ohms: $000 \leq aaa \leq 225$ . Default is 171; (6.5Vpp, approx.)
	TOtt:	Response Timeout	Specifies time interval BUS-68005 waits for status word response from RT before reporting time out error. Time is per 1553B specification (mid parity of preceding word to mid sync of responding status word). Used in BC mode and in RT mode when BUS-68005 acts as receiving RT in an RT-to-RT transfer. $05 \leq tt \leq 32$ microseconds; default is 15.
Parameters For Individual Message Blocks	EPmm:	Error Position	Used with PG. Specifies the Error Position or Error Modifier two-digit HEX byte for individual message words which specifies word error conditions. $00 \leq mm \leq FF$ (HEX). See table 4.
	FRff:	Format	Specifies format for Current message. $00 \leq ff \leq 20$ (HEX); default is 00. See table 3.
	IMiiii:	Intermessage Gap Time	Specifies intermessage gap time (time preceding start of message in microseconds per 1553 definition) for current block. $7 \leq iiii \leq 2047$ .
	NW	Next Word	Increments Block/Word pointer to next word position; contents of next word are returned.
	PGddddee. ...ddddee:	Program	Specifies 4 digit HEX data (dddd) and two digit HEX error codes (ee) for contiguous command, status, and data words to be transmitted. Entries for individual words are separated by commas.
	RAEdaan; or RAx; or RAn:	RT Address	In RT mode, specifies data direction (d=T for transmit, d=R for receive), address ( $00 \leq a \leq 31$ ) and linked to block ( $0 \leq n \leq 8$ ) for current message block. E enables block for RT simulation; x=D disables block; x=C disables all 8 blocks, n specifies the linked-to block number. Also, n may assume the value d, indicating the linked to block is disabled. Default is all eight blocks disabled.
	RErr:	Response Time	Specifies response time in microseconds for the Current block's simulated RT. For BC mode (RT-to-RT transfer formats) $5 \leq rr \leq 31$ ; for RT mode, $6 \leq rr \leq 31$ . Default is 5.
	WCnn:	Word Count	Specifies data word count for Current message. In BC mode, word count defaults to block's command word value, but may be overridden with WC command. $00 \leq nn \leq 45$ ; default is 32.

**TABLE 9. BUS-68005 REMOTE I/O COMMANDS (CONTINUED)**

LOW SPEED COMMANDS			
	COMMAND	FUNCTION	DESCRIPTION
1553 Processor Run Halt Control	GO	GO	In BC mode, initiates message frame sequence. In RT mode, puts BUS-68005's enabled RTs on-line.
	HA	Halt	In Repeat BC mode, BUS-68005 stops programmed message processing following current frame; in RT mode, BUS-68005 goes off-line following current message.
Data Reporting	SB	Send Block	BUS-68005 returns all words of current message block in reply string.
	SS	Send Status	BUS-68005 returns status of operating modes and parameters in its reply string.
	SW	Send Word	BUS-68005 returns current word of current block.
Display Control and Self-Test	DD	Display Disabled.	Stops update of front panel display or blanks display if DD is last command in command string. Increases I/O throughput speed.
	DE	Display Enabled.	Resumes updating front panel display; default is enabled.
	LT	Lamp Test.	Blanks display for 1.5 seconds, fully lights display for 1.5 seconds, resumes previous display.
	ST	Self Test.	BUS-68005 performs self-test of PROMs, message and trigger RAMs, and front-end wraparound (encoder/decoder) test. Display blanks, lights, and displays test results. Initializes instrument to power-on state.
HIGH SPEED COMMANDS			
	COMMAND	FUNCTION	DESCRIPTION
	&bwnd1 d2...dn	High Speed Input	Transfers n bytes from active I/O port to message RAM. Transfer starts at word w of block b. b, w, n, and d1...dn are binary bytes. Four bytes are used for each control, command, status, or data word in message RAM: (0000 0001) ≤ b ≤ (0000 1000); (0000 0000) ≤ w ≤ (0011 0001); (0000 0001) ≤ n ≤ (1100 1000); (0000 0000) ≤ (d1...dn) ≤ (1111 1111).
	*bwn	High Speed Output	Transfers sequence of continuous bytes from message RAM to active I/O port. Reply string is n binary bytes (d1...dn). Parameters b, w, and n are the same for High Speed Input command.
		High Speed Go High Speed Stop	BUS-68005 immediately processes programmed message sequence. BUS-68005 immediately stops programmed message sequence.
DMA IEEE-488 COMMANDS			
	COMMAND	FUNCTION	DESCRIPTION
	>a1 a0 c1 c0 d1 d2...dn	DMA Input	Transfers sequence of contiguous data bytes, via DMA, from IEEE-488 interface to BUS-68005 memory address locations: a1, a0, c1, c0, and d1...dn are binary bytes; a1 and a0 define the DMA starting address; c1 and c0 specify the number of bytes to be transferred; d1...dn are data.
	< a1 a0 c1 c0	DMA Output	Transfers sequence of contiguous data bytes, via DMA, from BUS-68005 memory address locations to IEEE-488 interface. Parameters a1, a0, c1, c0, and d1...dn are same as DMA input. Reply string is n binary bytes: d1 d2...dn. Followed by a line feed character, <LF>, with EOI asserted.

TABLE 10. J2 PIN FUNCTIONS [PARALLEL I/O]		
PIN	FUNCTION	DESCRIPTION
1	T7	MSB of 8 bit parallel tri-state I/O bus.
2	T6	Part of 8 bit parallel tri-state I/O bus.
3	T5	Part of 8 bit parallel tri-state I/O bus.
4	T4	Part of 8 bit parallel tri-state I/O bus.
5	T3	Part of 8 bit parallel tri-state I/O bus.
6	T2	Part of 8 bit parallel tri-state I/O bus.
7	T1	Part of 8 bit parallel tri-state I/O bus.
8	T0	LSB of 8 bit parallel tri-state I/O bus.
9	$\overline{\text{READ}}$	A LOW on this input causes a read data sequence.
10	$\overline{\text{WRITE}}$	A LOW on this input causes a write data sequence.
11	$\overline{\text{TACK}}$	A LOW on this output indicates composite transfer acknowledge.
12	$\overline{\text{SERV REQ}}$	A LOW on this output indicates a service request.
13	GND	Digital ground.
14	$\overline{\text{RACK}}$	A LOW on this output indicates data output transfer acknowledge.
15	$\overline{\text{WACK}}$	A LOW on this output indicates data input transfer acknowledge.
16	CHASS GND	Chassis ground.
17 THRU 25	NC	No connection.

TABLE 11. J3 PIN FUNCTIONS [RS-232]		
PIN	FUNCTION	DESCRIPTION
1	PROT GND	Chassis ground.
2	TXD	Transmit Data output.
3	RXD	Receive Data input.
4	RTS	Request to Send output.
5	CTS	Clear to Send input.
6	NC	No connection
7	SIG GND	Signal ground.
8	DCD	Data Carrier Detect input.
9 THRU 25	NC	No connection.

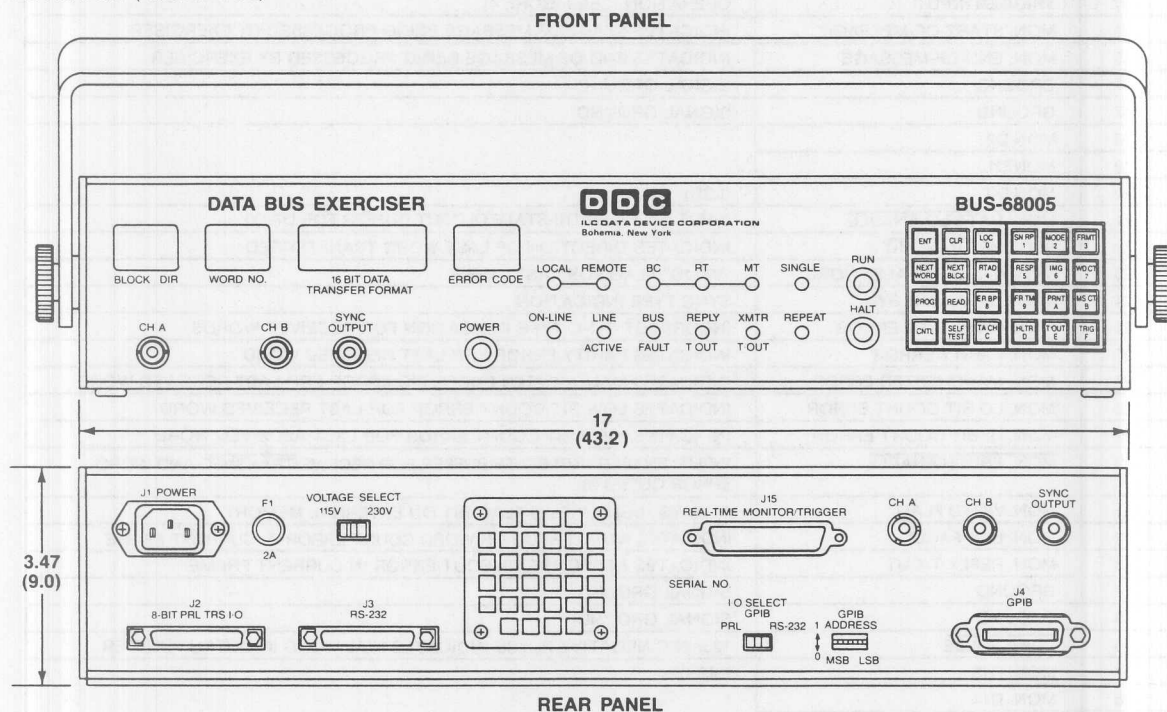
TABLE 12. J4 PIN FUNCTIONS [IEEE-488]		
PIN	FUNCTION	DESCRIPTION
1	D101	LSB of 8 bit tri-state GPIB bus.
2	D102	Part of 8 bit tri-state GPIB bus.
3	D103	Part of 8 bit tri-state GPIB bus.
4	D104	Part of 8 bit tri-state GPIB bus.
5	$\overline{\text{EOI}}$	End or Identify input/output.
6	$\overline{\text{DAV}}$	Data Available input/output.
7	RFD	Ready for Data input/output.
8	DAC	Data Accepted input/output.
9	$\overline{\text{IFC}}$	Interface Clear input.
10	$\overline{\text{SRQ}}$	Service Request output.
11	$\overline{\text{ATN}}$	Attention input.
12	CHAS GND	Chassis ground.
13	D105	Part of 8 bit tri-state GPIB bus.
14	D106	Part of 8 bit tri-state GPIB bus.
15	D107	Part of 8 bit tri-state GPIB bus.
16	D108	MSB of 8 bit tri-state GPIB bus.
17	$\overline{\text{REN}}$	Remote Enable input.
18 THRU 24	GND	Digital ground.

**TABLE 13. J15 PIN FUNCTIONS [REAL-TIME MONITOR/TRIGGER I/O]**

PIN	FUNCTION	DESCRIPTION
1	MON. XMTR T/OUT	INDICATES "TRANSMITTER" TIMEOUT (800 $\mu$ SEC) ERROR IN CURRENT FRAME
2	MON. FAULT ENABLE	INPUT: ENABLES TRI-STATE BUFFER FOR WORD FLAG, BUS FAULT, ETC...
3	RT TRIGGER WORD	INDICATES LAST WORD RT "TRIGGER" WORD
4	BLOCK ADDRESS 2	(MSB)
5	BLOCK ADDRESS 1	(INDICATES CURRENT EXERCISER MESSAGE BLOCK -1)
6	BLOCK ADDRESS 0	(LSB)
7	MON. BLOCK ADDRESS ENABLE	INPUT: ENABLES TRI-STATE BUFFER FOR RT TRIGGER WORD AND BLOCK ADDRESS
8	MON. FRAME ENABLE	INDICATES EXERCISER PROCESSING CURRENT MESSAGE FRAME
9	MONITOR BUS CYCLE ACTIVE	INDICATES EXERCISER PROCESSING CURRENT MESSAGE
10	MONITOR LINE ACTIVE	INDICATES ACTIVITY ON -1553 BUS
11	MONITOR ENCODER CLOCK	RISE EDGE SHIFTS MANCHESTER DATA IN ENCODER
12	TRIGGER OUTPUT	USED TO SYNCHRONIZE TWO BUS-68005S FOR DUAL-REDUNDANT
13	TRIGGER INPUT	OPERATION (SEE FIGURE 4)
14	MON. START-OF-MESSAGE	INDICATES START OF MESSAGE BEING PROCESSED BY EXERCISER
15	MON. END-OF-MESSAGE	INDICATES END OF MESSAGE BEING PROCESSED BY EXERCISER
16	GROUND	SIGNAL GROUND
17	GROUND	SIGNAL GROUND
18	MON.D2	(LSB)
19	MON.D1	
20	MON.D0	
21	MON. DATA LO ENABLE	INPUT: ENABLES TRI-STATE OUTPUT BUFFER FOR D7-D0
22	RECEIVE/TRANSMIT	INDICATES DIRECTION OF LAST WORD TRANSFERRED
23	MON. VALID /INVALID WORD	"VALID" FLAG FOR LAST WORD
24	MON. DATA/CMD SYNC	SYNC TYPE INDICATION
25	MON. SYNC TYPE ERROR	INCORRECT SYNC TYPE INDICATION FOR RECEIVED WORDS
26	MON. PARITY ERROR	INDICATES PARITY ERROR FOR LAST RECEIVED WORD
27	MON. MANCHESTER ERROR	INDICATES MANCHESTER ENCODING ERROR FOR LAST RECEIVED WORD
28	MON. LO BIT COUNT ERROR	INDICATES LOW BIT COUNT ERROR FOR LAST RECEIVED WORD
29	MON. HI BIT COUNT ERROR	INDICATES HIGH BIT COUNT ERROR FOR LAST RECEIVED WORD
30	MON. ERROR ENABLE	INPUT: ENABLES TRI-STATE BUFFER FOR RECEIVE/TRANSMIT, AND WORD ERROR OUTPUTS.
31	MON. WORD FLAG	ALWAYS HIGH: USE AS FLAG BIT ON EXTERNAL MEMORY
32	MON. BUS FAULT	INDICATES WORD ERROR OR WORD COUNT ERROR IN CURRENT FRAME
33	MON. REPLY T/OUT	INDICATES RESPONSE TIMEOUT ERROR IN CURRENT FRAME
34	GROUND	SIGNAL GROUND
35	GROUND	SIGNAL GROUND
36	LOAD PULSE	125nSEC NEGATIVE PULSE INDICATES NEW WORD IN OUTPUT BUFFER
37	MON. D15	(MSB)
38	MON. D14	UPPER 8 BITS OF LAST WORD ON -1553 BUS
39	MON. D13	
40	MON. D12	
41	MON. D11	
42	MON. D10	
43	MON. D9	
44	MON. D8	
45	MON. DATA HI ENABLE	INPUT: ENABLES TRI-STATE OUTPUT BUFFER FOR D15-D8
46	MON.D7	LOWER 8 BITS OF LAST WORD ON -1553 BUS
47	MON.D6	
48	MON.D5	
49	MON.D4	
50	MON.D3	

TABLE 14. MANUAL SWITCH/CONTROL FUNCTIONS		
SWITCH	FUNCTION	REMARKS
RUN	Starts the 1553 data bus message transfer cycle.	The ON-LINE indicator lights up and the display reads BUSY.
HALT	Stops the 1553 data bus message transfer cycle.	The ON-LINE indicator shuts off and the display reads HALT.
I/O SELECT	Selects I/O interface as either Parallel, IEEE-488 or RS-232.	Rear panel switch.
GPIB ADDRESS	Selects the Exerciser's GPIB (IEEE-488) address.	Address has 5 bits. Rear panel switch.
POWER	Turns on the internal power supply.	An initialization and self-test sequence is performed immediately after power turn-on.
VOLTAGE SELECT	Selects 115V or 230VAC line voltage.	Rear panel switch.

DIMENSIONS IN INCHES (CENTIMETERS)  
17 x 14.5 x 3.47 (43.2 x 37 x 9.0)



**FIGURE 6. MECHANICAL OUTLINE**

## ORDERING INFORMATION

BUS-68005

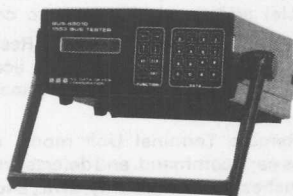
Mating Connector for J15 Amphenol 17-10500-1-390 included.

1553 Mating Connector Trompeter PL75-47 (2 included).

Also included are 2 rack adapters and hardware for full-rack mounting.



## MIL-STD-1553 DATA BUS TESTER



### DESCRIPTION

The BUS-68010 is a low cost bench top portable instrument for testing and troubleshooting MIL-STD-1553 systems. Its price/performance makes it a leader for Bus Controller, Remote Terminal or Bus Monitor simulation applications.

Its simple and flexible operation is controlled via a 24 pad keyboard, with the aid of a 16 character alphanumeric

display. Packaged in a 3.5 x 8.5 x 9.3 inch enclosure, it features error generation and error detection, single or repeat messages, and variable inter-message gap time. BC to RT, RT to BC, RT to RT message formats are simulated by the BUS-68010.

The Data Bus Tester's versatility and small physical size make it an ideal choice for laboratory and field testing applications.

### FEATURES

- **LOW COST**
- **SMALL SIZE: 3.5" x 8.5" x 9.3"**
- **FLEXIBLE OPERATION:**  
BUS CONTROLLER  
REMOTE TERMINAL  
BUS MONITOR
- **PROGRAMMABLE:**  
24 PAD KEYBOARD
- **ERROR GENERATION**
- **ERROR DETECTION**
- **16 CHARACTER**  
ALPHANUMERIC DISPLAY

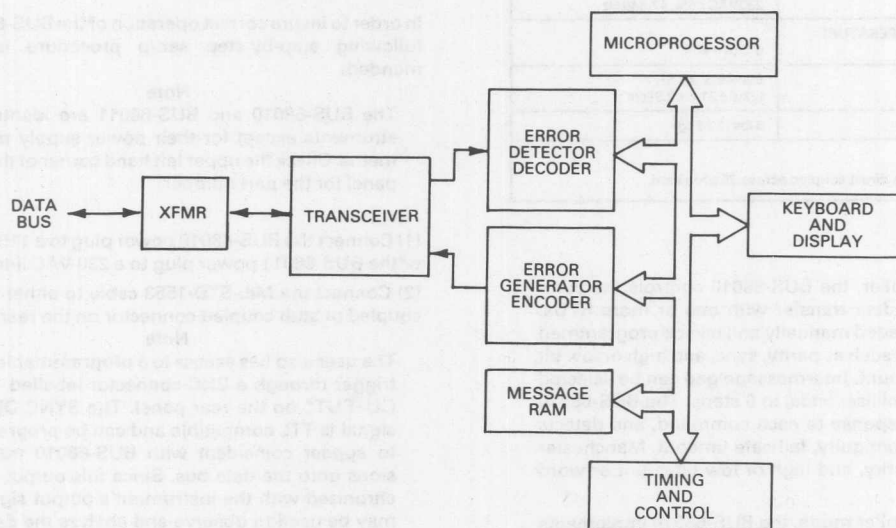


FIGURE 1. BUS-68010 BLOCK DIAGRAM

SPECIFICATIONS	
PARAMETER	VALUE
<b>DATA BUS INTERFACE</b>	
Coupling	Direct or stub
Transmitter	
Output Voltage <sup>(1)</sup>	6V <sub>p-p</sub> min; 9V <sub>p-p</sub> max
Rise/Fall Time	130 nsec typ
Output Noise	10mV <sub>p-p</sub> max (differential)
Receiver	
Input Voltage	40V <sub>p-p</sub> max (differential)
Input Impedance	4K $\Omega$ min (differential)
Threshold Level	1V <sub>p-p</sub> typ (direct coupled)
CMRR	40dB min
<b>MESSAGE CHARACTERISTICS</b>	
Formats	RT to BC, BC to RT, RT (ext) to RT (ext), RT (int) to RT (ext)
Repetition	Single, Double or Continuous
Words Per Message	Programmable 1 to 40
Intermessage Gap	Programmable 5 to 1000 msec
RTU Response Time	7.5 $\mu$ sec
Address (Trigger)	Programmable 0 to 31
Sync Output	Drives 10 LS TTL loads
<b>ERRORS DETECTED</b>	
Word Errors	Manchester Error, Parity Error, Word Length and Sync Errors
Incorrect Sync	
Invalid Word	
Message Errors	
Word Count	
T/R Bit Mismatch	
<b>ERRORS GENERATED</b>	
Word Errors	
Incorrect Sync	
Parity Error	
Short Word	
Long Word	
Message Errors	
Word Count	
<b>AC POWER INPUT</b>	
BUS-68010	115VAC $\pm$ 10%, 60-440 Hz
BUS-68011	230VAC $\pm$ 5%, 47-440 Hz
<b>OPERATING TEMPERATURE RANGE</b>	
	0°C to +70°C
<b>DIMENSIONS</b>	
	9.3" x 8.5" x 3.5" (23.6 x 21.6 x 8.9) cm
<b>WEIGHT</b>	
	5 lbs (2.27 kg)
Notes: (1) Output voltage direct coupled across 35 ohm load.	

## GENERAL

As a Bus Controller, the BUS-68010 controls the command/response data transfer with one or more RTUs. Messages are loaded manually and can be programmed to contain errors such as parity, sync, and high or low bit count or word count. Intermessage gap can be selected from 5 to 1000 milliseconds, in 8 steps. The BUS-68010 evaluates the response to each command, and detects errors such as contiguity, fail-safe timeout, Manchester coding, sync, parity, and high or low bit count or word count.

In the Bus Controller mode, the BUS-68010 implements BC to RT, RT to BC, and RT to RT message transfer formats. Each format may include broadcast or mode code commands. Furthermore, it can be configured to simulate both the BC and one of the RTUs in an RT to RT transfer. Commands and responses are stored in the BUS-68010 internal RAM, and may be viewed word by word

by means of the 16 character front panel alphanumeric displays.

As a Remote Terminal Unit, the BUS-68010 receives, validates and stores data bus commands containing its (selectable) address. It responds to commands with status and data, as appropriate. Response time is 7.5  $\mu$ sec. These messages may be accessed via the keyboard for viewing on the front panel alphanumeric display.

In the Remote Terminal Unit mode, the BUS-68010 evaluates each command, and detects errors such as format, Manchester coding, parity, sync, and high or low bit count or word count.

In the Monitor mode, the BUS-68010 receives, validates and stores data bus messages containing its programmed address (trigger). In accordance with MIL-STD-1553, it does not respond with a status word, nor does it transmit data. If programmed for single message, it will stop after one message and display any errors that have been detected. If continuous message has been selected, the BUS-68010 can be programmed to halt on error.

The BUS-68010 is packaged in a 3.5" x 8.5" x 9.3" enclosure with a handle that can be used as a tilt-stand. It operates from 115 VAC, 60-440Hz. The optional BUS-68011 operates from 230 VAC, 47-440Hz. With its flexible manual programmability and its error generation and detection, the BUS-68010 is ideal for simulation of Bus Controllers or Remote Terminal Units for bench, field or factory test applications.

## SETUP PROCEDURE

In order to insure correct operation of the BUS-68010, the following step-by-step setup procedure is recommended:

### Note

The BUS-68010 and BUS-68011 are identical instruments except for their power supply requirements. Check the upper left hand corner of the front panel for the part number.

- (1) Connect the BUS-68010 power plug to a 115 VAC line, or the BUS-68011 power plug to a 230 VAC line.
- (2) Connect the MIL-STD-1553 cable to either the direct coupled or stub coupled connector on the rear panel.

### Note

The user also has access to a programmable scope trigger through a BNC connector labelled "SYNC OUTPUT" on the rear panel. The SYNC OUTPUT signal is TTL compatible and can be programmed to appear coincident with BUS-68010 transmissions onto the data bus. Since this output is synchronized with the instrument's output signals, it may be used to observe and analyze the data bus activity.

- (3) Actuate the push-button power switch on the rear panel. The instrument will then spend the next 15 seconds identifying itself to the user, displaying the following information:

DDC BUS-68010/11  
1553 BUS TESTER  
ILC/DDC PRODUCT  
SELF TEST PASSED  
READY

By displaying "READY", the unit has indicated successful completion of an internal self check and the user may begin the desired functional setup. If the device encounters a problem during the self test, it will display "FAILURE" followed by a single digit message. The meaning of the message is as follows:

MESSAGE	FAILURE
FAILURE - 1	ROM Test
FAILURE - 2	1553 Test
FAILURE - 3	Multiple Tests
FAILURE - 4	Display Test

When "READY" is displayed, only the SEL or GO keys can create an action response condition. The instrument is now capable of performing as a Bus Controller, Remote Terminal or Monitor. Forty data words may be entered into the RAM locations where they may be observed or edited with the display cursor and keyboard. During data editing, the up (▲) and down (▼) arrows are used to scroll through the list of words; the left (◀) and right (▶) arrows are used to move through the different digits. Once the instrument is fully programmed following data entry and editing, pressing the GO key begins transmission.

## MANUAL PROGRAMMING

After power-on self test, with the display indicating "READY", the instrument's default conditions are as follows:

DEFAULT STATE	RELATED KEYS
BUS CONTROLLER	SEL FCTN
BRO OFF, MC ON	SEL BCMC
EXPANDED FIELD	SEL CMDW
01 T 01R01 00 00	SEL DATA
BC to RT/RT to BC	SEL FRMT
IMG: 5ms	SEL # (t)
MESSAGE CORRECT	SEL WERR
TR 01 X XX XX	SEL TRIG
SINGLE MESSAGE	SEL S/C
ANGLE #3	SEL DSPL

The BUS-68010/11 now may be programmed by the user for any specific function using the front panel keyboard and liquid crystal display. Keys on the panel are grouped within two bracketed areas: FUNCTION and DATA. The FUNCTION keys are used to select a specific menu and, with the GO key, to run the chosen instrument function. The DATA keys permit entry, analysis and modification of data related to the specific function selected.

The keys are tactile-type (pressure sensitive), requiring only a light touch to activate. Note that the SEL key (within the FUNCTION brackets) is blue, matching the color of the non-numeric legends imprinted on 10 of the 16 DATA keys.

The operating sequence requires that the SEL key be pressed first, then one of the blue-legend keys. This pro-

cess is repeated until the user achieves the desired configuration for the selected function.

Information is presented to the user on a 16-character alphanumeric liquid crystal display. A cursor on the display permits the user to edit data when the DATA or TRIG keys have been selected. The cursor is a horizontal bar appearing below the alphanumeric character to be modified. Its position is controlled by left (◀) and right (▶) arrow keys at the top of the FUNCTION bracket. If the cursor cannot be positioned under a character, it means that no modification to that character is necessary.

The following are the keyboard sequences for entering the four possible types of programmable words:

Command Word: WW D AATSS CC EE  
Data Word: WW D S XXXX EE  
Status Word: ST AA B FF DD EE  
Trigger Word: TR AATSS GG

where:

WW = word number (in decimal)

D = direction of transfer

T = instrument *will* transmit this word

P = a word *will* be received in this slot

R = a word *has* been received in this slot

AA = RT address (In HEX)

T = T/R Bit (R = 0, T = 1)

SS = RT sub address or mode code field (In HEX)

CC = Word count or mode code (In HEX)

EE = Sync output or induced error on transmitted words, detected error on received words

S = Sync type (C = command, D = data)

XXXX = Data in four-digit HEX

ST = Status

B = Message error bit (1 = True)

FF = Instrumentation bit, service request bit, plus three reserve bits (in HEX)

DD = Broadcast command bit, busy bit, subsystem flag bit, dynamic bus control bit, and terminal flag bit (in HEX)

TR = Trigger

GG = XX (don't care) if T/R = R. Word count (in HEX) if T/R = T.

A two digit code representing a sync output, an induced error on transmitted words, or a detected error on received words will be displayed at the end of a command word. These programming possibilities are summarized in Table 1.

**TABLE 1 ERROR CODES**

CODE	ERROR	GENERATED	DETECTED
00	No error	—	—
01	Word sync	Yes	Yes
02	Word 1 bit short	Yes	(Note 1)
04	Word 4 bits long	Yes	(Note 1)
08	Parity	Yes	(Note 1)
10	Invalid word	(Note 2)	Yes
20	Missing word (Note 3)	No	Yes
40	Sync output	Yes	No

Notes: (1) Included in Error Code 10  
(2) Error Codes 01, 02, 04 and 08 must be specified.  
(3) Missing word error is displayed when an RT response timeout (no response) has occurred.

KEYBOARD AND DISPLAY FUNCTIONS		
KEY SEQUENCE	FUNCTION	DISPLAY
SEL FCTN ◀ or ▶ ENT	Selects Bus Controller, Remote Terminal or Monitor Mode. The arrows scroll to the next choice.	The current mode will be displayed.
SEL FRMT ◀ or ▶ ENT	For Bus Controller mode only. Selects Normal, RT (EXT) to RT (INT), or RT (INT) to RT (EXT) message format.	The current message format will be displayed.
SEL S/C ◀ or ▶ ENT	Selects single, double or continuous message. The arrows scroll to the next choice.	The current message repetition will be displayed.
SEL TRIG DIGIT DIGIT ENT	For Remote Terminal mode. The RT address is entered with 2 (HEX) digits. For Monitor mode the trigger address is entered.	The entered address is displayed
SEL DATA ◀ or ▶ DIGIT DIGIT ENT	Data word and word errors are entered with 6 (hex) digits. Word errors include incorrect sync, parity error, long word and short word. The arrows scroll to the next word in memory. Command words are entered with 4 (HEX) digits or, when in expanded field format, 9 (HEX) digits.	The entered data and word error are displayed.
SEL WERR ◀ or ▶ ENT	Selects word count error 2 words short, or 1 word short, or correct, or 1 word long, or 2 words long. The arrow scrolls to the next choice.	The current word count error is displayed.
SEL BCMC ◀ or ▶ ENT	Selects Broadcast/Mode Code options. Either one may be ON or OFF. The arrows scroll to the next choice.	The current broadcast and mode code option is displayed.
SEL # (t) ◀ or ▶ ENT	Selects the intermessage gap time between 5 msec and 1000 msec. The arrows scroll to the next choice.	The current intermessage gap time is displayed.
GO	Starts operation. For continuous message operation, press CLR key to STOP.	
CLR	Stops operation. Clears last entry.	
SEL CMDW ◀ or ▶ ENT	Selects Command Word display format of 4-digit (HEX) or expanded field (HEX). The arrows scroll to the next choice.	The current Command Word display format choice is displayed.
SEL DSPL ◀ or ▶ ENT	Selects LCD viewing angle. Arrows scroll to the next choice.	The optimum display viewing angle varies through 4 choices.

## FRONT PANEL CONTROLS/INDICATORS

24 PAD KEYBOARD

16 CHARACTER LCD DISPLAY

## REAR PANEL SWITCHES/CONNECTORS

POWER ON/OFF SWITCH

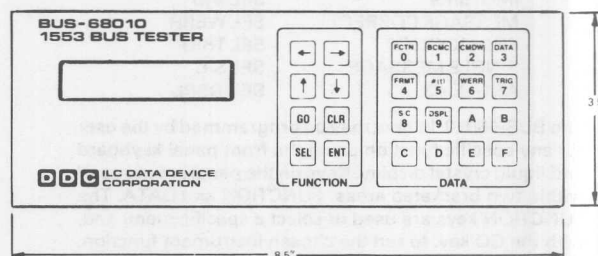
1553 DIRECT COUPLED CONNECTOR

1553 STUB COUPLED CONNECTOR

SYNC OUTPUT

## MECHANICAL OUTLINE

3.5" x 8.5" x 9.3"  
(8.9 x 21.6 x 23.6 cm)



## ORDERING INFORMATION

BUS-68010

Options:

0 = 115 VAC Power

1 = 230 VAC Power

## MIL-STD-1553 NOISE TESTER



### DESCRIPTION

The BUS-68015 Noise Tester is a low cost bench top portable instrument used for performing the noise rejection tests specified in MIL-STD-1553.

It is fully self-contained, thereby eliminating the need for special test equipment. The BUS-68015 has the noise source, amplifiers, filters, and tester logic built in. Signal and noise levels are user controlled and may be varied independently. The BUS-68015 includes a self-test feature initialized dur-

ing power-on.

Packaged in a compact 8.25 x 3.5 x 14.5 inch enclosure, manual operation is easily controlled via a 16 pad keyboard, with the aid of a 16 character alphanumeric display. For ATE applications, the BUS-68015 is controlled by means of its IEEE-488 interface.

The BUS-68015 Noise Tester's versatility and small physical size make it an ideal choice for laboratory and field testing applications.

### FEATURES:

- IMPLEMENTS MIL-STD-1553 NOISE REJECTION TESTS
- FULLY SELF-CONTAINED:  
NOISE SOURCE  
FILTER AMPLIFIER  
BUS CONTROLLER  
WORD AND ERROR COUNTERS
- PROGRAMMABLE:  
16 PAD KEYBOARD  
IEEE-488 I/O
- INDEPENDENTLY VARIABLE  
SIGNAL AND NOISE LEVELS
- LOW COST
- COMPACT SIZE:  
8.25" x 3.5" x 14.5"
- 16 CHARACTER  
ALPHANUMERIC DISPLAY
- AUTOMATIC SELF-TEST

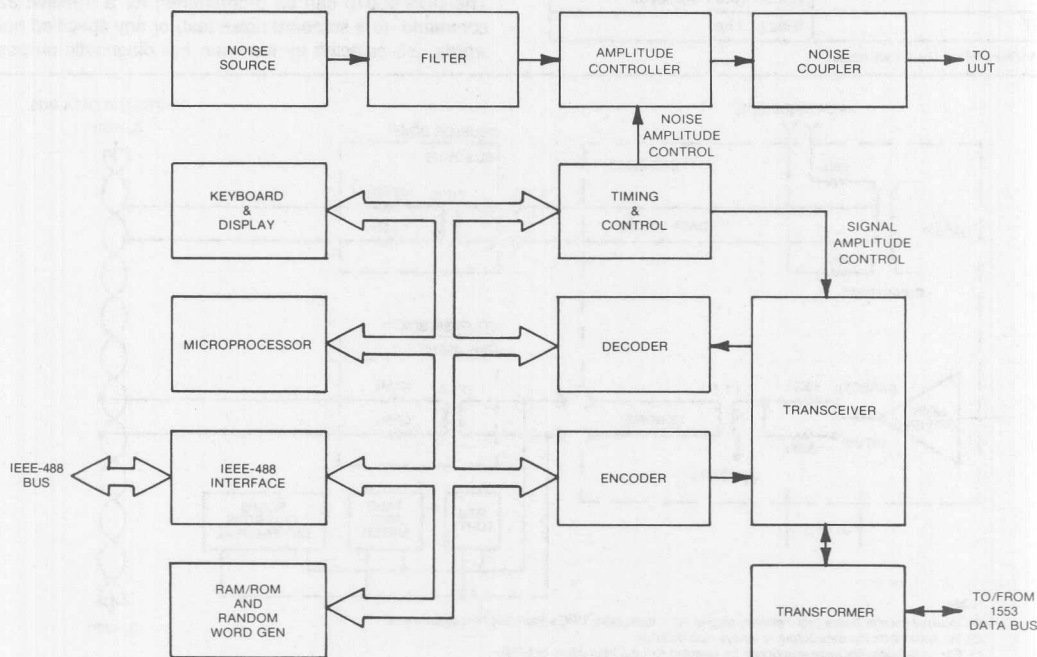


FIGURE 1. BUS-68015 BLOCK DIAGRAM



TABLE 1. BUS-68015 SPECIFICATIONS	
PARAMETER	VALUE
<b>DATA BUS INTERFACE</b>	
Noise Output <sup>(1)</sup>	
Voltage Level (adjustable)	50mVrms min, to 350mVrms max
Impedance	
Transformer coupled	700 $\Omega$ , approx
Direct coupled	350 $\Omega$ , approx
Stub Input Signal (receive)	Vin = 0.86Vpp min to 14.0Vpp max
Direct Input Signal (receive)	Vin = 1.2Vpp min to 20.0Vpp max
Stub Output Signal (adjustable, transmit)	Vout = 18Vpp, min (70 $\Omega$ $\pm$ 2% resistor termination)
Direct Output Signal (adjustable, transmit)	Vout = 6Vpp, min (35 $\Omega$ $\pm$ 2% resistor termination)
SYNC Output	For scope triggering purposes TTL level pulse, 10 LSTTL driving load capability.
<b>AC INPUT POWER</b>	
Voltage	115V/230V $\pm$ 10% (switch selectable)
Power	20VA max
Frequency	47-63 Hz
<b>OPERATING TEMPERATURE RANGE</b>	
	0°C to +70°C
<b>DIMENSIONS</b>	
	8.25 x 3.5 x 14.5 inches (20.64 x 8.0 x 36.83) cm
<b>WEIGHT</b>	
	9 lbs (4.1 kg)

Notes: <sup>(1)</sup>Additive white Gaussian noise.

## GENERAL

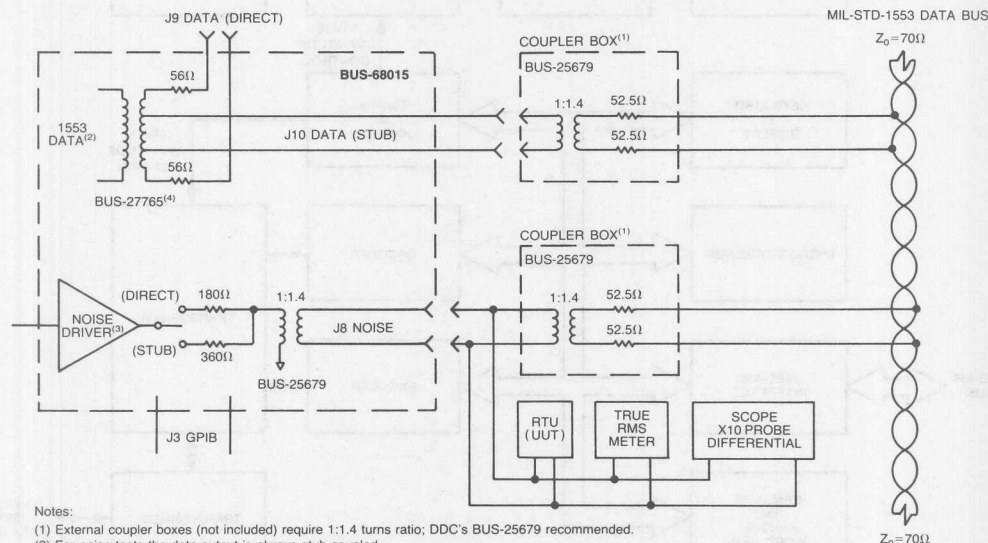
The BUS-68015 Noise Tester is used to test and troubleshoot the noise rejection characteristics of MIL-STD-1553 systems and subsystems. The noise source, amplifiers, filters, and tester logic are built into the BUS-68015, eliminating the need for special test equipment. The front panel contains a 16 pad keyboard and a 16 character alphanumeric display, which are used for manual programming. For automatic test (ATE) applications, the IEEE-488 interface may be used. A beeper sounds when any front panel key has been depressed.

Figure 2 illustrates a typical BUS-68015 based noise test. The BUS-68015 transmits a specified number of random data words over the 1553 Data Bus and reads the status word from the RTU under test. If the RTU does not send a status word, BUS-68015 records an error. An error will also be recorded if the status word has the wrong RT address or has any bits set other than BUSY or SERVICE REQUEST. The test stops when the RTU passes or fails the criteria of MIL-STD-1553, shown in table 2. The total number of words transmitted and the total number of errors detected may be displayed during the test.

The BUS-68015 also has the capability to characterize the rejection of MIL-STD-1553 systems and subsystems by performing the noise test continuously and not stopping until the STOP key is pressed. This allows accumulating a large number of words and errors to determine the true long-term error rate.

A set-up mode permits output to the 1553 of noise only or signal only to allow adjusting of these levels. The set-up mode is also used to set the RT address and the number of words transmitted.

The BUS-68015 can be programmed for a "receive 32 words command" (the standard noise test) or any specified number of words,  $\geq 3$  selected by the user. For diagnostic purposes, the



- Notes:
- (1) External coupler boxes (not included) require 1:1.4 turns ratio; DDC's BUS-25679 recommended.
  - (2) For noise tests the data output is always stub coupled.
  - (3) For noise tests, the noise output can be selected (via the front panel or GPIB) for either stub or direct coupling.
  - (4) Turns ratio 1:1 for direct coupling and 1.4:1 for stub.

FIGURE 2. TYPICAL BUS-68015 BASED NOISE TEST

**TABLE 2. CRITERIA FOR ACCEPTANCE OR REJECTION OF A TERMINAL FOR THE NOISE REJECTION TEST.**

No. of errors	Total words received by terminal (in multiples of 10 <sup>3</sup> )	
	Reject (equal or less)	Accept (equal or more)
0	NA	4.40
1	NA	5.21
2	NA	6.02
3	NA	6.83
4	NA	7.64
5	NA	8.45
6	0.45	9.27
7	1.26	10.08
8	2.07	10.89
9	2.88	11.70
10	3.69	12.51
11	4.50	13.32
12	5.31	14.13
13	6.12	14.94
14	6.93	15.75
15	7.74	16.56
16	8.55	17.37
17	9.37	18.19
18	10.18	19.00
19	10.99	19.81
20	11.80	20.62
21	12.61	21.43
22	13.42	22.24
23	14.23	23.05
24	15.04	23.86
25	15.85	24.67
26	16.66	25.48
27	17.47	26.29
28	18.29	27.11
29	19.10	27.92
30	19.90	28.73
31	20.72	29.54
32	21.53	30.35
33	22.34	31.16
34	23.15	31.97
35	23.96	32.78
36	24.77	33.00
37	25.58	33.00
38	26.39	33.00
39	27.21	33.00
40	28.02	33.00
41	33.00	NA

Note: NA - not applicable

BUS-68015 is capable of transmitting a receive 4 word fixed message.

The BUS-68015 is packaged in a 8.25" x 3.5" x 14.5" enclosure with a handle that can be used as a tilt-stand. Input power is switch-selectable for 115VAC or 230VAC operation. With its compact size, programmability, and special noise tests, the BUS-68015 is ideal for use in bench, field, or factory test applications.

## SET-UP PROCEDURE

To insure correct operation of the BUS-68015, the following step-by-step procedure is recommended:

1. Set the VOLTAGE SELECT switch, located on the rear panel of BUS-68015, to the desired line voltage (115VAC or 230VAC) and connect the line cord to connector J12.
2. Connect the MIL-STD-1553 signal cable to either the direct coupled (J9) or stub coupled (J10) connector on the rear panel.

### NOTE

Accessed through the rear panel is a scope trigger signal labeled "SYNC OUTPUT." The SYNC OUTPUT is TTL compatible and coincident with BUS-68015 transmissions on the data bus, allowing observation and analysis of data bus activity.

3. Connect the MIL-STD-1553 noise cable to the noise connector (J8).
4. Plug in the line cord and depress POWER switch. Once power is applied, it takes approximately 15 seconds for the BUS-68015 to display "ready." During that time the BUS-68015 performs a self-test and identifies itself through the front panel display.
5. Observe the front panel display indications:

```
DDC BUS-68015
1553 Bus Tester
ILC/DDC product
Selftest passed
Software ref: XX
ready
```

By displaying "ready", the BUS-68015 has successfully completed a self-test and the user may begin the functional set-up. If a failure was detected during self-test, "failure" will be displayed, followed by a decimal error code. The types of failures and corresponding error codes are as follows:

### MESSAGE

```
FAILURE-1
FAILURE-2
FAILURE-4
```

### FAILURE

```
ROM TEST
1553 TEST
DISPLAY TEST
```

Note: If there is more than a single failure (for example, failure 1 and failure 2 occur), this condition will be displayed as FAILURE 3.

## BUS-68015 PROGRAMMING

After the power-on self-test has been completed and the display indicates "ready", default conditions occur; they are listed in table 3.

Once "ready" is displayed, the BUS-68015 can be programmed for any specific function. Programming is accomplished either through the front panel keyboard utilizing the liquid crystal display or through the rear panel GPIB (IEEE-488) port.

### GPIB (IEEE-488) Port Programming

To program from the GPIB, set the BUS-68015 address through the GPIB ADDRESS switch located on the rear panel. Note that each switch in the up position represents a logic "1", and each down position a logic "0". Viewing from the rear panel, the leftmost switch sets the MSB and the rightmost sets the LSB. Table 4 lists the GPIB pin functions.

**TABLE 3. POWER-ON DEFAULT CONDITIONS**

DEFAULT CONDITION	RELATED KEYS
In local	LCL
Stub Coupled	CPLR
RT101 SA30 WC32 random data check pass/fail	RT ADRS
SIGNAL LEVEL 150	SIG LVL
NOISE LEVEL 120 test no noise	NSE LVL
00000000;000;00	DSPL EVNT
ANGLE #2 beeper on	DSPL ADJ

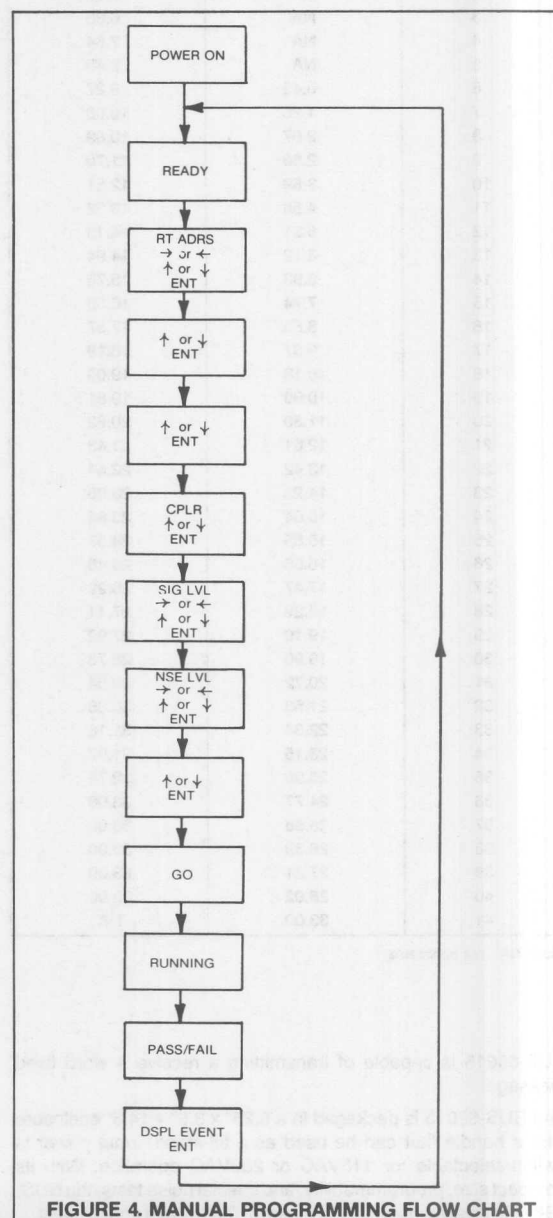
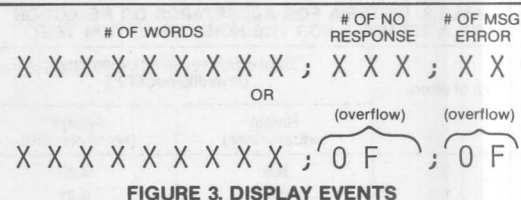
Note: RT=RT ADDRESS, SA=SUBADDRESS,  
and WC=WORD COUNT.

**TABLE 4. GPIB PIN FUNCTIONS**

PIN	FUNCTION	DESCRIPTION
1	DI01	LSB of 8 bit tri-state GPIB bus.
2	DI02	Part of 8 bit tri-state GPIB bus.
3	DI03	Part of 8 bit tri-state GPIB bus.
4	DI04	Part of 8 bit tri-state GPIB bus.
5	EOI	End or Identify input/output.
6	DAV	Data Available input/output.
7	RFD	Ready for Data input/output.
8	DAC	Data Accepted input/output.
9	IFC	Interface Clear input.
10	SRQ	Service Request input.
11	ATN	Attention input.
12	CHAS GND	Chassis ground.
13	DI05	Part of 8 bit tri-state GPIB bus.
14	DI06	Part of 8 bit tri-state GPIB bus.
15	DI07	Part of 8 bit tri-state GPIB bus.
16	DI08	MSB of 8 bit tri-state GPIB bus.
17	REN	Remote Enable input.
18 THRU 24	GND	Digital ground.

## Front Panel Programming

Keys on the front panel (figure 9) are grouped within two bracketed areas: CONTROL and SELECT. The CONTROL keys are used for overall control of the BUS-68015, such as: running (GO key), clearing, stopping, or resetting to the default condition. The keys within the SELECT brackets are used for specific instrument menu set-up selection, such as: selection of mode, coupling, RT address, signal level, and noise level. Also within the SELECT brackets are keys for displaying a particular test event, data entry, and display view adjust. Full functional descriptions of all keys are listed in table 5. These keys are tactile-type (pressure sensitive), requiring only a light touch to activate.



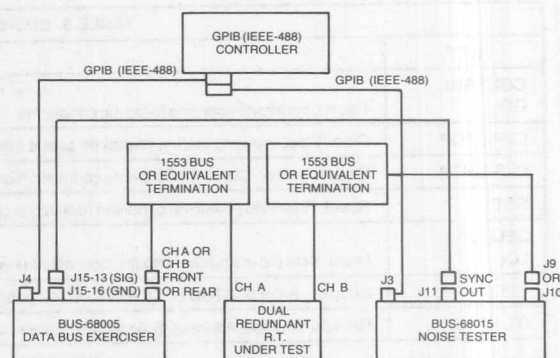
Data and information are presented on a 16-character alphanumeric liquid crystal display. A cursor on the display permits adjusting of levels, addresses and conditions. The cursor is a horizontal bar appearing below the alphanumeric character to be modified. Its position is controlled by left (◀) and right (▶) arrow keys in the SELECT bracket. If the cursor cannot be positioned under a character, it means that modification is not necessary. Events are displayed on the liquid crystal display as shown in figure 3. The steps for manual programming are shown in figure 4.

## PERFORMING DUAL REDUNDANT OPERATION TEST

The dual redundant operation test is performed on a Remote Terminal (RT) configured with a dual redundant data bus, per section 4.6 of MIL-STD-1553. The test is a requirement of the proposed SAE-9 Validation Test plan, and of the Production Test Plan for Aircraft Internal Time Division Command/Response Multiplex Data Remote Terminals.

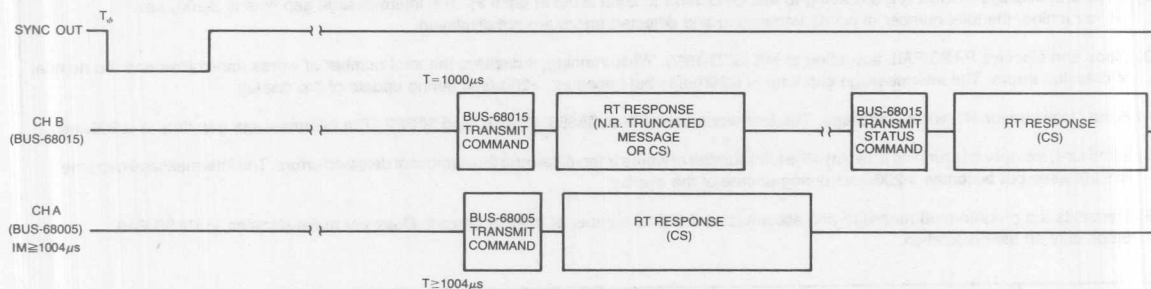
The set-up for performing the dual redundant bus switching test uses a DDC BUS-68005 (MIL-STD-1553 Data Bus Exerciser) and a DDC BUS-68015 (MIL-STD-1553 Noise Tester) in conjunction with a GPIB (IEEE-488 1978) controller. The test is performed on a dual redundant RT as illustrated in figure 5. Table 6 lists the Direct/Stub Coupling Connections for the BUS-68005 and BUS-68015 used for this test.

Figure 6 is a flow chart showing the sequential steps that may be used to perform the Dual Redundant Operation Test. Figures 7 and 8 illustrate timing diagrams for the BUS-68005 and BUS-68015 when an Interrupt Command is sent.

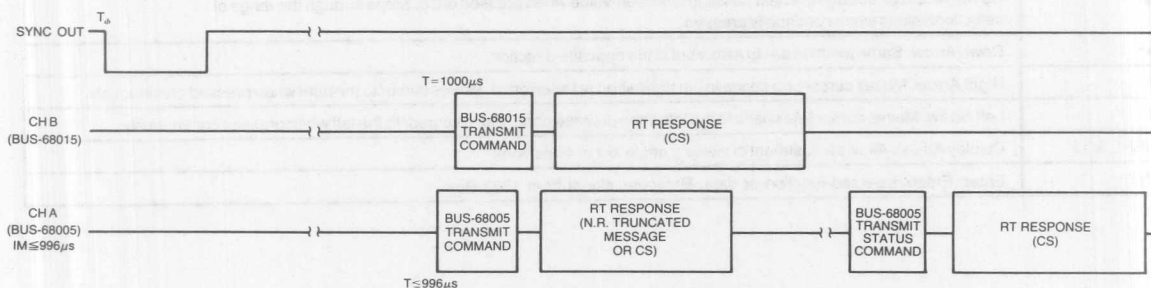


**FIGURE 5. MIL-STD-1553-DUAL REDUNDANT OPERATION TEST SET-UP**

TABLE 6. DIRECT STUB COUPLING CONNECTIONS		
1553 Coupling	BUS-68005	BUS-68015
Direct	Front Panel CH A or CH B	Rear Panel J9
Stub	Rear Panel CH A or CH B	Rear Panel J10



**FIGURE 7. BUS-68005 TIMING FOR DUAL REDUNDANT OPERATION TEST**



**FIGURE 8. BUS-68015 TIMING FOR DUAL REDUNDANT OPERATION TEST**

KEY	FUNCTION
<b>CONTROL</b>	
GO	Starts operation according to set-up conditions.
CLR/STOP	Clear/Stop. Stops operation (removes signal from 1553 Bus).
CLR/CNTR	Clear/Counter. Clears the following counters: Number of Words Transmitted, Number of No Response, and Message Error.
RST	Reset. Resets to power-on condition (default) state, in conjunction with the CLR/STOP key.
<b>SELECT</b>	
LCL	Local. Sets the instrument into the local mode (keyboard controlled).
CPLR	Coupler. Selects STUB or DIRECT noise coupling onto the 1553 Bus.
RT ADRS	Remote Terminal Address. Selects RT address, sub-address, and numbers of words to be transmitted.
Valid Selections for RT ADRS in conjunction with     and the ENT keys are listed below.	
RT 01 SA30 WC32	(default) (See note 1)
random data	(default) (See note 2)
check pass/fail	(default) (See note 2)
random, show tot.	(See note 3)
fixed data	(See note 4)
fixed, show tot.	(See note 5)
run until halted	(See note 6)
Notes:	
(1) RT=RT ADDRESS, SA=SUBADDRESS, and WC=WORD COUNT. (WC≥3).	
(2) Stops and displays PASS/FAIL according to MIL-STD-1553 (criteria listed in table 2). The intermessage gap time is ≤200μsec. While running, the total number of words transmitted and detected errors are not displayed.	
(3) Stops and displays PASS/FAIL according to MIL-STD-1553. While running, it displays the total number of words transmitted and the number of detected errors. The intermessage gap time is ≤200μsec but becomes >200μsec during update of the display.	
(4) Fixed "receive four (4) words" message. The four words are \$0000, \$5555, \$AAAA, and \$FFFF. The intermessage gap time is ≤200μsec.	
(5) Same as 4, except while running it displays the total number of words transmitted and the number of detected errors. The intermessage gap time is ≤200μsec but becomes >200μsec during update of the display.	
(6) Transmits the programmed message and accumulates the total number of detected errors. Does not make decision to PASS/FAIL. Stops only on user discretion.	
SIG LVL	Signal Level. Allows set-up of the signal level on 1553 Bus.
NSE LVL	Noise Level. Allows set-up of the noise level on 1553 Bus.
DSPL EVENT	Display Event. Displays test events after test completion or stopping.
	Up Arrow. Steps through the next possible selection/value when pressed once. Steps through the range of selection/values when continually pressed.
	Down Arrow. Same function as Up Arrow but in the opposite direction.
	Right Arrow. Moves cursor one space to the right when pressed once. Moves cursor to the right when pressed continuously.
	Left Arrow. Moves cursor one space to the left when pressed once. Moves cursor to the left when pressed continuously.
DISPL ADJ	Display Adjust. Allows adjustment of viewing angle to 1 of 4 positions.
ENT	Enter. Enters selected function or data. Removes signal from 1553 Bus.



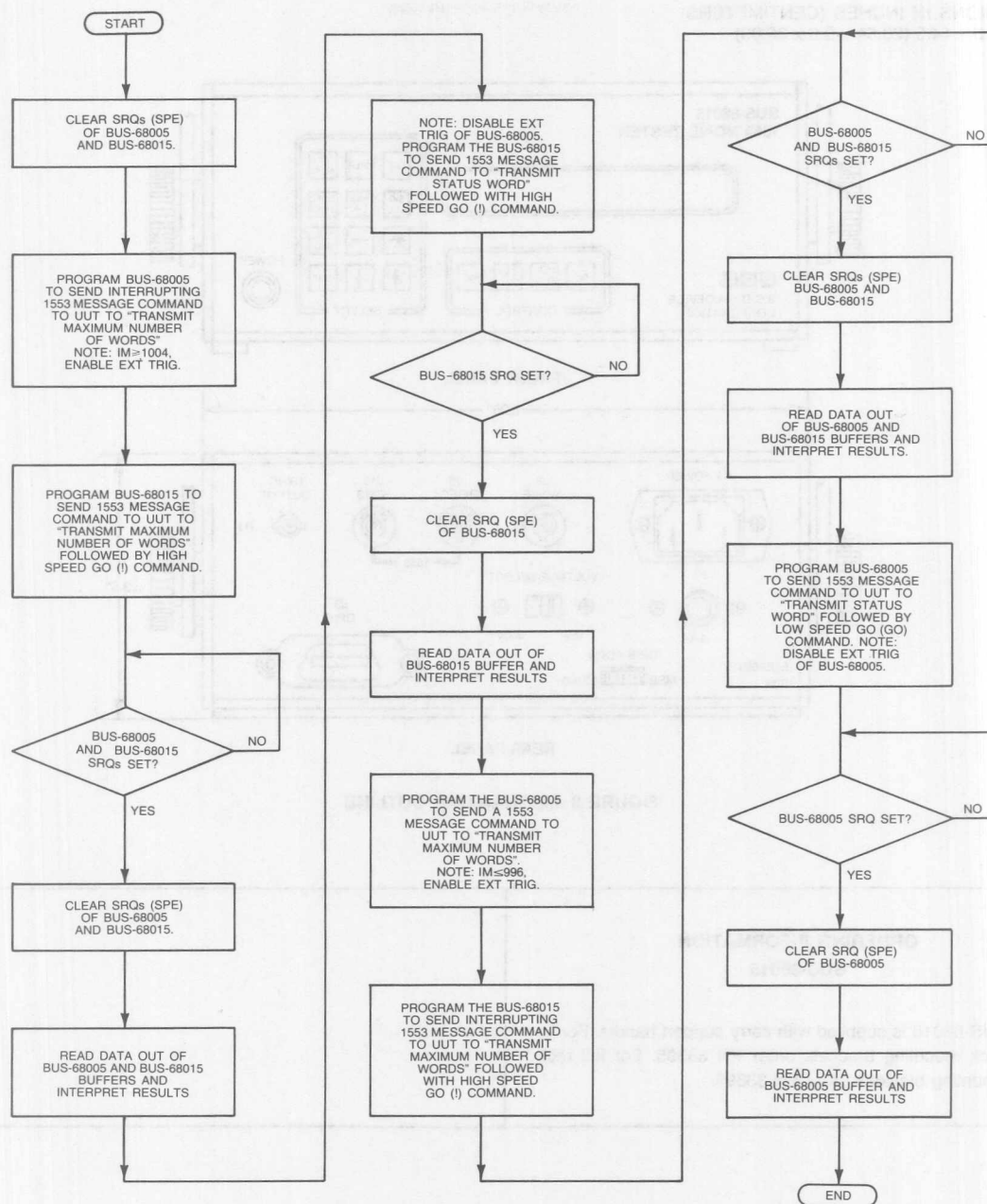


FIGURE 6. DUAL REDUNDANT OPERATION TEST FLOW CHART

DIMENSIONS IN INCHES (CENTIMETERS)  
8.25 x 3.5 x 14.5 (20.64 x 8.0 x 36.83)

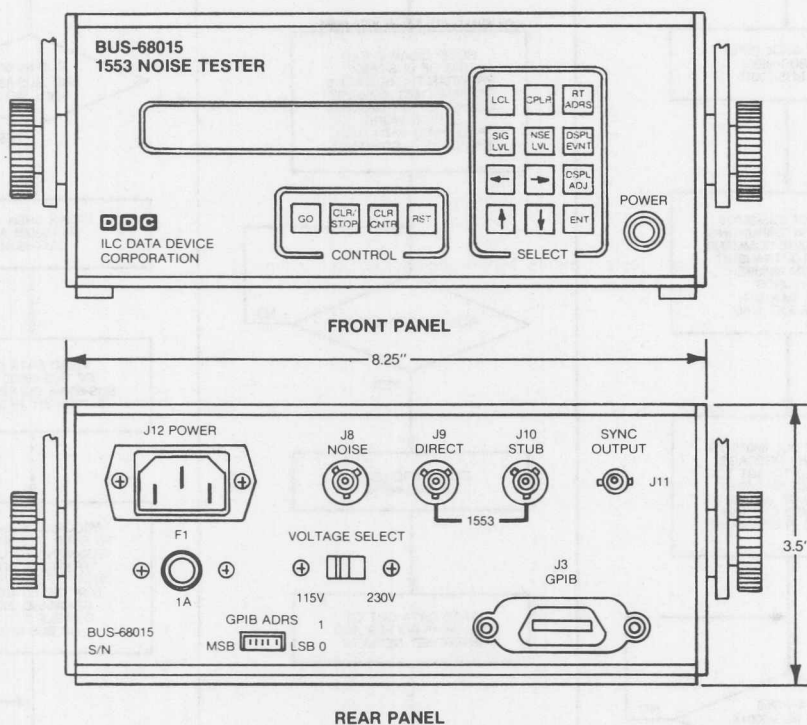
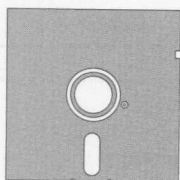


FIGURE 9. MECHANICAL OUTLINE

## ORDERING INFORMATION BUS-68015

Note: BUS-68015 is supplied with carry support handle. For 1/2 rack mounting brackets order PN 33395. For full rack mounting brackets order PN 33396.

## MIL-STD-1553 PROTOCOL SOFTWARE



### DESCRIPTION

The BUS-69005 MIL-STD-1553 Protocol Test software provides a menu-driven Automatic Test Equipment (ATE) environment using an IBM PC/XT/AT host along with DDC's BUS-68005 Data Bus Exerciser and BUS-68015 Noise Tester to perform all protocol tests specified in the SAE RTU Production Test Plan (Section 5.2).

Using a National Instruments GPIB 488 I/O board, the Complete RTU Protocol PTP or any subgroup of tests can be executed simply by choosing the appropriate test(s) and factory or user-definable default parameters from respective menus. Halt on Error, Single Test Execution, Repeat Sequence and Continuous testing options are all supported and menu-selectable.

Test parameters describing Unit-Under-Test (UUT) capabilities and tests to be performed are stored on disk in Configuration files. Multiple Configuration files can be updated and saved on a single disk to meet various device/test requirements. Minimizing operator set-up time, a Configuration file can be saved under the filename DEFAULT. and auto-loaded.

The BUS-69005 software features a simple-to-use on-line help facility allowing the user to select a particular test paragraph in the PTP option, depress the HELP (F1) key, and the respective paragraph within the SAE document is displayed. A print option is also available to produce hard copies of the Configuration files and individual UUT test results.

### FEATURES

- **IMPLEMENTS COMPLETE SAE RTU PRODUCTION TEST PLAN PROTOCOL TESTING (PTP)**
- **MENU-DRIVEN COMPLETE/ PARTIAL PTP EXECUTION**
- **DISK STORAGE OF PTP-SUBSET AND RTU CONFIGURATIONS**
- **SINGLE, CONTINUOUS AND HALT-ON-ERROR EXECUTION**
- **SELECTABLE TEST DATA PRINTOUT**
- **MENU-DRIVEN HELP DISPLAYS PTP PARAGRAPHS**
- **RUNS ON IBM PC/XT/AT® OR COMPATIBLE**

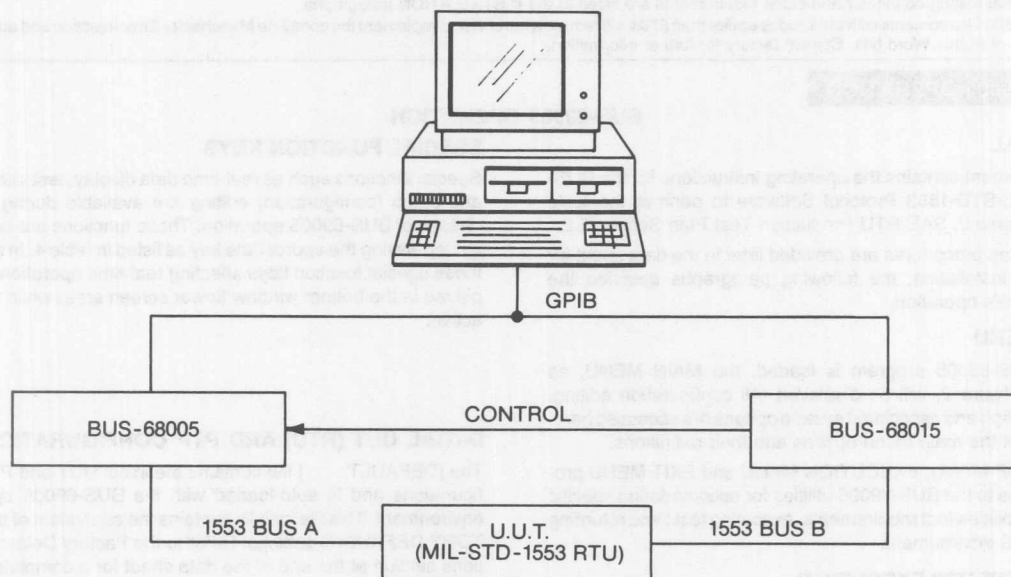


FIGURE 1. BUS-69005 OPERATING ENVIRONMENT

TABLE 1. BUS-69005 REQUIREMENTS AND CAPABILITIES

**HARDWARE REQUIREMENTS†**

IBM PC/XT/AT or Compatible with 256K RAM  
 DDC's BUS-68005 Bus Exerciser††  
 DDC's BUS-68015 Noise Tester (Optional: used only for Bus Switching Test – Section 5.2.2.1, Dual Redundant Operation)  
 National Instruments PC-2A (National Instruments Corp., Austin, TX)

**SOFTWARE REQUIREMENTS**

PC DOS 2.0 or higher

**EXECUTION TIME**

Time per 1553 channel using a Basic IBM PC  
 Sections 5.2.2.4.1.1 and 5.2.2.6: approximately 15 minutes.  
 Rest of 5.2: approximately 5 minutes

**FILES CONTAINED ON BUS-69005 SYSTEM DISK**

Reserved Filenames	Function
BUS-69005.000	BUS-69005 operating environment and associated data.
BUS-69005.001	BUS-69005 operating environment and associated data.
BUS-69005.002	BUS-69005 operating environment and associated data.
COLOR.CFG	System Data.
KEYCODE.CFG	System Data.
GPIB.CFG	System Data
HELP.FLE	System Data
MENUS.MNU	System Data
AAAREAD.ME	ASCII file containing data sheet update information and application information.

**AVAILABLE OPERATIONS**

- Run SAE Production Test Plan (PTP) protocol tests or any subset.
- Define PTP configuration files for execution and/or disk storage.
- Define most RTU configurations in accordance with MIL-STD-1553.
- Print current test configuration and/or execution log.
- User-definable command illegalization/mode code response.
- Selective 5.2.2.6 task execution for RTU development.
- Execute ATP incoming inspection test.

† Additional mating connector and cable requirements are listed in the INSTALLATION paragraphs.

†† BUS-68005 instruments with date codes earlier than 8704 will require a retrofit kit to implement the complete Manchester Error Injection and automatic update of Status Word bits. Consult factory for further information.

**BUS-69005 OPERATION****GENERAL**

This data sheet contains the operating instructions for the BUS-69005 MIL-STD-1553 Protocol Software to perform the tests listed in Table 2, SAE RTU Production Test Plan Section 5.2.

Step-by-step procedures are provided later in the data sheet for hardware installation; the following paragraphs describe the BUS-69005's operation.

**MAIN MENU**

When BUS-69005 program is loaded, the MAIN MENU, as shown in figure 2, will be displayed. All configuration editing, test execution and associated system options are accessed here. Table 3 list the main menu options and their definitions.

The SETUP MENU, EXECUTION MENU and EXIT MENU provide access to the BUS-69005 utilities for accommodating specific UUT capabilities/test requirements, executing tests and returning to the DOS environment.

**COMPLETE PTP EXECUTION**

To run the complete SAE-AE9 RTU PTP protocol tests (Section 5.2), select EXECUTION MENU (from the Main Menu) and then select EXECUTE FULL TEST (Execution Menu).

**BUS-69005 OPERATION****SPECIAL FUNCTION KEYS**

Special functions such as real-time data display, test interruption and setup (configuration) editing are available during various phases of BUS-69005 operation. These functions are accessed by depressing the appropriate key as listed in table 4. In addition, those special function keys affecting real-time operation are displayed in the bottom window (lower screen area) while they are active.

**INITIAL UUT (RTU) AND PTP CONFIGURATIONS**

The [DEFAULT. ] file contains the initial UUT and PTP configurations and is auto-loaded with the BUS-69005 operating environment. This file initially contains the equivalent of the FACTORY DEFAULTS settings. Refer to the Factory Default Conditions section at the end of the data sheet for a complete listing. The DEFAULT. configuration setup can be edited/resaved using the methods outlined below. Note that the active UUT/test configuration at any time is referred to as the *current setup* (SETUP MENU) or *full test* (EXECUTION MENU).

## BUS-69005 OPERATION

**TABLE 2. TESTS INCLUDED IN SAE PTP SECTION 5.2**

SECTION	TEST
5.2.1	RTU RESPONSE TO COMMAND WORDS
5.2.1.1	RTU ADDRESS
5.2.1.1.1	VALID RTU ADDRESS
5.2.1.1.2	INVALID RTU ADDRESS
5.2.1.2	WORD COUNT
5.2.1.3	SUBADDRESS
5.2.1.4	ERROR INJECTION
5.2.2	OPTIONAL OPERATION
5.2.2.1	DUAL REDUNDANT OPERATION
5.2.2.2	MODE COMMANDS
5.2.2.2.1	DYNAMIC BUS CONTROL
5.2.2.2.2	SYNCHRONIZE
5.2.2.2.2.1	SYNCHRONIZE (WITHOUT DATA WORDS)
5.2.2.2.2.2	SYNCHRONIZE (WITH DATA WORDS)
5.2.2.2.3	TRANSMIT STATUS
5.2.2.2.4	INITIATE SELF TEST
5.2.2.2.5	TRANSMIT BIT WORD
5.2.2.2.6	TRANSMITTER SHUTDOWN AND OVERRIDE
5.2.2.2.6.1	DUAL REDUNDANT SHUTDOWN AND OVERRIDES
5.2.2.2.6.2	SELECTIVE SHUTDOWN AND OVERRIDES
5.2.2.2.7	TERMINAL FLAG BIT INHIBIT AND OVERRIDE
5.2.2.2.8	RESET REMOTE TERMINAL
5.2.2.2.9	TRANSMIT VECTOR WORD
5.2.2.2.10	TRANSMIT LAST COMMAND
5.2.2.3	STATUS WORD
5.2.2.3.1	SERVICE REQUEST
5.2.2.3.2	BROADCAST
5.2.2.3.3	BUSY
5.2.2.3.4	SUBSYSTEM FLAG
5.2.2.3.5	TERMINAL FLAG
5.2.2.4	BROADCAST MESSAGES
5.2.2.4.1	RESPONSE TO BROADCAST MESSAGES
5.2.2.4.1.1	BC TO RTU BROADCAST COMMANDS
5.2.2.4.1.2	BROADCAST MODE COMMANDS
5.2.2.4.1.2.1	BROADCAST SYNCHRONIZE (WITHOUT DATA WORD)
5.2.2.4.1.2.2	BROADCAST SYNCHRONIZE (WITH DATA WORD)
5.2.2.4.1.2.3	BROADCAST INITIATE SELF TEST
5.2.2.4.1.2.4	BROADCAST TRANSMITTER SHUTDOWN AND OVERRIDES
5.2.2.4.1.2.4.1	BROADCAST DUAL REDUNDANT SHUTDOWN AND OVERRIDES
5.2.2.4.1.2.4.2	BROADCAST SELECTIVE BUS SHUTDOWN AND OVERRIDES
5.2.2.4.1.2.5	BROADCAST TERMINAL FLAG BIT INHIBIT AND OVERRIDE
5.2.2.4.1.2.6	BROADCAST RESET REMOTE TERMINAL
5.2.2.4.1.3	RTU TO RTU BROADCAST COMMANDS
5.2.2.5	RTU TO RTU TRANSFERS
5.2.2.5.1	RTU TO RTU TRANSMIT
5.2.2.5.2	RTU TO RTU RECEIVE
5.2.2.5.3	RTU TO RTU TIMEOUT
5.2.2.6	ILLEGAL COMMANDS
5.2.2.6A	ILLEGAL TX + RX
5.2.2.6B	ILLEGAL INVALID
5.2.2.6C	ILLEGAL MODE CODE

**TABLE 3. BUS-69005 MAIN MENU OPTIONS**

MAIN MENU	DEFINITIONS
(1) SETUP MENU	Edit RTU (UUT) and/or Test Configuration.
(2) EXECUTION MENU	Run current-configuration PTP or single PTP paragraph.
(3) EXIT PROGRAM	Return control to DOS.

**TABLE 4. SPECIAL FUNCTION KEYS**

FUNCTION KEY	DESCRIPTION
Return	Terminates field entry.
Pg Up	PREVIOUS screen.
Pg Down	ADVANCE to next screen.
Home	Return to PREVIOUS menu.
Del	Delete char at left.
Ins (Insert)	Insert/Overwrite edit
Up Arrow	BACKUP one field
Down Arrow	ADVANCE one field
Left Arrow	Move LEFT one digit
Right Arrow	Move RIGHT one digit
F1	List single tests, display paragraph, Bus Activity window on/off.*
F2	Real time Single Step on/off.*
F3	Real time Repeat Sequence on/off.*
F10	Halt execution.*

\*See EXECUTION MENU for detailed description.

## SETUP MENU OPTIONS

### DESIGNING USER CONFIGURATIONS

All user UUT and Test configuration definition options are provided through the SETUP MENU (see table 5). Using these facilities, the BUS-69005 software can be programmed for the specific capabilities associated with a given RTU and/or specific user test requirements. The setup menu provides access to all means of PTP and UUT configuration editing, data-file handling (save/load configuration) and configuration printing.

**TABLE 5. SETUP MENU**

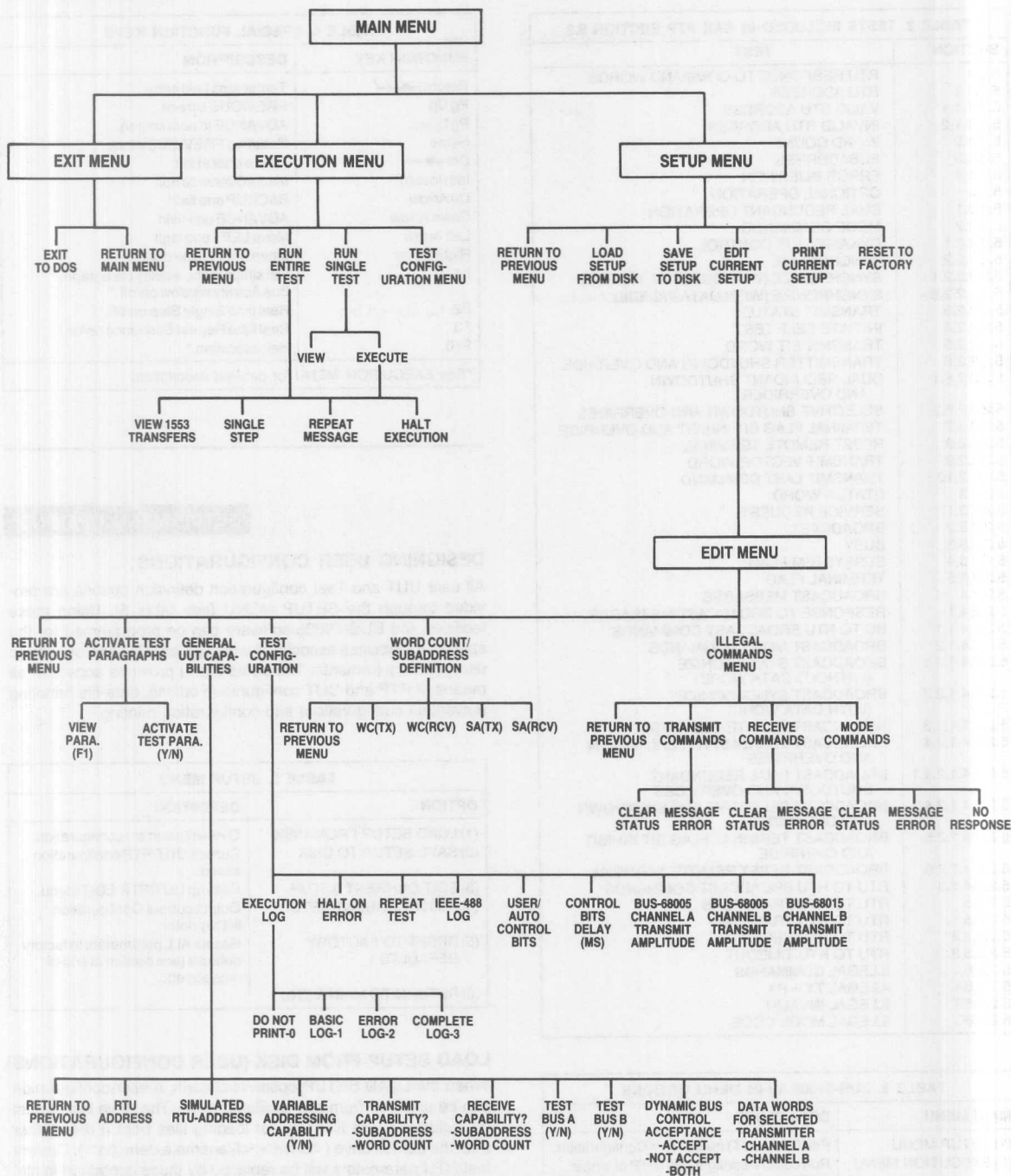
OPTION	DEFINITION
(1) LOAD SETUP FROM DISK	Overwrite current configuration.
(2) SAVE SETUP TO DISK	Current UUT/PTP configuration saved.
(3) EDIT CURRENT SETUP	Calls up UUT/PTP EDIT Menu.
(4) PRINT CURRENT SETUP	Output current Configuration list to printer.
(5) RESET TO FACTORY DEFAULTS	Resets ALL parameters to factory defaults (see section at end of data sheet).
(6) RETURN TO MAIN MENU	

### LOAD SETUP FROM DISK (USER CONFIGURATIONS)

When the LOAD SETUP option is chosen, a user-configuration can be selected from any available drive. The drive letter must be included in the filename for loading files from a drive other than the default drive (<drive>:<filename.extension>). Current test/RTU parameters will be replaced by those contained in file. (Consult DOS manual for details regarding recovery from disk errors.)



**BUS-69005 MAIN MENU**



**FIGURE 2. MAIN MENU STRUCTURE**

## SETUP MENU OPTIONS

### SAVE SETUP TO DISK

This option saves the current setup to disk with a <filename> entered by the user. Both the filename and extension can be user-defined with the following considerations:

1. Filename format for load/save is:  
" <drive letter>: <FILENAME.EXT> "
2. The current default drive is used if none is specified by user.
3. BUS-69005 SYSTEM filenames (except DEFAULT. ) should not be used as this will cause respective files to be overwritten. This is a non-recoverable error, i.e., an alternate (backup) system disk must be used. Consult Table 1 BUS-69005 Requirements and Capabilities for filename list.
4. [DEFAULT. ] is auto-loaded during BUS-69005 loading as the initial current setup.

If the file [(drive):filename.ext] already exists, the user can optionally overwrite the file or terminate the SAVE operation. (Consult the DOS manual for details regarding recovery from disk error.)

### PRINT CURRENT SETUP

This option sends a listing of the CURRENT CONFIGURATION to the printer device (see DOS manual) for a printout of all menu definable variables. A listing of the factory defaults in the PRINT CURRENT SETUP format is available at the end of the data sheet.

### RESET TO FACTORY DEFAULTS

This option replaces *all* configuration values in the CURRENT SETUP to reflect the Complete PTP as performed on a full-function dual-redundant RTU. A list of factory defaults is provided at the end of the data sheet.

## EDIT MENU

### EDIT CURRENT SETUP

This option activates the EDIT MENU, allowing the user to describe the capabilities of the specific UUT to the BUS-69005 software (see table 6). Deviations from the UUT and test requirements as outlined by the Factory Defaults can be input and then executed and/or saved to disk for future use. Note that the EDIT MENU is extensive; refer back to figure 2 for detailed structure.

TABLE 6. EDIT MENU

OPTION	DEFINITION
(1) RETURN TO MAIN MENU	
(2) ACTIVATE TEST PARAGRAPHS	Select PTP paragraphs to execute.
(3) GENERAL U.U.T. CAPABILITIES	Default (Global) values menu.
(4) TEST CONFIGURATION	Execution Sequence/Log menu.
(5) WORD COUNT/SUBADR DEFINITION	Select word count and subaddress for transmit and receive.
(6) ILLEGAL COMMANDS	Select transmit/receive/mode codes illegal commands.

**EDITING A SETUP.** The current setup (RTU/PTP configuration) can be altered by:

1. LOADING a SETUP (Configuration file), this overwrites all parameters.
2. RESETing to FACTORY PRESETS, this replaces all parameters in current setup with factory defaults.
3. EDITing the CURRENT SETUP (updating individual parameters).

The new CURRENT SETUP can then be executed, printed and/or saved to disk using any filename and extension except those reserved by BUS-69005. ([DEFAULT. ] can be overwritten for use as a customized auto-load setup).

### ACTIVATE/VIEW TEST PARAGRAPHS

This option provides the user with a multi-screen listing of all SAE-AE9 PTP (section 5.2) paragraph titles. The user can select paragraphs for execution and/or view the corresponding test plan paragraph by pointing to the appropriate paragraph (using arrow keys) and selecting Yes (Enable test), No (Disable test) or F1 (View).

### GENERAL UUT CAPABILITIES

This option allows the user to select default (global) values for RTU ADDRESS, transmit/receive SUBADDRESS and transmit/receive WORD COUNT. TRANSMIT enable/disable, RECEIVE enable/disable, Test BUS-A enable, Test BUS-B enable and USER/AUTOMATIC RTU Address and status bits are also provided within this menu.

**RTU ADDRESS (nn).** This option sets the RTU address to nn for all RTU testing except variable addressing testing (see below).

**SIMULATED RTU ADDRESS (nn).** This option sets an address of nn for the RTU simulated by the BUS-68005 during RTU-RTU transfers.

## SETUP MENU OPTIONS

**VARIABLE ADDRESSING (Y/N).** Selecting "Y" (Yes) enables testing of "variable" RTU addresses (addresses 0, 1, 2, 4, 8 and 16) in addition to that specified as the DEFAULT RTU address (above). See AUTOMATIC CONTROL CIRCUIT and related paragraphs in the INSTALLATION AND STARTUP sections.

**TRANSMIT CAPABILITY/RECEIVE CAPABILITY: (Y/N).** These options specify the ability of the RTU under test to process transmit and/or receive commands respectively.

**DEFAULT SUBADDRESS (nn).** This option sets all RTU subaddress references to the value input as nn. This value can be overridden by entering the desired subaddress(es) using the SUBADDRESS/WORD COUNT MENU, SA(Tx) and/or SA(Rcv) options.

It should be noted that the default subaddress is NOT utilized in two messages in which a Manchester encoding error is induced in the parity-bit position of a command word (Error Injection: 5.2.1.4). In these messages, one of the default subaddress bits is inverted to force the command word parity bit to a desired state.

**DEFAULT WORD COUNT (nn).** This option sets all RTU word count references to the value input as nn. This value can be overridden by entering the desired word count(s) using the SUBADDRESS/WORD COUNT MENU, WC(Tx) and/or WC(Rcv) options.

**TEST BUS A/TEST BUS B: (Y/N).** These options allow tests (full PTP or single test) to be executed on the primary (Bus A), secondary (Bus B) or both MIL-STD-1553 busses by selecting "Y" (Yes) to enable or "N" (No) to disable each. The bus being used is displayed during test execution and in the resulting execution log (see EXECUTION LOG).

**DBC ACCEPT.** This option allows the user to enable ACCEPT and/or NON-ACCEPT responses to the Dynamic Bus Control Mode Code command. The user can select testing for ACCEPT bus control, NON-ACCEPT bus control, or BOTH.

**SELECTED TRANSMITTER SHUTDOWN AND OVERRIDE (nnnn).** Independently programmable for Channels A and B in four digit HEX. Default = 0001 for Channel A and 0000 for Channel B.

## TEST CONFIGURATION

This option provides yes/no selections including Halt On Error, Repeat Test (until Halt-on-error, if enabled), or a Halt Execution (F10) and execution log printing.

**PRINT EXECUTION LOG (n).** This option outputs selected run-time information to the PC's printer port in one of three forms by entering the number of the desired selection. The following selections are illustrated in the Print Execution Log example shown at the end of the data sheet.

0. Do NOT print execution log
1. Print BASIC Log
2. Print EXPANDED ERROR Log
3. Print EXPANDED COMPLETE Log

**HALT ON ERROR (Y/N).** This option affects execution flow by either terminating (Yes) or continuing test execution in the event of a test failure. Note that test execution will begin with the first test specified rather than continuing from a point following the test failure.

**REPEAT TEST (Y/N).** This option allows the continuous repetition of a single test or group of tests (execute full PTP). This may also be used in conjunction with HALT ON ERROR (above) to isolate intermittent failures. Note that this feature is also provided as a real-time function using the F3 key.

**IEEE-488 LOG (Y/N).** This option (default = off) allows the user to save all GPIB transfer data. Data including time tag (time of day), test paragraph, transfer direction (read, write tester), address, number of data words and data bytes (HEX) are written/overwritten to a system designated disk file [IEEE488.DBG] with each FULL TEST or SINGLE TEST execution instruction. Note that a Full Test of one bus requires approximately 2M bytes of storage per bus; therefore, this option is not saved to configuration files.

**USER/AUTOMATIC CONTROL BITS (U/A).** This option provides software control of status word bits, variable RTU addressing and RTU reset. The parallel I/O port of the BUS-68005 provides 5 RTU address outputs, 1 address parity output (odd parity), 5 status word flag outputs and an RTU RESET signal. These options may be used by constructing a simple circuit to interface between the BUS-68005's parallel I/O port and the test fixture or subsystem side of the RTU Under Test (UUT) and selecting automatic RTU address/status bits control.

The **AUTOMATIC** option supports fully unattended testing by updating the appropriate address and status signals and then pausing for a user-programmable test set/UUT-update delay time before resuming the test sequence. The delay time is applicable for automatic operation only and is programmable with a range from 0 to 999 ms with a default value of 0 (less than 1 ms).

The **USER** (default) option causes the RTU address and status outputs to be updated, an "Operator Action Required" message to be displayed and program execution to halt. The user may then modify the test configuration as required and then depress the RETURN key to resume test execution.

## SETUP MENU OPTIONS

**CONTROL BITS DELAY (nnnn).** This option allows the user to specify a test-execution pause interval (in ms) following control bits output for UUT updating before resuming execution. Control bits delay is valid only when utilizing AUTOMATIC CONTROL BITS operation. The range for Control Bits Delay is 0 to 999 ms. See AUTOMATIC CONTROL CIRCUIT and related paragraphs in the INSTALLATION AND STARTUP data sheet section.

**BUS-68005 CHANNEL A/B TRANSMIT AMPLITUDE (nn).** These options allow user selection of appropriate transmitter amplitudes for direct coupled and transformer coupled UUT configurations. Consult TRANSMIT AMPLITUDES in the INSTALLATION AND STARTUP section.

**BUS-68015 CHANNEL B TRANSMIT AMPLITUDE (nn).** This option allows user selection of appropriate transmitter amplitudes for direct coupled and transformer coupled UUT configurations. Note that only a Channel B value is required (Dual Redundant Testing only). Consult TRANSMIT AMPLITUDES in the INSTALLATION AND STARTUP data sheet section.

### WORD COUNT/SUBADDRESS

This option provides a means of overriding the default options established via the DEFINE UUT sub-menu for the PTP Subaddress Test and the Word Count Test using transmit and receive commands respectively (see above). Undefined values remain set at DEFINE UUT selected values.

**SUBADDRESS DEFINITION.** This allows each subaddress to be enabled or disabled for transmit and/or receive commands (using the SUBADDR(TX) and SUBADDR(RX) menus). Enabled subaddresses will be tested per PTP paragraph 5.2.1.3. The word count for each transmit and receive enabled subaddress can also be specified; unspecified word counts are accepted as the default value specified in the DEFINE UUT CAPABILITIES sub-menu.

**WORD COUNT DEFINITION.** This allows the user to define which word counts the UUT is capable of transmitting and receiving (using the WORD COUNT(TX) and WORD COUNT(RX) menus respectively). The enabled word counts will be tested per PTP paragraph 5.2.1.2. The subaddress for each enabled transmit and receive word count can also be specified; unspecified subaddresses are accepted as the default value specified in the DEFAULT UUT CAPABILITIES sub-menu.

### PTP PARAGRAPH 5.2.2.6 ILLEGAL COMMANDS

Production Test Plan paragraph 5.2.2.6 (Illegal Commands) has been subdivided into three sections (A, B, and C) in order to provide a mechanism for developing/debugging command illegalization circuitry (PROM) for the RTU/Subsystem under test.

As with all tests, selecting a higher level test will execute all lower level tests (for example, selecting 5.2.2.6 will select 5.2.2.6 A, B, and C as well).

**Section A (PTP steps 1-4).** These steps test all legal and illegal non-broadcast non-mode code commands. Default: all legal commands' expected response is Clear Status. May be overwritten as illegal with an expected response of Status Word with Message Error bit set.

**Section B (PTP steps 5-10).** These steps test invalid illegal commands. This verifies that the RTU's response is "No Response" for invalid illegal commands.

**Section C (PTP steps 11-12).** These steps test all 128 combinations of T/R bit, subaddress 00 and 1F, and 32 possible non-broadcast mode code commands.

- \* = CLEAR STATUS
- = NO RESPONSES
- . = STATUS WORD WITH MESSAGE ERROR BIT SET

A complete list of the steps in Section 5.2.2.6 of the PTP can be viewed through the HELP screens in the BUS-69005.

### ILLEGAL COMMANDS MENU

The respective illegal commands menus allow the illegalization of selected Transmit, Receive and Mode commands (those commands that are not accepted by a given UUT). Expected RTU-response types can be assigned to each command; an error will be flagged if the UUT fails to provide the assigned response type.

**ILLEGAL MODE COMMANDS.** This option allows the selective illegalization of mode commands. The user can specify "C" (Clear status: no status bits set), "N" (No Response expected), "M" (Message Error type response), or "C" (Clear Status) as an expected response to each possible mode command.

**ILLEGAL TRANSMIT AND ILLEGAL RECEIVE COMMANDS MENUS.** These menus allow the illegalization of selected transmit and/or receive commands respectively. A clear response is expected in response to Legal commands (select "L") and a message error condition is expected for Illegalized commands (select "I").

**FACTORY DEFAULTS/EXPECTED RESPONSE TO ILLEGAL COMMANDS.** A CLEAR RESPONSE is expected for (1) all non-reserved mode commands with correct T/R-bit (except Selected Transmitter Shutdown/Override) and (2) legal non-mode commands. NO RESPONSE is expected for undefined mode commands only. A response with a MESSAGE ERROR is expected for (1) selected transmitter shutdown/override, (2) all reserved mode codes, (3) defined commands with incorrect T/R bit and (4) illegalized transmit/receive commands.



## EXECUTION MENU OPTIONS

### EXECUTION MENU OPTIONS

The execution menu provides access to actual test *execution* including complete PTP protocol testing, user configurations and single test (individual portions of paragraph 5.2) execution.

### EXECUTE ENTIRE PTP

This option is selected by depressing the key corresponding to the appropriate Execution Menu Selection. Note that test execution begins immediately and can be interrupted by depressing the F10 (HALT EXECUTION) key.

The ENTIRE PTP represents the setup (configuration) currently residing in memory. This setup could have been loaded from a disk file, auto-loaded with the BUS-69005 operating environment (DEFAULT. file – see general operation), factory presets and/or an edited from of one of these setups.

### REAL-TIME FUNCTIONS

These functions allow the user to alter the test execution flow by polling for function actuation following the completion of each test.

Each feature can be used independently or in conjunction with most other REAL-TIME and TEST EXECUTION functions. Prompts within the BOTTOM WINDOW indicate the condition initiated (toggle on/off) by depressing the key indicated.

**VIEW 1553 TRANSFERS (F1).** Depressing the F1 key toggles the View 1553 Transfers on/off function. Switching to the ON position ("F1 = OFF" will be displayed) causes the BUS ACTIVITY WINDOW to become active and all data (command/data/status) transmitted on the active 1553 bus to be displayed. Note that execution time will be increased by activating this function.

**SINGLE STEP (F2).** Depressing the F2 key toggles the Single Step on/off function. Switching to the ON position ("F2 = OFF" will be displayed) causes test execution to pause following transmission of each message; continue testing by depressing any key.

**REPEAT SEQUENCE (F3).** Depressing the F3 key toggles the Repeat Test on/off function. Switching to the ON position ("F3 = OFF" will be displayed) causes the current PTP test paragraph to be repeated until (1) the test-in-progress is completed following Repeat Test disable (i.e., off) or (2) the UUT fails the test with Halt On Error enabled.

**HALT EXECUTION (F10).** Depressing the F10 key causes test execution to halt following the current transmission. Subsequent testing will begin from the start of the sequence; testing cannot be continued from the halted instruction.

**ADDITIONAL FEATURES.** Execution log printing, disk storage of IEEE-488 data, BUS-68005 user/automatic mode implementation, transmit amplitude specification and additional non-real time access features are provided via the TEST CONFIGURATION and DEFINE UUT menus; see specific paragraphs for detailed discussion of these topics.

### RUN SINGLE TEST

Selecting Single Test from the EXECUTION MENU provides the user with the following options:

- (1) Entering a test paragraph or sub-paragraph number for immediate execution. When a paragraph number is entered, all tests within that paragraph and respective sub-paragraphs are executed based on the current test and UUT configurations (current setup).
- (2) Depressing F1: providing test paragraph list. From the test paragraph list the user may then select any paragraph or sub-paragraph using the arrow keys and then depress F1 to display test paragraph or depress F2 and execute test paragraph.

### EXITING THE BUS-69005 PROGRAM

The EXIT MENU should be used to exit the BUS-69005 operating environment. Do not exit by power-down or Ctrl-Alt-Del. To insure proper program parameters, exit from any menu by simply selecting option "1" and then answering "Y" " ← " to the "Are You Sure" prompt in the EXIT MENU.

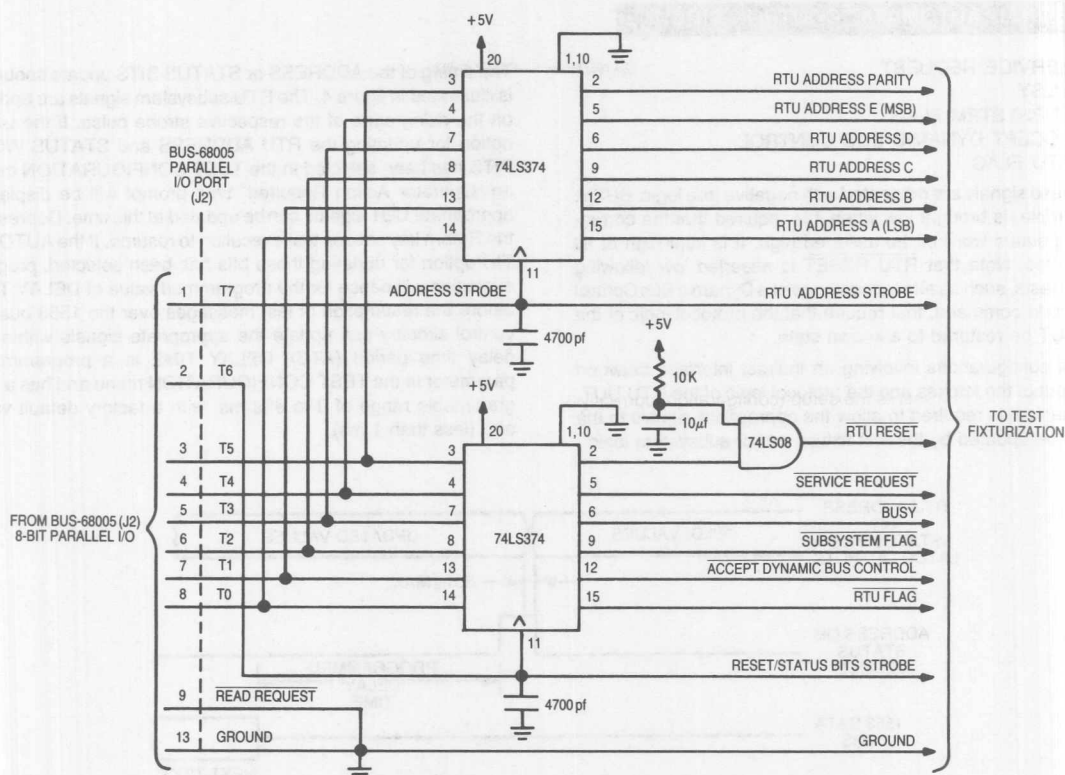
## BUS-69005 OPERATING ENVIRONMENT

### BUS-69005 OPERATING ENVIRONMENT

Figure 6 on the last page illustrates the full electrical set-up required to use the BUS-69005 operating environment. Any additional mating connectors or cables are listed in table 7 and described in the INSTALLATION paragraph. Note that the BUS-68015 Noise Tester and the Automatic Control circuit for RTU address and status word bits are optional items; their operations are described in the following paragraphs.

**BUS-68015 NOISE TESTER.** The BUS-68015 Noise Tester is only used for the Bus Switching Test (refer to Section 5.2.2.1, Dual Redundant Operation) and can be eliminated if this test is not required. The BUS-69005 software self-adjusts to either configuration.





Note: See figure 6 on the last page for the complete operating environment.

FIGURE 3. OPTIONAL AUTOMATIC CONTROL CIRCUIT

### OPTIONAL AUTOMATIC CONTROL CIRCUIT

An optional circuit, (see figure 3), provides a method for varying the RTU Address and status word flag bits under direct control of the BUS-69005 software. If enabled, (DEFINE UUT menu), the testing of the RTU's variable address capability is performed per paragraph 5.2.1.1.1 of the PTP. Varying the status word bits is required for the following paragraphs:

- 5.2.2.2.1 Dynamic Bus Control
- 5.2.2.2.7 Terminal Bit Flag Inhibit and Override
- 5.2.2.3.1 Service Request
- 5.2.2.3.3 Busy
- 5.2.2.3.4 Subsystem Flag
- 5.2.2.3.5 Terminal Flag

Also **RTU RESET** is asserted low following tests, such as Dynamic Bus Control Acceptance, that require the RTU UUT to be restored to a known state.

**AUTOMATIC CONTROL CIRCUIT OPERATION.** As shown in figure 3, the ADDRESS and STATUS signals from this circuit interface either directly to the protocol logic of the RTU UUT or indirectly, through the test fixture and/or the subsystem under test.

Bit 0 (LSB) through bit 5 of the BUS-68005 parallel port (J2) convey the data to update the 74LS374 latches in the interface circuit. Bit 7 (MSB) from the parallel port is used as a positive edge-triggered strobe to update the RTU ADDRESS and RTU ADDRESS PARITY signals. Bit 6 is used as a strobe to latch in the desired signals for the RTU RESET and RTU status word bit signals.

Under control of the BUS-69005 software, the PC communicates to the Exerciser parallel port by means of the DMA IEEE-488 (GPIB) interface.

The upper latch shown in the optional interface circuit provides the RTU ADDRESS signals, RTU ADDRESS E (MSB) through RTU ADDRESS A (LSB) and the RTU ADDRESS PARITY signal. The odd sense of the RTU ADDRESS PARITY signal represents odd parity based on the value of RTU ADDRESS E through RTU ADDRESS A. This signal is required to enable operation of most 1553 RTUs. Both the RTU ADDRESS and RTU ADDRESS PARITY signals are output with positive true logic sense.

The lower latch shown in figure 3 provides an RTU RESET signal and 5 signals to control various status word flag bits for the RTU UUT. The 5 status word control signals are:

SERVICE REQUEST  
 BUSY  
 SUBSYSTEM FLAG  
 ACCEPT DYNAMIC BUS CONTROL  
 RTU FLAG

All of these signals are presented with negative true logic. BUSY, for example, is brought low when it is required that the corresponding status word bit be asserted high. It is kept high at all other times. Note that RTU RESET is asserted low following specific tests, such as after acceptance of a Dynamic Bus Control mode code command, that require that the protocol logic of the RTU UUT be restored to a known state.

For test configurations involving an indirect interface between the output of the latches and the protocol logic of the RTU UUT, a mechanism is required to allow the appropriate signals to the RTU to be updated by the test fixture and/or subsystem logic.

The timing of the ADDRESS or STATUS BITS update sequence is illustrated in figure 4. The RTU subsystem signals are updated on the rising edge of the respective strobe pulse. If the USER option for updating the RTU ADDRESS and STATUS WORD BITS has been selected in the TEST CONFIGURATION menu, an "Operator Action Required" type prompt will be displayed; appropriate UUT signals can be updated at this time. Depressing the Return key causes test execution to resume. If the AUTOMATIC option for updating these bits has been selected, program execution will pause for the programmed value of DELAY TIME before the resumption of test messages over the 1553 busses; control circuitry can update the appropriate signals within this delay time period (ATE). DELAY TIME is a programmable parameter in the TEST CONFIGURATION menu and has a programmable range of 0 to 999 ms, with a factory default value of 0 (less than 1 ms).

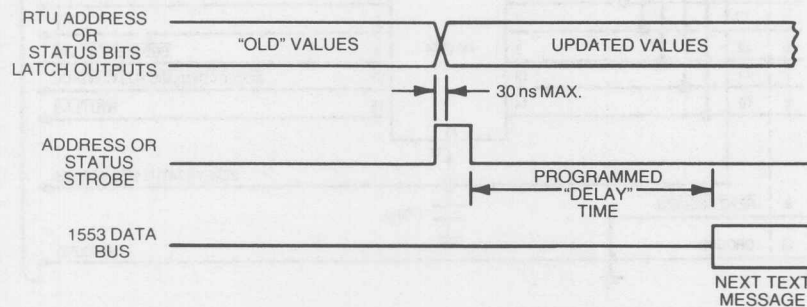


FIGURE 4. AUTOMATIC CONTROL CIRCUIT TIMING

## TRANSMITTER AMPLITUDES

The protocol portion of the PTP specifies the bus tester transmitter amplitudes of 3.0 Vp-p for direct coupled stubs for the RTU UUT, or 2.1 Vp-p for transformer coupled RTUs.

**BUS-68005 TRANSMITTER AMPLITUDE.** The transmitter amplitude of the BUS-68005 is variable from approximately 0 to 10 Vp-p across 35 ohms in 255 steps of approximately 40 mV. The factory default relative amplitude setting of 87 provides an output of approximately 3.0 Vp-p across 35 ohms, as the test plan requires for direct coupled RTUs. A programmed relative amplitude of 46 provides an approximate amplitude of 2.1 Vp-p across 70 ohms, as required for transformer coupled RTUs.

**BUS-68015 TRANSMITTER AMPLITUDE.** The transmitter amplitude of the BUS-68015 is variable from approximately 0 to 6.5 Vp-p from its direct coupled output (J9) across 35 ohms. The factory default relative amplitude setting of 117 provides an approximate output of 3.0 Vp-p across 35 ohms. A programmed relative amplitude of 51 provides the 2.1 Vp-p output across 70 ohms required for testing of transformer coupled RTUs.

**PROGRAMMING THE TRANSMITTER AMPLITUDE.** By means of the TEST CONFIGURATION menu, the transmitter amplitude is a programmable parameter. The transmitter amplitudes for Channel A from the BUS-68005, Channel B from the BUS-68005 and Channel B from the BUS-68015 (for the Bus Switching Test) are independently programmable. For testing of transformer coupled RTUs, the three parameters should be programmed to the values mentioned above. In addition, the programmed values may be further adjusted to compensate for variations in cabling and loading. The recommended method for doing this is to program the respective transmitter amplitudes by means of the instrument front panel keyboards and increment or decrement the relative output value (0 to 255) while viewing the data bus output on an oscilloscope. The bus waveform should be viewed differentially at a point as close as possible to the input to the RTU UUT. The final adjusted values should then be entered as the respective parameters in the TEST CONFIGURATION menu. Refer to the BUS-68005 and BUS-68015 instruction manuals for further information regarding the programming of transmitter amplitudes.

## PC CONFIGURATION

### PC CONFIGURATION

To use the BUS-69005 ATE operating environment, a National Instruments GPIB-PC2A controller card must be installed in one of the expansion slots *other than slot 8* in the PC. The GPIB address is fully programmable using the software installation procedure described in step 3 of the GPIB-PC2A INSTALLATION paragraph.

### GPIB-PC2A CONTROLLER CARD CONFIGURATION

To configure the GPIB-PC2A controller card, proceed as follows:

1. Install jumper I7. Jumpers I2 through I6 not installed. Set switch U17 positions 0, 1, and 2 to the OFF (1) position. (Enables interrupt line 17).
2. Set switch U17 positions 13 and 14 to the ON (0) position. (Configures GPIB-PC2A card's base address to 02E1 HEX).
3. Install jumpers R1 and A1. Jumpers R2, A2, R3, and A3 are not installed. (Designates DMA Channel 1 for the GPIB-PC2A card's use to access memory.)

For additional information, consult the GPIB-PC User Manual.

### GPIB-PC2A CONTROLLER CARD INSTALLATION

Once the GPIB-PC2A is configured, plug into one of the expansion slots (other than slot 8) in the PC and perform the following:

1. Connect the GPIB-PC2A to the IEEE-488 (GPIB) ports of BUS-68005 Data Bus Exerciser and the BUS-68015 Noise Tester (if used) using any standard 24-conductor GPIB cable.

#### Note

To assure that the BUS-68005 and BUS-68015 operate properly, turn power off before updating the GPIB addresses and make certain the BUS-68005's I/O SELECT SWITCH on the rear panel is set to the GPIB position.

2. Set the GPIB address of the BUS-68005 and BUS-68015 using the rear panel switches on each. The MSB/LSB and logic sense are marked on the panels. Note that the selected addresses must agree with the respective addresses specified in the BUS-69005's INSTALL program. The factory default addresses are 0 for the GPIB-PC2A card, 1 for the BUS-68005, and 2 for the BUS-68015.

### GRAPHICS ADAPTER

Make sure that any color graphics enhancement cards in the PC's expansion slots are set for CGA (color graphics adapter) compatibility. The BUS-69005 software adapts automatically to monochrome and color monitors.

TABLE 7. SUGGESTED MATING CONNECTORS

BUS-68005	CONNECTOR
J2 (PARALLEL I/O)	TRW DB25S (DB25 FEMALE)
J15 (TRIGGER INPUT)	AMPHENOL 17-10500-1-390 50-PIN FEMALE
J9, J10 (CHA A, CHA B)	TROMPETER PL75-47 TRIAX MALE
BUS-68015	CONNECTOR
J9 (DIRECT COUPLING)	TROMPETER PL75-47 TRIAX MALE
J11 (SYNC OUTPUT)	PONONA 4488 BNC MALE
BUS CABLES	TROMPETER 14949 78 OHM TRIAX

### TEST EQUIPMENT CONNECTIONS

Once the GPIB-PC2A has been configured and installed and the color enhancement cards in the PC are set for CGA, refer to figure 3 and table 7 and perform the following steps:

1. Connect the GPIB-PC2A controller to GPIB ports on BUS-68005 (J4) and BUS-68015 (J3).
2. Connect the SYNC OUTPUT (J11) from the BUS-68015 to the TRIGGER INPUT (J15) of the BUS-68005.

#### Note

When connecting 1553 Bus A and B, the use of two 35 Ohm resistors (direct coupling) or two 70 Ohm resistors (transformer coupling) to simulate the two data busses complies with the PTP for the protocol portion of the test.

3. Connect BUS-68005 CH. A (J9) to PRIMARY BUS A input of RTU UUT.
4. Connect BUS-68005 CH. B (J10) and BUS-68015 DIRECT (J9) to SECONDARY BUS B input of RTU UUT.

### OPTIONAL AUTOMATIC CONTROL INTERFACE CIRCUIT

If the optional automatic control interface circuit is used, refer to figure 3 and perform the following:

1. Connect PARALLEL I/O (J2) of BUS-68005 to the external circuit. Keep ground connection from J2-9 and J2-13 as close as possible to the J2 connector pins to minimize noise.
2. Connect outputs of Interface Circuit to RTU test fixture or Subsystem Interface.


## IBM PC/XT/AT OR COMPATIBLE SET-UP

### IBM PC/XT/AT OR COMPATIBLE SET-UP

To "boot up" the PC, place the DOS SYSTEM disk (DOS 2.0 or higher) in the default drive; then, if the power switch is in the off position, toggle the power switch to the on position. If the PC is already powered up, (1) depress the Ctrl, Alt and Del keys simultaneously, or (2) toggle the power switch to the off position and then back to the on position. After a short (self test) period, the following will appear:

```
A: Date
Current date is xxx nn-nn-yy
Enter new date:
```

(xxx = Abbr. day of the week; nn = Num. day, month, year)


Type the new date in the SAME format as the current date appears followed by  (Return). The new time will then be requested. Follow the same procedure as in entering the date making sure that the time is entered in the same format as it is presented.

## LOADING THE INS69005 (INSTALLATION) PROGRAM

### LOADING THE INS69005 (INSTALLATION) PROGRAM


The complete BUS-69005 Installation Menu is shown in figure 5.

#### Note

Throughout this data sheet, when keyboard entries are required from the user, they will be enclosed in double quotation marks ("  ").

Load the BUS-69005 Installation program by placing the BUS-69005 system disk in the default drive and typing "INS69005" ("Hard drive" users select drive C: and the appropriate subdirectory). The installation menu will appear providing the options listed in table 8.


### COLOR DEFINITION

This installation option provides listings of all available foreground and background colors as well as all available menus. Two spare windows have been included for future expansion and are not used in the current BUS-69005 software. Simply select the appropriate window, background and foreground numbers, depressing the  key following each entry (see table 9 for window definitions).


### BACKING UP THE BUS-69005 SYSTEM DISK

Cover the notch in the BUS-69005 SYSTEM disk with a write-protect tab to prevent accidental erasure. Place the BUS-69005 SYSTEM disk in the PC's A drive. To make a backup copy, proceed as follows:

For a two drive system, type:

```
DISKCOPY A: B: 
```

For single drive systems, type:

```
DISKCOPY A: A: 
```

At the prompt, insert the appropriate disk. To continue execution, press any key. When the PC prompts "COPY (?) ANOTHER", type "NO". The A> prompt will be displayed.

### INSTALLING THE SYSTEM DISK FILES ON A HARD DISK SYSTEM

Boot up the PC as described above. Insert the BUS-69005 SYSTEM disk in the current default drive and type:




```
MD C:\<subdirectory name> 
CD \<subdirectory name> 
COPY *.* C:\<subdirectory name> 
```

TABLE 8. BUS-69005 INSTALLATION MENU

OPTION	FUNCTION
(1) COLOR DEFINITION	Foreground/Background color: each Window.
(2) KEYBOARD DEFINITION	For accomodating custom keyboard layouts.
(3) GPIB DEFINITION	GPIB Address.
(4) EXIT	Return to DOS.

### KEYBOARD DEFINITION

This option allows the user to re-assign each key function to any key on his or her current keyboard. For each key-name displayed, depress the corresponding key for assignment. Note that a given key function can be applied to only one key. See SPECIAL FUNCTION KEYS paragraph for a complete description.



## INSTALLATION (INS69005) MENU

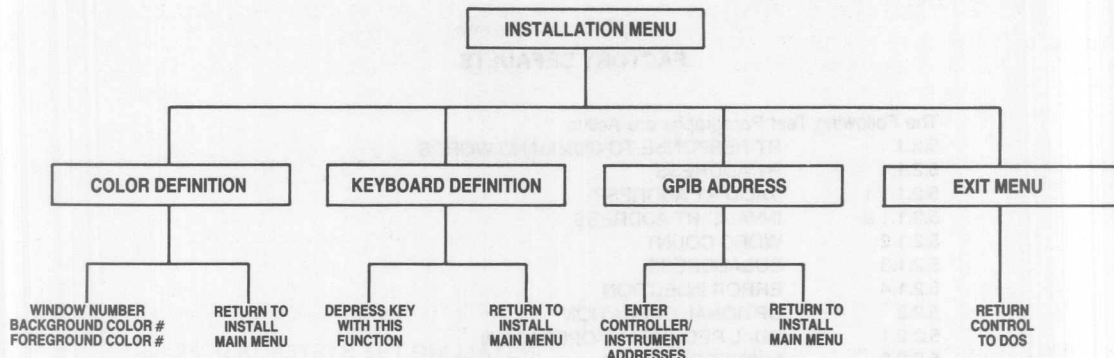


FIGURE 5. INSTALLATION MENU (INS69005 PROGRAM)

TABLE 9. BUS-69005 WINDOWS

Window Name	Definition	Associated Menu/Selection	Evoking Window
Top	ILC Data Device Corp.	All Menus	All screens
Main	Menus, Colors, Options	All Menus	Auto as necessary
Bottom	Prompts, Instructions	All Menus	Auto as necessary
File Transfer	Filename entry	SETUP/Save, Load	Initiate transfer
Manual Operation	Status condition setup	EDIT/Intervention	Select MANUAL
Bus Activity	1553 data-transfer monitor	EXECUTION/Run...	F1-key when available
IEEE-488 Error	GPIB failure reporting	EXECUTION/Run...	Auto as necessary
HELP/Paragraphs	PTP paragraphs displayed	EDIT/Activate Test	F1-key when available

### GPIB DEFINITION

This option allows the user to specify the I/O port address, DMA channel and timeout value for the GPIB-PC2A Controller card as well as the GPIB address of the National Instruments GPIB-PC2A Controller card and the BUS-68005 and BUS-68015 instruments.

Following the "PC-2A I/O PORT ADDRESS" prompt, enter the Base I/O address of the GPIB-PC2A within the PC in decimal (i.e., 02E1 hex = 737 decimal).

Following the "PC-2A ADDRESS OF GPIB", enter the GPIB address of the Controller card (0 to 32).

Following the "PC-2A DMA CHANNEL" prompt, enter the value to agree with the value of the card, as configured by the jumpers.

Following the "PC-2A TIMEOUT" prompt, enter the timeout value, in ms (10,000 is the suggested value).

Finally, enter the address of the BUS-68005 and BUS-68015 (if used). The default values for the PC-2A port address, DMA channel, and timeout are 737 (02E1 HEX), 1 and 10,000, respec-

tively. The default GPIB address for the controller card, BUS-68005, and BUS-68015 are 0, 1, and 2, respectively.

### EXITING THE INS69005 PROGRAM

When selected, INS69005 program is exited and the computer returned to DOS control.

Once the hardware has been connected as described in the TEST EQUIPMENT CONNECTION paragraph, the boot-up procedures of the IBM PC/XT/AT OR COMPATIBLE SETUP paragraph have been followed, and the INS69005 program has been run, the BUS-69005.COM program can now be installed.

Load the BUS-69005 operating environment by placing the BUS-69005 SYSTEM disk in the default drive and typing "BUS69005". Note that all files on the original BUS-69005 diskette must be present during loading. The BUS-69005 operating environment is loaded along with the RTU Unit-Under-Test (UUT) and RTU Protocol Production-Test-Plan (PTP) configurations contained in the [DEFAULT. ] setup-file.



## FACTORY DEFAULTS

The Following Test Paragraphs are Active

5.2.1	RT RESPONSE TO COMMAND WORDS
5.2.1.1	RT ADDRESS
5.2.1.1.1	VALID RT ADDRESS
5.2.1.1.2	INVALID RT ADDRESS
5.2.1.2	WORD COUNT
5.2.1.3	SUBADDRESS
5.2.1.4	ERROR INJECTION
5.2.2	OPTIONAL OPERATION
5.2.2.1	DUAL REDUNDANT OPERATION
5.2.2.2	MODE COMMANDS
5.2.2.2.1	DYNAMIC BUS CONTROL
5.2.2.2.2	SYNCHRONIZE
5.2.2.2.2.1	SYNCHRONIZE (WITHOUT DATA WORD)
5.2.2.2.2.2	SYNCHRONIZE (WITH DATA WORD)
5.2.2.2.3	TRANSMIT STATUS
5.2.2.2.4	INITIATE SELF TEST
5.2.2.2.5	TRANSMIT BIT WORD
5.2.2.2.6	TRANSMITTER SHUTDOWN AND OVERRIDE
5.2.2.2.6.1	DUAL REDUNDANT SHUTDOWN AND OVERRIDES
5.2.2.2.6.2	SELECTIVE SHUTDOWN AND OVERRIDES
5.2.2.2.7	TERMINAL FLAG BIT INHIBIT AND OVERRIDE
5.2.2.2.8	RESET REMOTE TERMINAL
5.2.2.2.9	TRANSMIT VECTOR WORD
5.2.2.2.10	TRANSMIT LAST COMMAND
5.2.2.3	STATUS WORD
5.2.2.3.1	SERVICE REQUEST
5.2.2.3.2	BROADCAST
5.2.2.3.3	BUSY
5.2.2.3.4	SUBSYSTEM FLAG
5.2.2.3.5	TERMINAL FLAG
5.2.2.4	BROADCAST MESSAGES
5.2.2.4.1	RESPONSE TO BROADCAST MESSAGES
5.2.2.4.1.1	BC TO RT BROADCAST COMMANDS
5.2.2.4.1.2	BROADCAST MODE COMMANDS
5.2.2.4.1.2.1	BROADCAST SYNCHRONIZE (WITHOUT DATA WORD)
5.2.2.4.1.2.2	BROADCAST SYNCHRONIZE (WITH DATA WORD)
5.2.2.4.1.2.3	BROADCAST INITIATE SELF TEST
5.2.2.4.1.2.4	BROADCAST TRANSMITTER SHUTDOWN AND OVERRIDES
5.2.2.4.1.2.4.1	BROADCAST DUAL REDUNDANT SHUTDOWN AND OVERRIDES
5.2.2.4.1.2.4.2	BROADCAST SELECTIVE BUS SHUTDOWN AND OVERRIDES
5.2.2.4.1.2.5	BROADCAST TERMINAL FLAG BIT INHIBIT AND OVERRIDE
5.2.2.4.1.2.6	BROADCAST RESET REMOTE TERMINAL
5.2.2.4.1.3	RT TO RT BROADCAST COMMANDS
5.2.2.5	RT TO RT TRANSFERS
5.2.2.5.1	RT TO RT TRANSMIT
5.2.2.5.2	RT TO RT RECEIVE
5.2.2.5.3	RT TO RT TIMEOUT
5.2.2.6	ILLEGAL COMMANDS
5.2.2.6A	ILLEGAL TX + RX
5.2.2.6B	ILLEGAL INVALID
5.2.2.6C	ILLEGAL MODE CODE

The Following Test Paragraphs are Inactive

\*\*\*\* NO INACTIVE TEST PARAGRAPHS \*\*\*\*

## FACTORY DEFAULTS (Configuration Printout Example)

### General UUT Capabilities

RT ADDRESS	1
VARIABLE ADDRESS CAPABILITY	N
TRANSMIT CAPABILITY	Y
TRANSMIT SA	30
TRANSMIT WC	32
RECEIVE CAPABILITY	Y
RECEIVE SA	30
RECEIVE WC	32
TEST BUS A	Yes
TEST BUS B	Yes
SIMULATED RT ADDRESS	30
SELECTED BUS SHUTDOWN DATA (A)	1
SELECTED BUS SHUTDOWN DATA (B)	0
DYNAMIC BUS CONTROL:	3 Both

### Test Configuration

EXECUTION LOG:	0
HALT ON ERROR:	NO
REPEAT TEST:	NO
IEEE-488 Debug:	NO
USER/AUTOMATIC CONTROL BITS	User
CONTROL BITS DELAY	0
AMPLITUDE BUS-68005 BUS A	87
AMPLITUDE BUS-68005 BUS B	87
AMPLITUDE 68015	117

### SUB ADDRESS TEST – TRANSMIT COMMANDS

SA 01 WC 20	SA 09 WC 20	SA 11 WC 20	SA 19 WC 20
SA 02 WC 20	SA 0A WC 20	SA 12 WC 20	SA 1A WC 20
SA 03 WC 20	SA 0B WC 20	SA 13 WC 20	SA 1B WC 20
SA 04 WC 20	SA 0C WC 20	SA 14 WC 20	SA 1C WC 20
SA 05 WC 20	SA 0D WC 20	SA 15 WC 20	SA 1D WC 20
SA 06 WC 20	SA 0E WC 20	SA 16 WC 20	SA 1E WC 20
SA 07 WC 20	SA 0F WC 20	SA 17 WC 20	
SA 08 WC 20	SA 10 WC 20	SA 18 WC 20	

### SUB ADDRESS TEST – RECEIVE COMMANDS

SA 01 WC 20	SA 09 WC 20	SA 11 WC 20	SA 19 WC 20
SA 02 WC 20	SA 0A WC 20	SA 12 WC 20	SA 1A WC 20
SA 03 WC 20	SA 0B WC 20	SA 13 WC 20	SA 1B WC 20
SA 04 WC 20	SA 0C WC 20	SA 14 WC 20	SA 1C WC 20
SA 05 WC 20	SA 0D WC 20	SA 15 WC 20	SA 1D WC 20
SA 06 WC 20	SA 0E WC 20	SA 16 WC 20	SA 1E WC 20
SA 07 WC 20	SA 0F WC 20	SA 17 WC 20	
SA 08 WC 20	SA 10 WC 20	SA 18 WC 20	

### WORD COUNT TEST – TRANSMIT COMMANDS

WC 01 SA 1E	WC 09 SA 1E	WC 11 SA 1E	WC 19 SA 1E
WC 02 SA 1E	WC 0A SA 1E	WC 12 SA 1E	WC 1A SA 1E
WC 03 SA 1E	WC 0B SA 1E	WC 13 SA 1E	WC 1B SA 1E
WC 04 SA 1E	WC 0C SA 1E	WC 14 SA 1E	WC 1C SA 1E
WC 05 SA 1E	WC 0D SA 1E	WC 15 SA 1E	WC 1D SA 1E
WC 06 SA 1E	WC 0E SA 1E	WC 16 SA 1E	WC 1E SA 1E
WC 07 SA 1E	WC 0F SA 1E	WC 17 SA 1E	WC 1F SA 1E
WC 08 SA 1E	WC 10 SA 1E	WC 18 SA 1E	WC 20 SA 1E

### WORD COUNT TEST – RECEIVE COMMANDS

WC 01 SA 1E	WC 09 SA 1E	WC 11 SA 1E	WC 19 SA 1E
WC 02 SA 1E	WC 0A SA 1E	WC 12 SA 1E	WC 1A SA 1E
WC 03 SA 1E	WC 0B SA 1E	WC 13 SA 1E	WC 1B SA 1E
WC 04 SA 1E	WC 0C SA 1E	WC 14 SA 1E	WC 1C SA 1E
WC 05 SA 1E	WC 0D SA 1E	WC 15 SA 1E	WC 1D SA 1E
WC 06 SA 1E	WC 0E SA 1E	WC 16 SA 1E	WC 1E SA 1E
WC 07 SA 1E	WC 0F SA 1E	WC 17 SA 1E	WC 1F SA 1E
WC 08 SA 1E	WC 10 SA 1E	WC 18 SA 1E	WC 20 SA 1E

**FACTORY DEFAULTS (Configuration Printout Example)**

**ILLEGAL TRANSMIT COMMANDS**

Word Count  
00000000000000001111111111111112  
SA 123456789ABCDEF0123456789ABCDEF0  
01 \*\*\*\*\*  
02 \*\*\*\*\*  
03 \*\*\*\*\*  
04 \*\*\*\*\*  
05 \*\*\*\*\*  
06 \*\*\*\*\*  
07 \*\*\*\*\*  
08 \*\*\*\*\*  
09 \*\*\*\*\*  
0A \*\*\*\*\*  
0B \*\*\*\*\*  
0C \*\*\*\*\*  
0D \*\*\*\*\*  
0E \*\*\*\*\*  
0F \*\*\*\*\*

**ILLEGAL RECEIVE COMMANDS**

Word Count  
00000000000000001111111111111112  
SA 123456789ABCDEF0123456789ABCDEF0  
01 \*\*\*\*\*  
02 \*\*\*\*\*  
03 \*\*\*\*\*  
04 \*\*\*\*\*  
05 \*\*\*\*\*  
06 \*\*\*\*\*  
07 \*\*\*\*\*  
08 \*\*\*\*\*  
09 \*\*\*\*\*  
0A \*\*\*\*\*  
0B \*\*\*\*\*  
0C \*\*\*\*\*  
0D \*\*\*\*\*  
0E \*\*\*\*\*  
0F \*\*\*\*\*

**ILLEGAL MODE CODES**

RX Mode Codes  
00000000000000001111111111111112  
SA 123456789ABCDEF0123456789ABCDEF0  
00 - - - - - \* . . . . . -  
1F - - - - - \* . . . . . -

**Word Count**

00000000000000001111111111111112  
SA 123456789ABCDEF0123456789ABCDEF0  
11 \*\*\*\*\*  
12 \*\*\*\*\*  
13 \*\*\*\*\*  
14 \*\*\*\*\*  
15 \*\*\*\*\*  
16 \*\*\*\*\*  
17 \*\*\*\*\*  
18 \*\*\*\*\*  
19 \*\*\*\*\*  
1A \*\*\*\*\*  
1B \*\*\*\*\*  
1C \*\*\*\*\*  
1D \*\*\*\*\*  
1E \*\*\*\*\*  
1F \*\*\*\*\*

**Word Count**

00000000000000001111111111111112  
SA 123456789ABCDEF0123456789ABCDEF0  
11 \*\*\*\*\*  
12 \*\*\*\*\*  
13 \*\*\*\*\*  
14 \*\*\*\*\*  
15 \*\*\*\*\*  
16 \*\*\*\*\*  
17 \*\*\*\*\*  
18 \*\*\*\*\*  
19 \*\*\*\*\*  
1A \*\*\*\*\*  
1B \*\*\*\*\*  
1C \*\*\*\*\*  
1D \*\*\*\*\*  
1E \*\*\*\*\*  
1F \*\*\*\*\*

**TX Mode Codes**

00000000000000001111111111111112  
SA 123456789ABCDEF0123456789ABCDEF0  
00 \*\*\*\*\* . . . . . \* . . . . . \*  
1F \*\*\*\*\* . . . . . \* . . . . . \*

\* = CLEAR STATUS  
- = NO RESPONSES  
. = STATUS WORD WITH MESSAGE ERROR BIT SET

## PRINT EXECUTION LOG (Example)

Examples of the different formats of the Print Execution Log are shown below.

FORMAT 0. Do NOT print execution log  
FORMAT 1. Print BRIEF Log

FORMAT 2. Print EXPANDED ERROR Log  
FORMAT 3. Print EXPANDED COMPLETE Log

### FORMAT 1 Print BRIEF LOG

#### BRIEF LOG (NO ERRORS)

15:54:53  
Time<sup>1</sup>

5.2.1.1  
Paragraph  
Number

**VALID RTU ADDRESS**  
Test Paragraph  
Name

#### BRIEF LOG (ERRORS)

15:55:02  
Time<sup>1</sup>

5.2.1.2  
Paragraph  
Number

**WORD COUNT**  
Test Paragraph  
Name

**Init Block 01**  
Block  
Number

**RTU:01**  
RTU  
Address

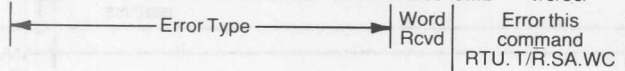
**TR:0**  
T/R  
bit

**SAE:1**  
Subaddress

**WC:01**  
Word Count

**EXPECTED: CS**  
Data Expected

**ERROR - INCORRECT STATUS WORD 0C00 CMD = 1/0/30/**



### FORMAT 2 Print EXPANDED ERROR LOG

#### EXPANDED ERROR LOG (NO ERRORS)

15:54:53  
Time<sup>1</sup>

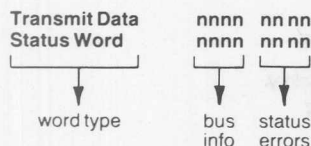
5.2.1.1  
Paragraph  
Number

**VALID RTU ADDRESS**  
Test Paragraph  
Name

### FORMAT 3 EXPANDED ERROR LOG (ERRORS) and EXPANDED COMPLETE LOG (WITH AND WITHOUT ERRORS)

#### Message Block 1

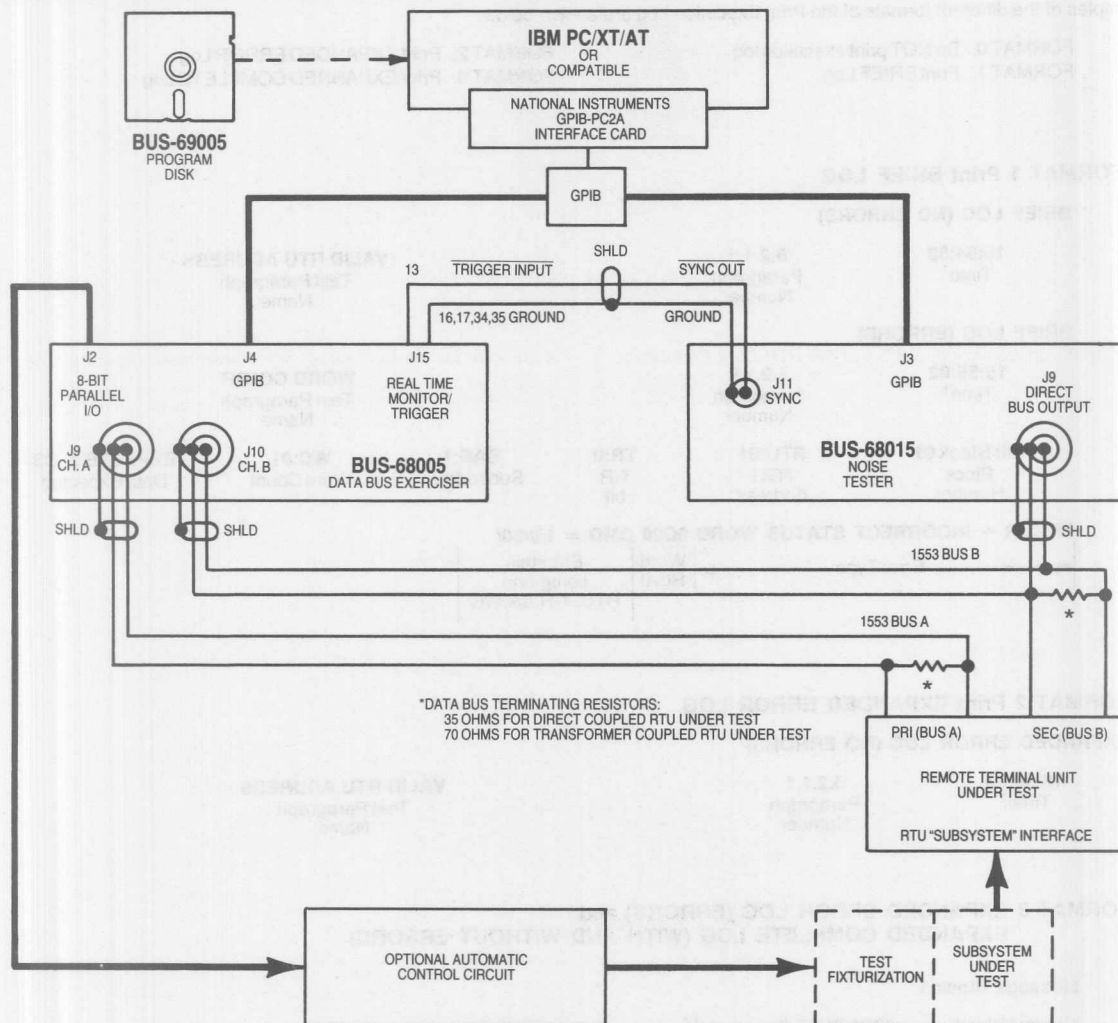
Control Word 02 00 FF FF (Hex code)<sup>2</sup>  
Command Word 0BC1 00 80  
Transmit Data 0000 00 80



#### Notes:

1. Start time of test or "SKIPPED" indicating that test is inactive. Each printout with all tests passed will be of same length.
2. Consult BUS-68005 Manual for definitions of hex codes.

## BUS-69005 OPERATING ENVIRONMENT INSTALLATION



**FIGURE 6. BUS-69005 OPERATING ENVIRONMENT ELECTRICAL SET-UP**

### ORDERING INFORMATION

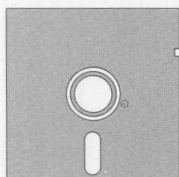
BUS-69005 MIL-STD-1553 PROTOCOL SOFTWARE

To obtain data sheets on the following products, consult factory.

BUS-68005 MIL-STD-1553 DATA BUS EXERCISER

BUS-68015 MIL-STD-1553 NOISE TESTER





## MIL-STD-1553 PROTOCOL SOFTWARE

PERFORMS BUS SWITCHING  
TEST WITH TWO BUS-68005s

### DESCRIPTION

The BUS-69006 MIL-STD-1553 Protocol Test software provides a menu-driven Automatic Test Equipment (ATE) environment using an IBM PC/XT/AT host along with two of DDC's BUS-68005 Data Bus Exercisers to perform all protocol tests specified in the SAE RTU Production Test Plan (Section 5.2).

The BUS-69006 Production Test Plan Software operates the same as the BUS-69005 Software with the following exception:

*In order to run Paragraph 5.2.2.1 of the PTP Dual Redundant Operation (or Bus Switching Test), a second BUS-68005 Data Bus Exerciser is used (instead of a BUS-68015 Noise Tester) in conjunction with the primary BUS-68005. It is necessary to*

*have two (2) BUS-68005s installed on the GPIB bus in order to run the BUS-69006 software.*

The second BUS-68005 is referred to as BUS-68005 #2. The BUS-68005 #2's GPIB Address factory default is 2 and may be changed with the INS69006 (installation) program. The factory default of the National Instruments GPIB-PC2A Card and BUS-68005 #1 remain 0 and 1, respectively.

In the TEST CONFIGURATION menu for the BUS-69006, there is an entry for the BUS-68005 #2 Transmitter Amplitude. The factory default is 87, the same as BUS-68005 #1 CH A and CH B. This provides approximately 3.0 Vpp across 35 Ohms as required by the PTP for direct coupled RTUs.

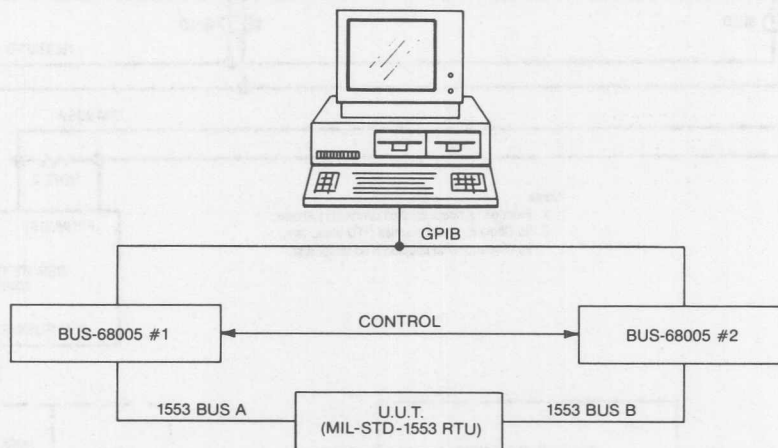


FIGURE 1. BUS-69006 OPERATING ENVIRONMENT

### BUS-69006 OPERATING ENVIRONMENT INSTALLATION

Figure 2 illustrates the full electrical set-up required to use the BUS-69006 operating environment. Table 1 lists the cable connectors required.

The BUS-69006 set-up is similar to the BUS-69005 with the following exceptions:

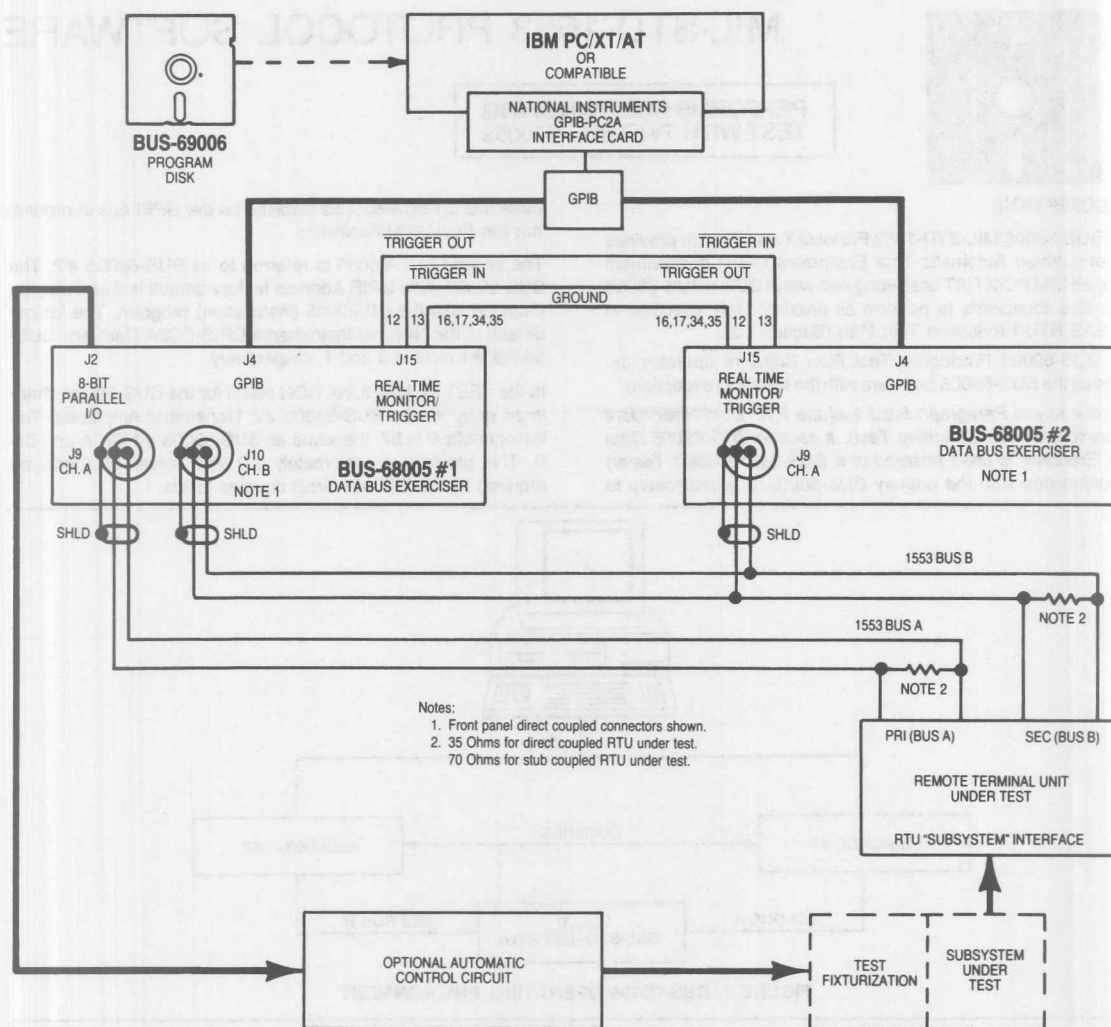
1. The BUS-68005 Data Bus Exerciser is designated BUS-68005 #1 and the BUS-68005 (which replaces the BUS-68015) is designated BUS-68005 #2.
2. Connection to the optional automatic control circuit for control of RTU Address and Status Word bits is from the Parallel I/O port connector J2 of BUS-68005 #1, not BUS-68005 #2.
3. 1553 Bus A connects from J9 (CH A) of BUS-68005 #1 to BUS A input of the RTU under test. 1553 Bus B connects

TABLE 1. BUS-69006 SUGGESTED MATING CONNECTORS

BUS-68005	CONNECTOR
J2 (PARALLEL I/O)	TRW DB25S (DB25 FEMALE)
J15 (TRIGGER INPUT)	AMPHENOL 17-10500-1-390 50-PIN FEMALE
J9, J10 (CH A, CH B)	TROMPETER PL75-47 TRIAX MALE
CABLE, TRIAX	TROMPETER 14949

from J10 (CH B) of BUS-68005 #1 to J9 (CH A) of BUS-68005 #2, and to the BUS B input of the RTU under test.

4. As shown in figure 1, a cable is required to connect between the two Real Time Monitor/Trigger I/O connectors (J15) of the two instruments. Note that TRIGGER OUTPUT (J15-12) from each BUS-68005 is connected to TRIGGER INPUT (J15-13) on the alternate instrument.



**FIGURE 2. BUS-69006 OPERATING ENVIRONMENT ELECTRICAL SET-UP**

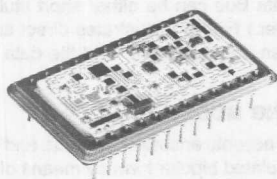
## ORDERING INFORMATION

## BUS-69006 MIL-STD-1553 PROTOCOL SOFTWARE

To obtain data sheets on the following products, consult factory.

BUS-68005 MIL-STD-1553 DATA BUS EXERCISER

BUS-69005 MIL-STD-1553 PROTOCOL SOFTWARE



## MIL-STD-1553 TRANSCEIVER

### FEATURES

- MEETS ALL MIL-STD-1553A AND 1553B REQUIREMENTS
- VERY LOW POWER DISSIPATION
- IMPROVED FILTERING ON RECEIVER TO ENHANCE BIT ERROR RATE OF SYSTEM
- $\pm 15V$  OR  $+15V$  AND  $-12V$  POWER SUPPLY VOLTAGES
- SCREENED TO MIL-STD-883
- HARRIS 15530 ENCODER/DECODER DIRECT INTERFACE COMPATIBILITY

### DESCRIPTION

The BUS-8553 Transceiver is a complete transmitter and receiver conforming fully to MIL-STD-1553A and 1553B. Features of this high reliability transceiver include: Harris 15530 type Encoder/Decoder direct interface capability,  $\pm 15V$  or  $+15V$  and  $-12V$  power supply voltage requirements, and an internal (factory pre-set) threshold level.

Figure 1 illustrates a block diagram of the BUS-8553 Transceiver. The receiver section accepts phase-modulated bipolar data from a MIL-STD-1553 Data Bus and produces TTL signal data at its outputs: RX Data Out and RX Data In. These outputs represent positive and negative excursions of the input Bus signals beyond a preset threshold level. The receiver can be taken off-line (outputs disabled) by the

application of a logic "0" to the STROBE input.

The transmitter section accepts bipolar TTL signal data at its TX Data and TX Data input lines and produces a 28Vpp differential signal across a 140 Ohm load that's coupled to the TX Data and TX Data outputs via transformer. An external input, INHIBIT, takes priority over the transmitter inputs and disables the transmitter when activated with a logic "1".

The BUS-8553 Transceiver is packaged in a 24 pin DDIP, measuring 1.4 x 0.8 x 0.2 inches. Its small size, low power dissipation, and direct interface compatibility with Harris 15530 type Encoder/Decoder make it an excellent choice for any MIL-STD-1553A or 1553B Transceiver application.

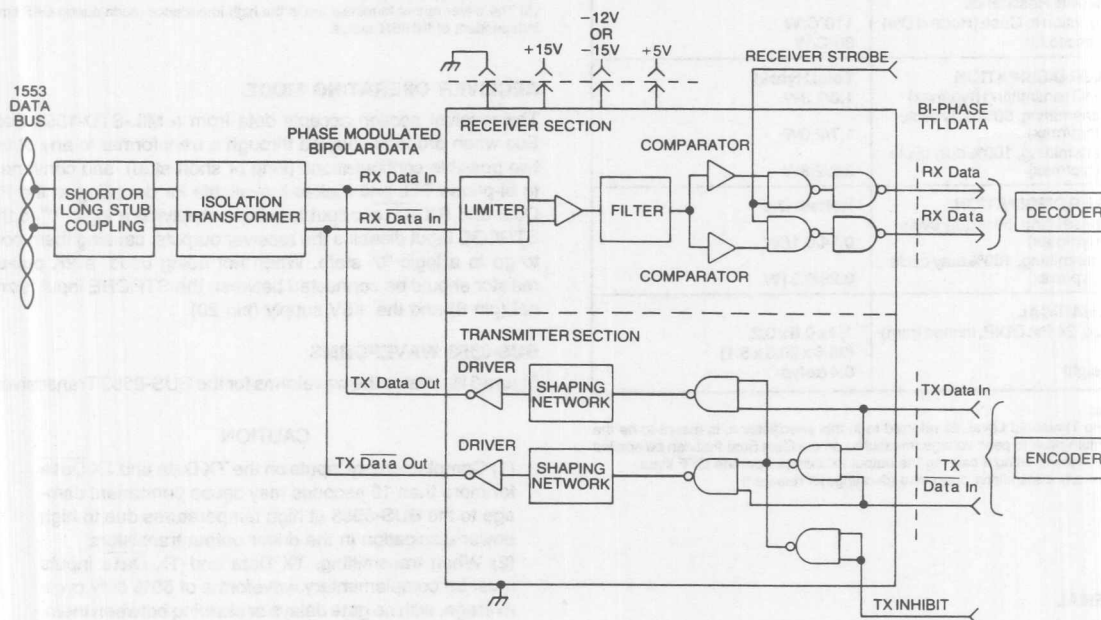


FIGURE 1. BUS-8553 BLOCK DIAGRAM

PARAMETER	VALUE
<b>RECEIVER</b> Input Level Internal Threshold <sup>(1)</sup> CMRR Input Resistance, differential Input Capacitance, differential	40Vpp, differential, max 0.56Vpp min, 1Vpp max 40 db, min 7K Ohm, min 5pf, max
<b>DRIVER</b> Output Level Rise/Fall Time Output Noise Output Offset  Output Impedance (Non-Transmitting) Output Resistance, differential Output Capacitance, differential	28Vpp, nominal, across 140 Ohm load 130ns, typical 10mVpp, differential, max ±90mVpp, max differential across 35Ω load  10K Ohm, min 5pf, max
<b>LOGIC; TTL/CMOS Compatible</b> Receiver Strobe Input All Logic Outputs (Receiver) Transmitter Inhibit Input Transmitter TX Data and TX Data Inputs	2 LSTTL loads, max 10 LSTTL loads, min 1 TTL load, max  2 TTL loads, max
<b>POWER SUPPLY REQMTS</b>  Non-Transmitting (typ/max) Transmitting, 50% duty cycle (typ/max) Transmitting, 100% duty cycle (typ/max)	+5V±10% +15V±5% -15V±5%  40/50mA 30/40mA 25/30mA 40/50mA 110/130mA 25/30mA 40/50mA 200/220mA 25/30mA
<b>THERMAL</b> Operating Junction Temp. <sup>(2)</sup> Operating Case Temperature <sup>(2)</sup> Storage Temperature Thermal Resistance Junction to Case (Hottest Die) Case to Air	-55°C to 160°C -55°C to 125°C -65°C to 150°C  110°C/W 30°C/W
<b>POWER DISSIPATION</b> Non-Transmitting (typ/max) Transmitting, 50% duty cycle (typ/max) Transmitting, 100% duty cycle (typ/max)	<b>Total Hybrid</b> 1.0/1.3W  1.7/2.0W 2.3/2.8W
<b>POWER DISSIPATION</b> Transmitting, 50% duty cycle (typ/max) Transmitting, 100% duty cycle (typ/max)	<b>Hottest Die</b>  0.14/0.16W 0.28/0.31W
<b>MECHANICAL</b> Size, 24 Pin DDIP, inches (mm)  Weight	1.4 x 0.8 x 0.2 (35.6 x 20.3 x 5.1) 0.4 oz typ

**Notes:**

- (1) The Threshold Level, as referred to in this specification, is meant to be the maximum peak to peak voltage (measured on the Data Bus) that can be applied to the receiver without causing the output to change from the OFF state.  
(2) For any transmitting duty cycle (derating not required).

## GENERAL

Figure 1 illustrates a BUS-8553 Transceiver with connections to a MIL-STD-1553 data bus. Once transformer isolated, coupling

or long stub (transformer.) Figure 2 illustrates direct and transformer coupling between the transceiver and the data bus.

## TRANSMIT OPERATING MODE

The transmitter section accepts encoded TTL data and converts this data to phase-modulated bipolar form by means of a wave-shaping network and driver circuitry. These driver outputs are coupled to a MIL-STD-1553 Data Bus by means of a transformer. These output terminals can be put into a high impedance state when transmitting by enabling the INHIBIT, or by placing both inputs at the same logic level. Table 2 is the truth table for the transmitter operating mode.

The transceiver's transmitter is able to operate in a "wraparound" mode; this allows output data to be monitored by the receiver section and returned to the decoder where it can be checked for errors.

TABLE 2. TRANSMITTER OPERATING MODE			
TX Data In	TX Data In	TX INHIBIT	DRIVER OUTPUT <sup>(1)</sup>
X <sup>(2)</sup>	X	H	OFF
0	0	X	OFF
0	1	L	ON <sup>(3)</sup>
1	0	L	ON
1	1	X	OFF <sup>(4)(5)</sup>

**Notes:**

- (1) Driver Out = TX Data Out and TXData Out.  
(2) X = don't care.  
(3) ON = low impedance.  
(4) OFF = high impedance.  
(5) The driver output terminals are in the high impedance mode during OFF time, independent of INHIBIT status.

## RECEIVER OPERATING MODE

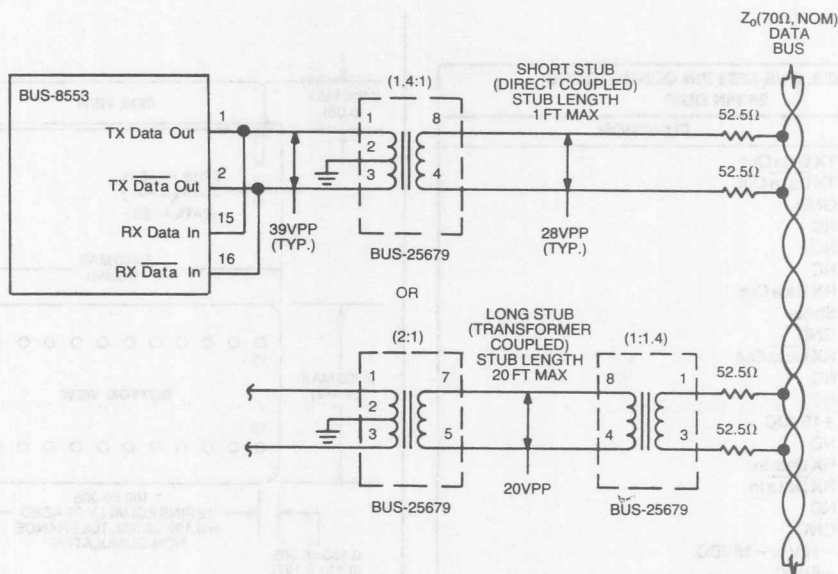
The receiver section accepts data from a MIL-STD-1553 Data Bus when properly coupled through a transformer in any of the two possible configurations (long or short stub), and converts it to bi-phase TTL and makes it available for decoding at the RX Data and RX Data output terminals. Applying a logic "0" to the STROBE input disables the receiver outputs, causing them both to go to a logic "0" state. When not being used, a 2K pull-up resistor should be connected between the STROBE input terminal (pin 8) and the +5V supply (pin 20).

## BUS-8553 WAVEFORMS

Figure 3 illustrates the waveforms for the BUS-8553 Transceiver.

## CAUTION

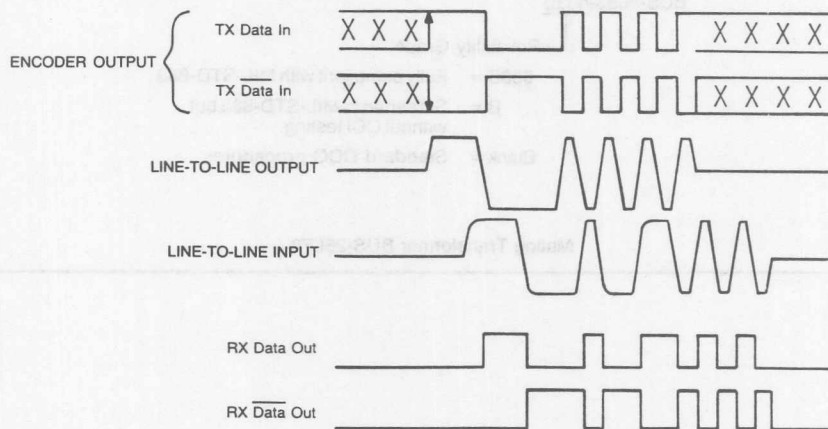
- (1) Complementary inputs on the TX Data and TX Data for more than 10 seconds may cause permanent damage to the BUS-8553 at high temperatures due to high power dissipation in the driver output transistors.  
(2) When transmitting, TX Data and TX Data inputs must be complementary waveforms of 50% duty cycle average, with no gate delays or skewing between them. It is recommended that the inputs be driven with a properly gated "D-type" flip-flop.



**Notes:**

- (1) Only one connection can be made from the Transceiver to the MIL-STD-1553 Data Bus, either short or long stub, but not both.
- (2) Value of isolation resistors are 52.5Ω (0.75Z<sub>0</sub>).
- (3) Bus must be terminated with its characteristic impedance at both ends.

**FIGURE 2. TRANSCEIVER TO DATA BUS COUPLING CONNECTIONS**



**Notes:**

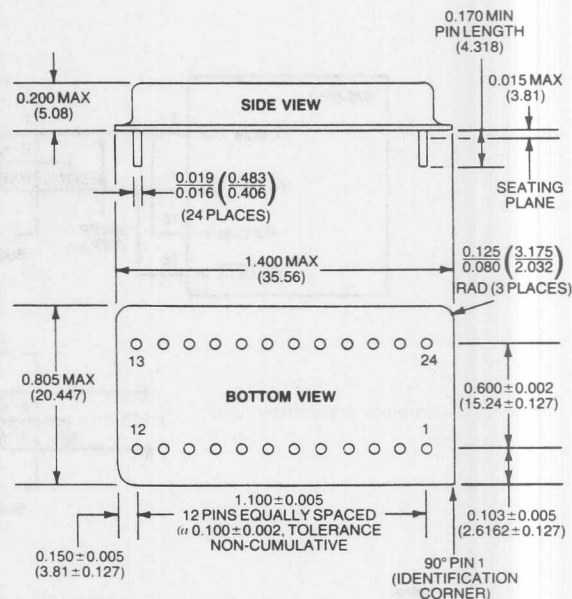
- (1) TX Data In and RX Data Out are TTL signals.
- (2) TX Data In lines must be at opposite logic levels during transmission, and at the same logic level when not transmitting.
- (3) LINE-TO-LINE output voltage is measured between TX Data and TX Data Out.
- (4) LINE-TO-LINE input voltage is measured on the Data Bus.
- (5) RX Data outputs are OFF when in the LOW state.
- (6) The BUS-8553 can be interfaced to Smiths type Encoder/Decoder by switching the RX Data and RX Data output lines and inverting their signal with external inverting gates.

**FIGURE 3. BUS-8553 WAVEFORMS**



**TABLE 3. BUS-8553 PIN CONNECTIONS  
24 PIN DDIP**

PIN	FUNCTION
1	TX Data Out
2	TX Data Out
3	GND
4	NC
5	NC
6	NC
7	RX Data Out
8	Strobe
9	GND
10	RX Data Out
11	NC
12	NC
13	+15VDC
14	NC
15	RX Data In
16	RX Data In
17	NC
18	GND
19	-12V or -15VDC
20	+5VDC
21	TX Inhibit
22	TX Data In
23	TX Data In
24	NC



- Notes:
- (1) Dimensions are in inches (millimeters).
  - (2) Lead identification numbers are for reference only.
  - (3) Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
  - (4) Pin material meets solderability requirements of MIL-STD-202E, Method 208C.

**FIGURE 4. MECHANICAL OUTLINE 24 PIN DDIP**

## ORDERING INFORMATION

**BUS-8553-883B**

Reliability Grade:

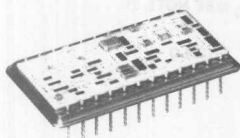
883B = Fully compliant with MIL-STD-883

B = Screened to MIL-STD-883 but without QCI testing.

Blank = Standard DDC procedures.

Mating Transformer BUS-25679

## VARIABLE OUTPUT MIL-STD-1553 TRANSCEIVER



### DESCRIPTION AND APPLICATIONS

Designed specifically for use in automatic test equipment when a variable transmitter output level is required, the DDC Model BUS-8559 Transceiver is a complete transmitter and receiver conforming to MIL standards 1553A and 1553B. The receiver section accepts phase-modulated bipolar data at the input and produces a bi-phase TTL signal at the output (Figure 1). The outputs, DATA and  $\overline{\text{DATA}}$ , represent positive and negative excursions of the input beyond an internally fixed threshold. These positive and negative thresholds are internally set at the factory for a nominal 1V p-p signal, measured at point "A", Figure 2. An external strobe input is provided to allow the removal of the receiver from the line. A logic "0" applied to "STROBE" will disable the receiver output.

The BUS-8559 transmitter section accepts bi-phase TTL data at the input and produces a 0 to 27 volt nominal

p-p differential signal across the  $145\Omega$  load, when measured at point "B", Figure 2. When coupled to the data bus with the specified transformer\*, isolated (on the data side) with two  $55.0\Omega$  fault isolation resistors, and loaded by two  $70\Omega$  terminations (plus additional receivers), the data bus signal produced is 0 to 7.5 volts nominal p-p measured at point "A" (Figure 2).

When both DATA and  $\overline{\text{DATA}}$  inputs are held low or high, the transmitter presents a high impedance to the line. An external inhibit input is provided to allow the removal of the transmitter output from the line (Figure 3). A logic "1" applied to the "INHIBIT" takes priority over the condition of the data inputs and disables the transmitter.

The transceiver is available in a 24 pin hybrid package measuring  $1.4 \times 0.8 \times 0.2$  inch, and can be used in any MIL-STD-1553 application which requires the use of a transceiver.

\*Transformer P/N BUS-25679. See Mechanicals.

### FEATURES

- VARIABLE TRANSMITTER OUTPUT
- TRANSMITTER/RECEIVER IN A SINGLE 24 PIN DDIP HYBRID
- VERY LOW POWER DISSIPATION
- MEETS MIL-STD-1553A AND 1553B
- IMPROVED FILTERING ON RECEIVER TO ENHANCE BIT ERROR RATE OF SYSTEM
- $\pm 15\text{V}$  OR  $+15$  AND  $-12\text{V}$  OPERATION

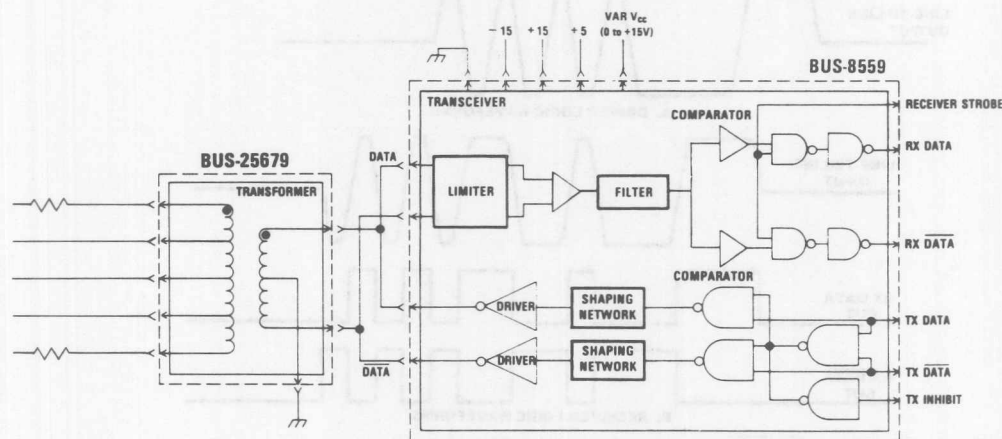
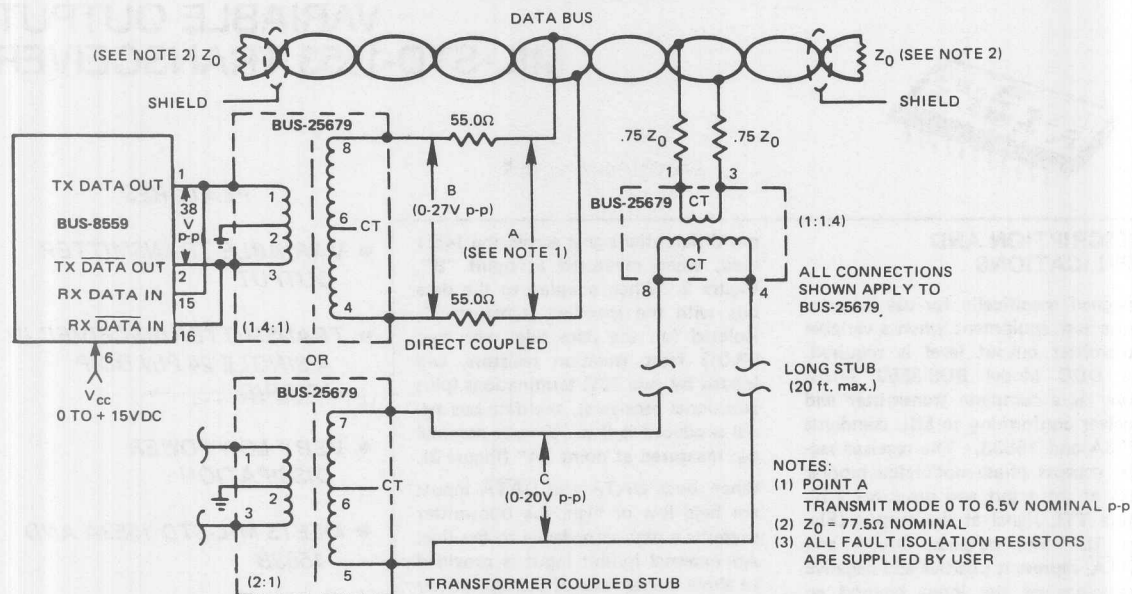
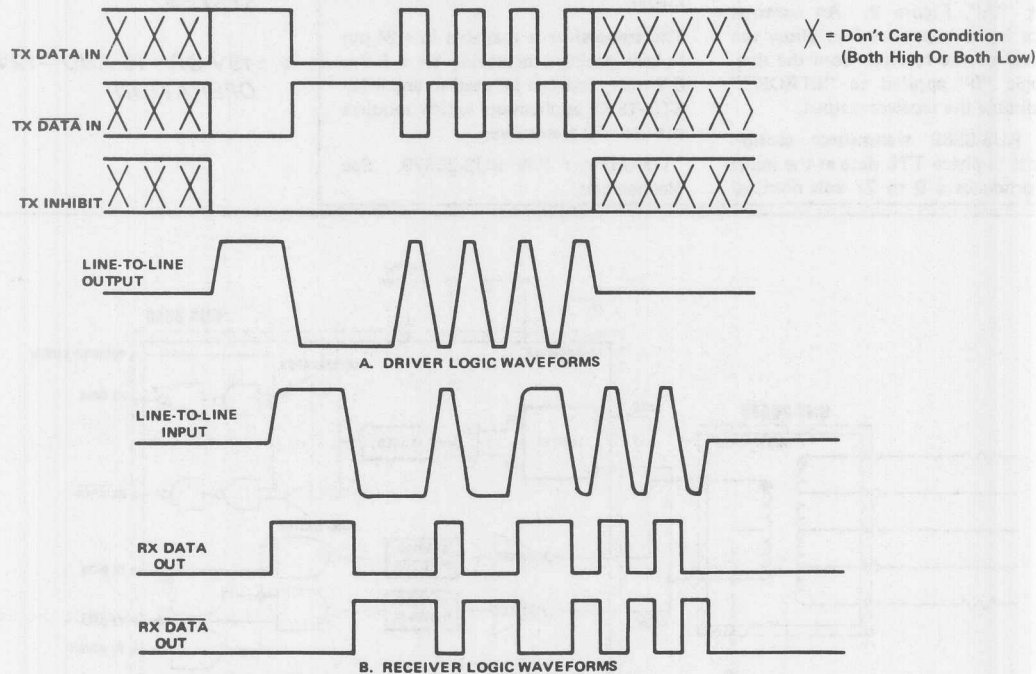


FIGURE 1. BLOCK DIAGRAM



CAUTION: Complementary inputs on TX and TX for more than 10 seconds may cause permanent damage at high temperatures due to high power dissipation by output drivers.



NOTE 1) RX DATA and RX DATA lines are low when BUS-8553 is not receiving.  
2) When BUS-8559 is used with Harris HD-15530, CMOS Manchester Encoder-Decoder no external logic is required.

FIGURE 3. LOGIC WAVEFORMS

## SPECIFICATIONS-TRANSFORMER AND BUS-8559 HYBRID

PARAMETER	VALUE																								
<b>RECEIVER</b>																									
Input Level	40V p-p differential max																								
Input Impedance	4 K $\Omega$ differential min																								
Threshold Level	1V p-p nominal, internally set (direct coupled mode)																								
Output Level	TTL, 10 LS Loads																								
Outputs:																									
V <sub>OL</sub>	0.6V max																								
V <sub>OH</sub>	2.5V min																								
I <sub>OL</sub>	4mA max																								
I <sub>OH</sub>	-400 $\mu$ A max																								
<b>TRANSMITTER</b>																									
Input Level	TTL, 2 LS Loads																								
Inputs:																									
V <sub>ih</sub>	2V min																								
V <sub>il</sub>	0.8V max																								
I <sub>ih</sub>	80 $\mu$ A max																								
I <sub>il</sub>	-3.2mA max																								
Output Level	0 to 27V p-p nominal across 145 $\Omega$ load 0 to 20V p-p nominal (measured at point C, Figure 2)																								
Rise/Fall Time	130 nsec typical																								
Output Noise	10mV p-p differential max																								
Variable V <sub>cc</sub>	0 to +15V DC																								
<b>GENERAL</b>																									
Power Supply Requirements	<table><tr><th>P.S.</th><th>STDBY</th><th>25%</th><th>100%</th></tr><tr><th>V</th><th>mA</th><th>mA</th><th>mA</th></tr><tr><td>+5</td><td>25 max</td><td>22 max</td><td>21 max</td></tr><tr><td>+15</td><td>30 max</td><td>30 max</td><td>30 max</td></tr><tr><td>-15</td><td>30 max</td><td>30 max</td><td>30 max</td></tr><tr><td>V<sub>cc</sub></td><td>0</td><td>70</td><td>180</td></tr></table>	P.S.	STDBY	25%	100%	V	mA	mA	mA	+5	25 max	22 max	21 max	+15	30 max	30 max	30 max	-15	30 max	30 max	30 max	V <sub>cc</sub>	0	70	180
P.S.	STDBY	25%	100%																						
V	mA	mA	mA																						
+5	25 max	22 max	21 max																						
+15	30 max	30 max	30 max																						
-15	30 max	30 max	30 max																						
V <sub>cc</sub>	0	70	180																						
Operating Temperature Range	-55°C to +125°C (case temp.)																								
Storage Temperature Range	-55°C to +135°C																								
Size (24pin DDIP hybrid)	1.4 x 0.8 x 0.2 inch (36 x 20 x 5mm)																								
Weight	0.4 oz typ (11g)																								

NOTES: (1) Will operate with  $\pm 12$ V P.S.

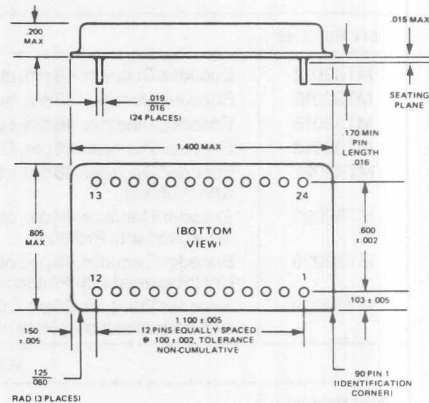
NOTES: (1) Will operate with  $\pm 12V$  P.S.

## BUS-8559 PIN CONNECTION TABLE

PIN	FUNCTION
1	TX Data Out
2	TX Data Out
3	GND
4	N.C.
5	N.C.
6	Variable V <sub>cc</sub>
7	RX Data Out
8	Strobe
9	GND
10	RX Data Out
11	N.C.
12	N.C.
13	+15V DC
14	N.C.
15	RX Data In
16	RX Data In
17	N.C.
18	GND
19	-15VDC
20	+5VDC
21	TX Inhibit
22	TX Data In
23	TX Data In
24	N.C.

## MECHANICAL OUTLINE

### 24 Pin Double DIP



#### NOTES

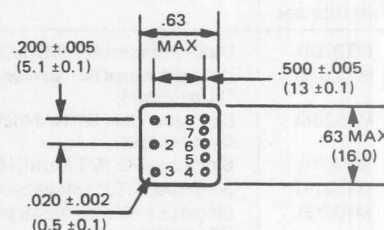
1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead cluster shall be centered within .010 of outline dimensions. Lead spacing dimensions apply only at seating plane
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

## MECHANICAL OUTLINE

### TRANSFORMER (P/N BUS-25679)



#### SIDE VIEW



#### BOTTOM VIEW

#### NOTES:

1. All dimensions are in inches (millimeters)
2. Pin callouts on bottom view are for reference only

## ORDERING INFORMATION

### BUS - 8559 - B

Reliability Grade:

B = Screened to MIL-STD-883 but without QCI testing.

Blank = Standard DDC procedures.

### TRANSFORMER: BUS-25679

NOTE: The transceiver and transformer must be ordered as separate parts.

DDC is a distributor of these components. Contact the factory for further information.

ENCODERS/DECODERS	
Part Number	Description
MT32012	Encoder/Decoder. 48 pin, quad redundant RT.
MT32016	Encoder/Decoder. 48 pin, quad redundant BC interface.
MT32018	Encoder/Decoder. 48 pin, quad redundant BC or RT interface.
MT32019	Encoder/Decoder. 56 pin, CC or 64 pin DIL, quad redundant BC or RT interface.
MT32022	Encoder/Decoder. 48 pin, quad redundant RT. Device will receive its own transmissions. Not to be used with Protocol.
MT32026	Encoder/Decoder. 48 pin, quad redundant BC interface. Device will receive its own transmissions. Not to be used with Protocol.
MT32028	Encoder/Decoder. 48 pin, quad redundant RT or BC interface. Device will receive its own transmissions. Not to be used with Protocol.
MT32029	Encoder/Decoder. 56 pin CC or 64 pin DIL, , quad redundant RT or BC interface. Device will receive its own transmissions. Not to be used with Protocol.
RTU PROTOCOL SEQUENCES	
Part Number	Description
MT32013	Protocol Sequencer. Optional FIFO. 40 pin, 16 bit x 32 word.
MT32014	Protocol Sequencer. 56 pin CC or 64 pin DIL, quad redundant.
MT32024	Protocol Sequencer. 48 pin dual redundant. No FIFO option.
MT32034	Protocol Sequencer. 48 pin, quad redundant. No Modecodes.
MT32044	Protocol Sequencer. 56 pin CC or 64 pin DIL, quad redundant. No modecodes.
MT32054	Protocol Sequencer. 56 pin CC or 64 pin DIL, with "No modecodes" option. Wrap around function not available.
MT32017	MT32014 and MT32013 in one 48 pin DIL package. Message Error, Terminal Flag, and Modecode Detect signals not available.
MT32047	MT32044 and MT32013 in one 48 pin DIL package. Message Error and Terminal Flag inputs not available.
MT32057	MT32054 and MT32013 in one 48 pin DIL package. Message Error, Terminal Flag, and Modecode Detect signals not available.
RTU COMBINATIONS	
Part Number	Description
MT32011	Dual redundant RT. (MT32018, MT32018, MT32013, and MT32014 in a standard 64 pin DIL package).
MT32041	Dual redundant RT. No Modecodes. (MT32018, MT32018, MT32013, and MT32044 in a standard 64 pin DIL package).
MT32051	Dual redundant RT. No Modecodes. (MT32018, MT32018, MT32013, and MT32054 in a standard 64 pin DIL package).
MT32111	Single bus RT. (MT32018, MT32013, and MT32014 in a standard 64 pin DIL package).
MT32141	Single bus RT. No Modecodes. (MT32018, MT32013, and MT32044 in a standard 64 pin DIL package).
MT32151	Single bus RT with "No Modecodes" option. (MT32018, MT32013, and MT32054 in a standard 64 pin DIL package).
MT32211	Dual redundant RT. No FIFO. (MT32018, MT32018, and MT32014 in a standard 64 pin DIL package).
MT32241	Dual redundant RT. No Modecodes. No FIFO. (MT32018, MT32018, and MT32044 in a standard 64 pin DIL package).
MT32251	Dual redundant RT with "No Modecodes" option. No FIFO. (MT32018, MT32018, and MT32054 in a standard 64 pin DIL package).
MT32311	Single bus RT. No FIFO. (MT32018 and MT32014 in a standard 64 pin package).
MT32341	Single bus RT. No Modecodes. No FIFO. (MT32018 and MT32044 in a standard 64 pin DIL package).
MT32351	Single bus RT with "No Modecodes" option. No FIFO. (MT32018 and MT32054 in a standard 64 pin DIL package).
BCU PROTOCOL SEQUENCERS	
Part Number	Description
MT32015	Protocol Sequencer. 56 pin CC or 64 pin DIL package.
MT32010	MT32015 and MT32013 in a 48 pin DIL package.

Note: For theory of operation of RTU chip set see BUS-65132 data sheet.

B



## VIII. APPLICATIONS INFORMATION

**APPLICATION NOTES  
CONTENTS**

<b>TITLE</b>	<b>PAGE</b>
Processor Interfaces To 1553 Buses .....	VIII-3
A Systems Approach To MIL-STD-1553 Terminal Design .....	VIII-8
Streamline Your MIL-STD-1553 Design By Eliminating The CPU .....	VIII-15
Factors to Consider When Using a PC in a MIL-STD-1553 Environment .....	VIII-26
Additional Application Notes Available from DDC .....	VIII-29

## PROCESSOR INTERFACES TO 1553 BUSES

When a design engineer addresses the task of implementing a MIL-STD-1553B interface he has available a number of "standard" components from which to select. In such situations, it is useful to have a "shopping list" of features that will ultimately ease the process of interface design. It is acknowledged that no two designers will necessarily have the same requirements due to particular system constraints. However, there are some commonly encountered questions which can be discussed in general terms.

What is the true board area required? Additional components necessary to fully implement an interface such as transceivers, interface logic, RAM etc, will take up quite large areas of pcbs. As a consequence

the board layout may become more complicated and more expensive to produce.

Is it possible to have a standard interface? In commercial terms, one card, which is able to provide all three 1553 functions of Bus Control, Remote Terminal and Monitor, is a desirable design goal. Commonality of components and pcbs assist the purchasing function and engineering and software development time can be minimised.

Is control of the device straightforward? This can affect the software overhead for the device. An intelligent interface requires minimal control. How good is the sub-system interface? A good interface can ease the design task to a very large extent. It should be compatible with a wide selection of microprocessors, minimise cpu intervention and offer maximum flexibility of use. Ideally, the sub-system interface should represent the 1553 terminal to the cpu in terms of other peripheral devices via an address bus, data bus and standard control signals for the transfer of data.

What about data integrity? Comprehensive built-in test features are necessary to ensure integrity of the terminal. Additionally, a means of ensuring that partially updated messages are not transferred to the 1553 bus or the sub-system, needs to be provided.

A number of different suppliers may be needed, therefore, to source the additional components which may be needed for complete implementation of the interface. Protocol chips need transceivers, devices with transceivers included usually require the addition of extra circuitry in order to interface with the sub-system.

One solution currently available, the BUS-61553 Aircraft Integrated Multiplex Hybrid (AIM-HY) is presented by its manufacturers as offering optimum integration, minimum size and a complete implementation of the standard. (Fig. 1).

Invariably a design will be constrained by size, weight and power consumption considerations. The device under examination here occupies a board area of just 4ins<sup>2</sup>.

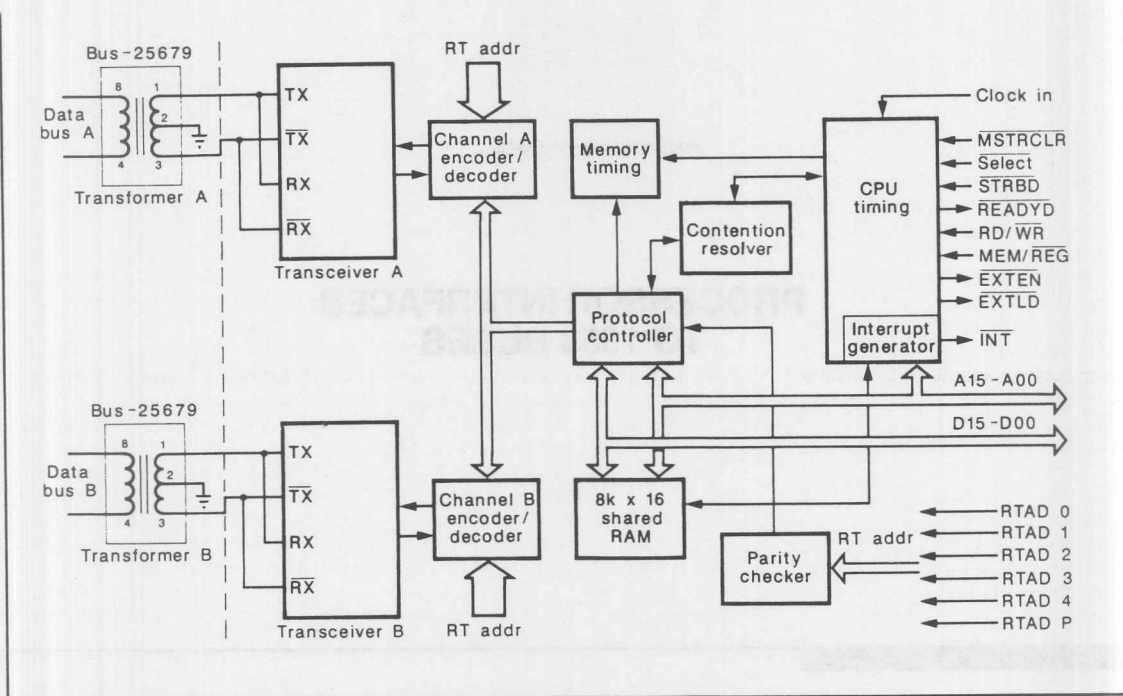


Fig. 1 Block diagram of the Bus 61553 Aircraft Integrated Multiplex Hybrid

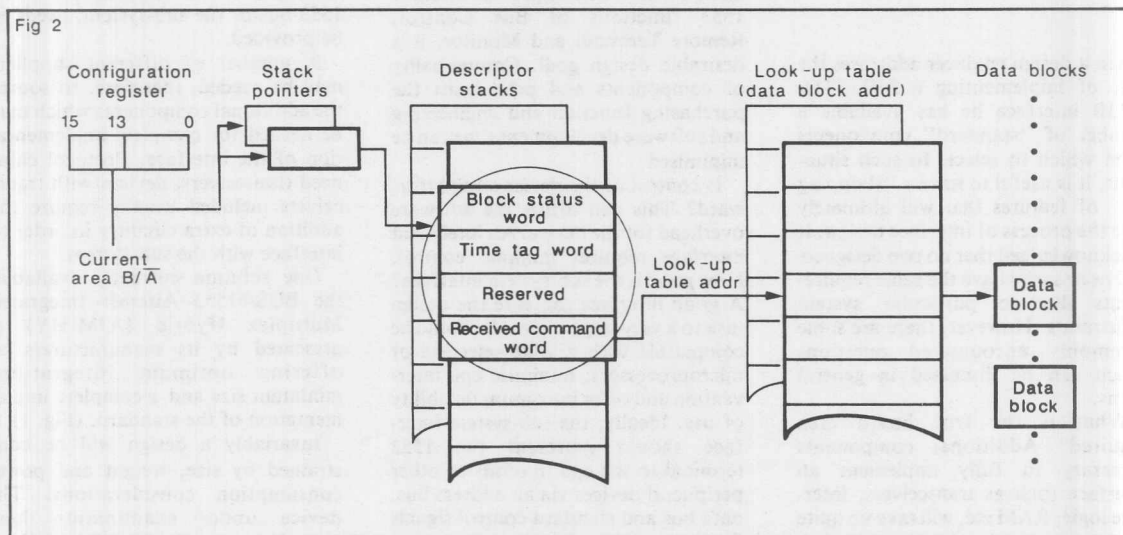


Fig. 2 Use of the descriptor stack—remote terminal configuration

The 'front end' is a dual low-power monolithic based transceiver. The typical standby power consumption of 0.54W keeps the temperature rise to acceptable levels and contributes to high MTBF. The protocol is contained in one silicon on sapphire custom ic and implements Bus Controller, Remote Terminal and monitor functions. All 13 dual redundant mode codes are catered for as is Broadcast.

The Remote Terminal Status Word is automatically generated allowing for sub-system inputs (Busy, Service Request etc). Status will automatically be suppressed should an invalid message be received and the Message Error bit will be set.

In Bus Controller mode, timing and full error checking is performed on all received transmissions providing comprehensive information to the sub-system host. All transmissions from the device are "wrapped around" through the front end and compared for data integrity. Monitor mode

allows all bus traffic to be received for systems analysis. Each received word in this mode has a tag word added indicating word validity, word type etc, to aid the analysis.

The sub-system interface circuitry is designed to minimise the host processor overhead associated with the "housekeeping" routines necessary to accomplish the transfers of information between the bus interface unit (BIU) and memory. As the sub-system interface is central to the discussion of the application of the AIM BIU, we need not dwell upon it just yet. The device is completed by  $8k \times 16$  random access memory. This amount of RAM is normally more than sufficient for most applications. However, the amount of RAM can be extended external to the device if necessary to a maximum of 64k; the amount of memory that can be addressed by the interface circuitry.

The BIU is packaged hermetically in a metal dual-in-line pack for operation over the full temperature

range  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . It is available fully compliant to MIL-STD-883 REV C, class B. In order to appreciate the application possibilities of the AIM-BIU, it is helpful to understand how the sub-system interface (SSI) works. Let us first investigate RT configuration. As an RT the BIU is usually required to cope with transfers of data to and from a number of sub-addresses. The SSI of the device contains a look-up table which, during initialisation, would be loaded with the starting address of blocks of memory in RAM (data blocks). There should be a data block for each combination of Transmit/Receive for each sub-address utilised in the RT (see Fig. 2). In fact there are two look-up tables A and B as the SSI has an in-built double buffering mechanism. This function offers the designer current and non-current areas of RAM for every data block, precluding overwriting stored data.

When a Command Word is received, it is stored in the fourth

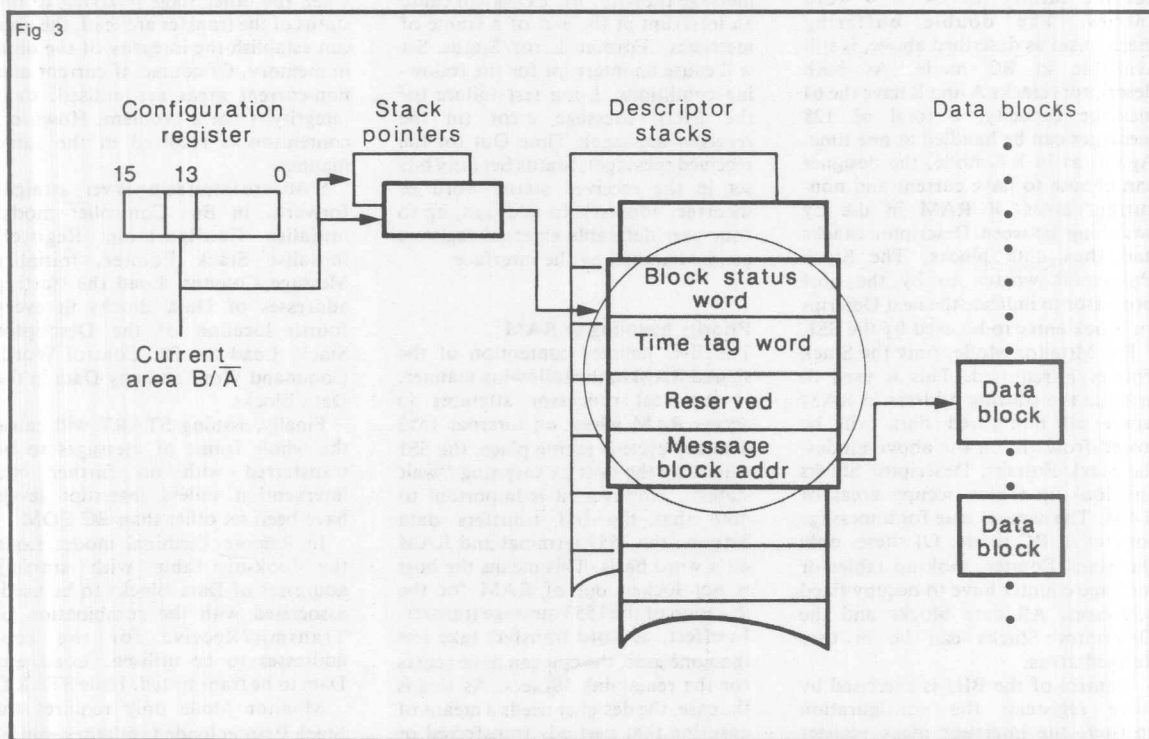


Fig. 3 Use of the descriptor stack—BC mode



location of the next entry in a Description Stack. In addition to the Command Word, the Descriptor contains information relating to the status of the transferred message associated with the data block. This is particularly useful when the host processor needs to access RAM. We will look at this in more detail later. The SSI looks up the correct data block address and completes the transfer of data by writing to or reading from the data block. The Stack Pointer increments, following a transfer, to the next descriptor stack entry.

In Bus Controller configuration the look-up table is not required (Fig. 3). The fourth location of the descriptor stack entry is loaded with the message block address. The descriptor stack has the facility for  $64 \times 4$  word entries. The double buffering mechanism as described above, is still available in BC mode. As both descriptors stacks A and B have the 64 message capacity, a total of 128 messages can be handled at one time. Again, as in RT mode, the designer can choose to have current and non-current areas of RAM in use by switching between Descriptor Stacks and thus data blocks. The Stack Pointer is written to by the host processor to indicate the next Descriptor Stack entry to be used by the SSI.

For Monitor Mode, only the Stack Pointer is required. This is used to indicate the starting address in RAM where all monitored data will be stored from. In all the above modes, the Stack Pointer, Descriptor Stacks and look-up tables occupy areas of RAM. The same is true for a message counter in BC mode. Of these, only the Stack Pointer, look-up tables or message counter have to occupy fixed addresses. All data blocks and the Descriptor Stacks can be in user defined areas.

Control of the BIU is exercised by three registers: the configuration register, the interrupt mask register and the start/reset register. The configuration register is used to set the

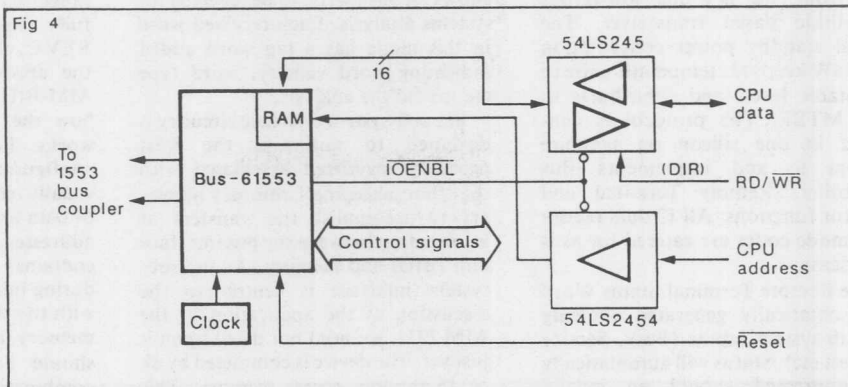


Fig. 4 AIM-BIU to central processing unit basic block diagram

operation mode, set sub-system flags (busy etc), select the current area of memory in use (A or B) and enable a Stop on Error facility. The interrupt mask register allows the user to select interrupts as required. EOM will cause an interrupt at the end of every message transfer. BC EOM will cause an interrupt at the end of a frame of messages. Format Error/Status Set will cause an interrupt for the following conditions: Loop test failure (of the BIU); Message error (in the received message); Time Out (of the received message); Status Set (any bits set in the received status word or incorrect address). In addition, up to four user definable external registers can be handled by the interface.

#### Priority handling in RAM

The BIU handles contention of the shared RAM in the following manner. If the host processor attempts to access RAM whilst an internal 1553 memory cycle is taking place, the SSI will delay the host by inserting "wait states". However, it is important to note that the SSI transfers data between the 1553 terminal and RAM on a word basis. This means the host is not locked out of RAM for the duration of the 1553 message transfer. In effect, as word transfers take less than one  $\mu$ sec, the cpu can have access for the remaining  $19\mu$ secs. As this is the case, the designer needs a means of ensuring that partially transferred or updated data blocks are not accessed. The Block Status Word in the

descriptor includes two flags; SOM (start of message) and EOM (end of message). SOM is set at the initialisation of a transfer to or from RAM. It stays set until the whole transfer has taken place, at which point it is cleared and EOM is set. In this manner, and when the other flags referring to the status of the transfer are read, the user can establish the integrity of the data in memory. Of course, if current and non-current areas are utilised, data integrity is not a problem. However, contention is resolved in the same manner.

Software interfacing is very straightforward. In Bus Controller mode: initialise Configuration Register, initialise Stack Pointer, initialise Message Counter. Load the starting addresses of Data Blocks in every fourth location of the Descriptor Stack. Load the BC Control Word, Command Word and any Data in the Data Blocks.

Finally, issuing START will cause the whole frame of messages to be transferred with no further cpu intervention unless interrupt levels have been set other than BC EOM.

In Remote Terminal mode: Load the look-up table with starting addresses of Data Blocks to be used, associated with the combination of Transmit/Receive for the sub-addresses to be utilised. Load any Data to be transmitted. Issue START.

Monitor Mode only requires the Stack Pointer loaded with the required starting address in RAM where information will be stored and the

START issued. Hardware interfacing allows for many popular cpus to be connected to the BIU. Fig. 4 shows a basic block diagram for a hardware interface. The Control Signals are standard interface signals for handling the flow of data between the cpu and AIM-BIU. These are defined below specifically for a range of microprocessors.

**MIL-STD-1750 processors (Fig. 5a)**  
Interconnection is straightforward as illustrated.

**Motrola 68000 (Fig. 5b)**  
As this microprocessor is byte oriented, direct word transfers to odd and even locations as required by the AIM-BIU, cannot take place. This is overcome by offsetting the cpu address bus and not connecting A0 as shown in Fig. 5b. /STRBD, which indicates a valid cycle, is derived by

ORing the upper and lower data strobes. /READYD is used as the /DTACK input to the 68000. This signal is shown buffered if there should be more than one device connected to this input to the cpu.

**Intel 8086 processor (Fig. 5c)**  
The 8086 interface is similar to the 68000 above. /STRBD is derived by ORing /MEMRD and /MEMWR signals. /READYD is inverted to create the correct logic sense and gated for when the AIM-BIU is not in use.

**Zilog Z8000 (Fig. 5d)**  
Again, the interface for the Z8000 is basically the same as the previous two. The /READYD signal is used to derive the /WAIT signal required by the Z8000.

It is important to note that Figs. 5a-5d illustrate interconnections for

use with the internal  $8k \times 16$  RAM. However, control signals are available from the AIM hybrid to enable the user also to utilise both internal and external RAM or, if preferred, external RAM only.

In summary, in this device, the design engineer is offered a complete MIL-STD-1553B bus interface unit and the facility to design a "standard" interface card for both BC & RT. His board size is minimised as is power consumption. Only standard control signals are required for the sub-system interface which is compatible with most "off the shelf" microprocessors. Memory mapping is mostly user definable with considerable memory expansion capability. Double or multiple buffering is supported. Dynamic self testing and built in test (BIT) features provide for data integrity. □

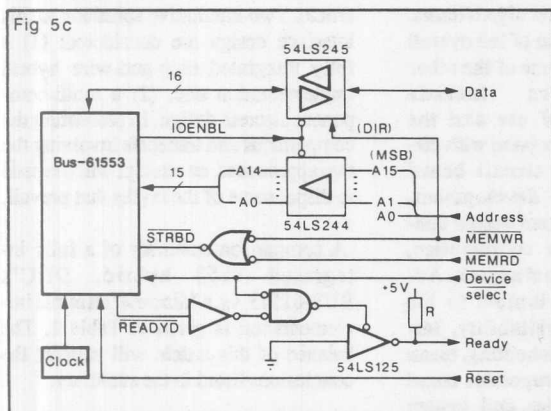
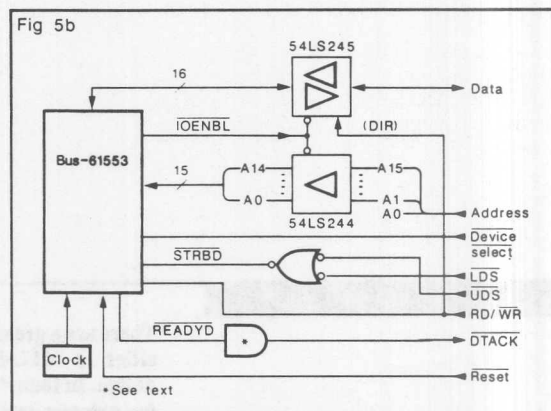
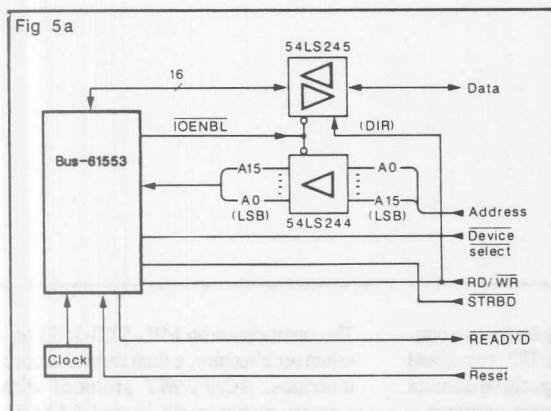


Fig. 5c Intel 8086 CPU interface

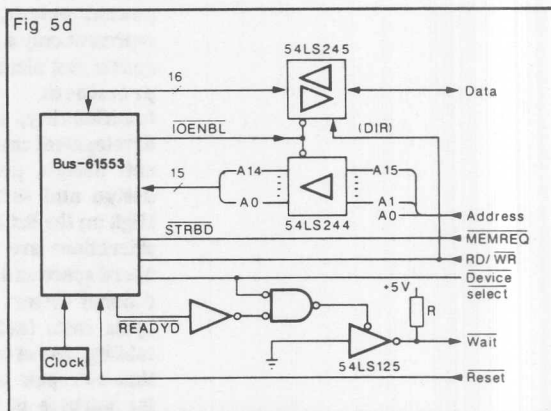


Fig. 5d Zilog Z8000 CPU interface

## A SYSTEMS APPROACH TO MIL-STD-1553 TERMINAL DESIGN

There are a great many factors to consider in MIL-STD-1553 terminal design. In today's competitive climate for avionics systems, cost assumes a high degree of importance. Component prices, while significant, represent only a portion of the overall system cost picture. Some of the other prominent factors include functionality, ease of use and the development costs associated with circuit design, printed circuit board design and software development. High on the list of system design considerations are power consumption, board space and thermal aspects. Additional factors contributing to life cycle costs include reliability, testability, ease of troubleshooting, mean time to repair and component count for purpose of logistics and system maintenance.

The most common MIL-STD-1553 terminal architecture, a dual redundant bus interface, BC/RT/MT protocol with memory management, shared RAM interface and RAM is the subject of this article. Two alternative solutions to this interface design are considered: (1) a fully integrated chip-and-wire hybrid implementation and, (2) a multi-component discrete design. In presenting the comparisons and tradeoffs involving the two approaches, an attempt will be made to dispel some of the myths that prevail.

A comparison summary of a fully integrated 1553 hybrid, DDC's BUS-61553, vs. a "discrete" terminal implementation is given in Table 1. The balance of this article will support the conclusions listed in the summary.

**TABLE 1. COMPARISON SUMMARY:**  
BUS-61553 AIM Hybrid vs. "Discrete" 1553 Terminal Implementation

PARAMETER	BUS-61553 AIM HYBRID	"DISCRETE" TERMINAL
Component Cost (Qty. 100)	\$1088	\$1135
NRE Costs	Moderate	Higher
Purchasing, Inspection and Handling	Low	Higher
P.C. Board Cost	Low	Higher
Board Assembly, Inspection and Re-Work	Low	Higher
Power Dissipation (W.)	1.325 (typ.) 2.155 (max.)	1.497 (typ.) 2.270 (max.)
Board Space (plug-in package)	4.33 sq. in.	5.22 sq. in.
Junction-to-Case Thermal Resistance	6.13 degrees C per watt	7.00 degrees C per watt
Layout Complexity	Low	Moderate
Software Complexity	Low	High
MTBF (ground benign environment) at 25 degrees C (hrs)	6,553,000	4,200,000
at 125 degrees C (hrs)	55,000	39,500
Testability	Good	Fair
Troubleshooting Effort Required	Minimal	Complex
MTTR	Low	Higher
Life Cycle Costs	Moderate	Higher

## CHIPS vs. HYBRIDS

There exists a good deal of confusion with respect to the tradeoffs regarding the use of a single hybrid in contrast to multiple discrete packaged chips, particularly in relation to MIL-STD-1553 interface design. The two fallacies that need to be dispelled are:

### (1) The Fully Monolithic 1553 Solution.

**There is no such thing.** As of this writing, there are no fully monolithic 1553 transceivers. Several have tried, but to date nobody has succeeded in producing a fully monolithic transceiver not requiring external passive components. The main area of difficulty lies in producing resistors and capacitors on a bipolar chip (providing the power level mandated by -1553 from a monolithic CMOS transmitter is not considered feasible at this time) to meet 1553's stringent electrical criteria. These passive components would have to be accurate and stable enough to reliably yield 1553's transmitter rise/fall times and receiver filter characteristics over the military temperature range. As a result, virtually all 1553 transceivers are implemented as hybrid circuits utilizing thick film

resistors and chip capacitors external to the active chips, or as discrete designs. Since a hybrid is required for the transceiver function, virtually all present day 1553 implementations include a minimum of one hybrid component. The "Monolithic 1553 Solution" is, indeed, a specious claim.

### (2) Monolithics Are Less Expensive Than Hybrids.

In a first glance price comparison between a 1553 protocol chip and a fully integrated 1553 hybrid, the protocol chip may appear to be the more economical choice. **In point of fact, this is not the case.** In order to comprise a complete microprocessor to shared RAM/1553 bus interface, today's single hybrid component is nearly autonomous. By contrast, in order to assemble a complete 1553 solution, the protocol chip requires, in addition to a clock oscillator, buffers and transformers; a separate hybrid transceiver, two packaged memory chips as well as increased P.C. board space and complexity. This article will proceed to show that the total cost of these components is greater than the single 1553 hybrid. Moreover, beyond raw material pricing, there are a num-

ber of other cost drivers that favor the single component solution.

## NON-RECURRING COSTS

This article takes a look at non-recurring engineering costs broken down into four areas: proposal costs, circuit design, printed circuit board layout design and software development.

The use of a single component provides obvious advantages in terms of proposal preparation effort. Since many system proposals are done on a tight schedule, it is of urgent importance to minimize not only risk but also the number of components requiring selection and evaluation. Typically, this entails analyses of functionality, cost, board space, power requirements, reliability and other system parameters. If this evaluation is done on a comparative basis, it will inevitably favor the use of the single integrated hybrid over the discrete design.

In contrast to an autonomous hybrid, a design consisting of multiple components requires additional analysis and evaluation to verify performance and ensure an optimal design. This generally entails the time, cost and risk of com-



ponent selection; breadboard design, build and evaluation. Assuming all goes well in the breadboard stage, the amount of documentation required for a multi-component bus interface design will be of necessity greater than that for a single hybrid. The use of the integrated hybrid design eliminates this portion of the system breadboarding, allowing the design team to concentrate on higher level tasks in the system development.

There is little question that the time, cost and risk of printed circuit board layout design for a multiple component 1553 interface is much greater than that incurred when designing in a single hybrid. Several factors favor the use of a single hybrid: (1) P.C. board real estate. This is often at a premium in avionics systems. The combination of a pin grid array 1553 protocol chip plus external transceiver and RAM chips will require more board space than a single integrated hybrid. This can be a restricting and complicating factor in P.C. board layout design. (2) The use of a multiple component 1553 interface will, in all likelihood, lead to the added complication of more board layers. The probability of having to add P.C. board layers will be even greater if the protocol chip is packaged in a pin grid array (PGA) package. (3) Routing. The use of the multi-component 1553 interface will require approximately 60 more interconnects than will the integrated hybrid. This is primarily attributable to the use of discrete static RAM chips, entailing the additional routing of 16-bit wide address and data buses, plus control signals. If the protocol chip is packaged in a PGA package, the routing task is further complicated by the difficulty of passing signals through the board region populated by the pin grid (four sides, multiple rows). (4) Component positioning. This is an aspect that should not be trivialized. Some of the issues requiring careful attention are component spacing, trace length, crosstalk and ground planes. The most risky interconnects, in terms of layout, are the protocol chip-to-transceiver and transceiver-to-transformer interfaces. Care must be taken in these areas to ensure proper transceiver and encoder/decoder opera-

tion. If the layout of this section has excessive capacitance, the effective input impedance of the receiver as seen from the bus could fall below 1553's specifications. Other possible effects of poor decoder/receiver layout include crosstalk and/or timing skews. In some instances, these can lead to failure of the 1553 tests for word error rate and zero-crossing deviation. The use of the integrated hybrid eliminates the protocol-to-transceiver interconnect on the board. Internal to an integrated 1553 hybrid, the transceiver-to-protocol connection distance is kept to an absolute minimum; the layout for this section is designed and optimized very carefully, tested and proven many times over.

**Software.** In many avionics systems, software represents the most expensive NRE item. The inherent complexity of real time data communications software is an important factor in 1553 terminal implementation. In terms of the software required to control a 1553 I/O port, the development effort may be minimized by judicious component selection. The important factors to consider are functionality and ease of programming. The level of functional complexity should be sufficient, but not greater, than that needed to meet the system requirements. The overkill of too much functionality can, in many instances, complicate the software development. Selecting a 1553 interface configuration with the optimal architecture for a specific interface requirement can lead to software development savings in several areas: learning curve, design, coding, system integration and debug, documentation and maintenance. These cost factors can be further magnified if the burdens of DOD-STD-2167A are mandated for a particular program.

The architecture of the AIM series hybrids includes a number of features to facilitate software development. These include a minimal number of registers (three) as well as highly simplified pointer and data structures. Some of the programmer-friendly features of the AIM hybrids include a single stack area containing both BC setup information as well as a chronology of all messages

processed for BC and RT modes. For each BC message, control information is contained in a single word. For RT mode, data blocks for individual messages are located in the shared RAM by means of a single lookup table pointer for each TR/subaddress. Other features include comprehensive error handling and maskable interrupt conditions. The AIM hybrids, being the second generation of the same design, represent a thoroughly proven architecture.

By contrast, other 1553 protocol devices, aside from being less proven than the AIM hybrid family, contain many times the number of registers (typically 14 to 16) and more complex data structures than do the AIM hybrids. In a typical application, there are many more data pointers and interrupt conditions to be managed. The inevitable result is an extended learning curve period and increased coding/debug time required for software development. Furthermore, memory (RAM/ROM) requirements tend to be higher and effective data throughput rates tend to be lower (due to increased BC intermessage gap times) for these implementations of the -1553 protocol. To summarize, the AIM hybrids, by virtue of their simple, versatile and proven design, provide an optimal tradeoff between functional performance and software development time.

## RECURRING COSTS

Depending on production volume, recurring costs may assume a greater level of importance than NRE costs. For the 1553 interface, the two areas of recurring cost are component cost and miscellaneous system production costs.

The primary recurring cost is component cost. The cost analysis, in Table 2, compares the pricing of a single 1553 hybrid terminal against the total cost of a multi-component design, consisting of a PGA protocol chip plus dual hybrid transceiver and two discrete 8K X 8 static RAM chips. This comparison assumes 100 piece quantities and MIL-STD-883 parts screening. The costs of tri-state data and address buffers, clock oscillator and pulse transformers are not considered, since they are common to both approaches.



TABLE 2. COST ANALYSIS	
Single component vs Multi-Component (100 piece quantity)	
<b>Single Component 1553 Interface:</b>	
BUS-61553-883B.....	\$1088
<b>Multi-Component 1553 Interface:</b>	
Multi-Component 1553 Interface:	
1553 Protocol PGA Chip.....	\$ 600
Dual Hybrid Transceiver.....	\$ 415
Two 8K X 16 Static RAM Chips.....	\$ 120
<b>TOTAL.....</b>	<b>\$1135</b>

While the component cost advantage for the integrated hybrid 1553 terminal solution over the multi-component approach is relatively modest, the comparison is clearer in other recurring aspects of system production. The reduced number of components results in cost advantages throughout the production cycle. This includes:

- (1) Purchasing
- (2) Paperwork
- (3) Material Handling
- (4) Incoming Inspection
- (5) Component Test
- (6) Printed Circuit Board Cost
- (7) Board Assembly
- (8) Board Inspection
- (9) Testing and Troubleshooting
- (10) Yield and Re-work costs

## ADVANTAGES OF THE AIM SERIES INTEGRATED 1553 SOLUTION

As mentioned, the use of the integrated hybrid results in advantages throughout the development and production cycles. In addition to the advantages listed above, it is important to consider that a 1553 hybrid such as the BUS-61553 is procured as a **fully integrated, tested and inspected single component**. All other things assumed equal (they're not), this reduces the associated cost and overhead burdens for the user.

### Power and Thermal Considerations.

Several important aspects of system design relate to power requirements. These include the number of supply voltages, current requirements, dissipation, size, weight, complexity, heatsinking and thermal budgeting. All weigh significantly in system MTBF and life cycle costs.

DDC, in the evolution of its 1553 product line, has been through several generations of transceiver and protocol design. The present generation of transceivers integrates all active components onto a single monolithic chip per

channel requiring only a -15 volt or -12 volt supply along with a +5 volt supply. The need for a +15 or +12 volt supply, as required in earlier generation DDC products and some competitive transceivers, is eliminated. The latest generation transceiver monolithics, which are incorporated into the BUS-61553 and BUS-61554 hybrids, not only eliminate the need for a positive supply rail, but greatly reduce the 1553 interface power consumption and power dissipation. Going one step further, the +5 volt only dual transceiver integrated into the BUS-61555 AIM hybrid not only eliminates the -15V (-12V) supply as well as the +15V (+12V) supply, but requires an **even lower level of input power** than the BUS-61553 or BUS-61554. In fact, since the transceiver is integrated in the same package as the protocol, it has been possible to optimize the design of the receiver logic such that the 5 volt transceiver in the BUS-61555 draws even lower power (about 10% at Idle) than the corresponding dual transceiver hybrid, the BUS-63148. This provides an advantage for the 5 volt AIM hybrid that cannot be duplicated in a multi-component discrete design.

## THE BUS-6155X/6X AIM SERIES HYBRIDS

Figure 1 illustrates a simplified block diagram of the BUS-61553 Advanced Integrated Mux Hybrid (AIM-HY). The BUS-61553 AIM hybrids comprise complete 1553 BC/RT/MT terminals. They are available in 78-pin DDIP or 82-pin flatpack packages. Power supply options include -15V/+5V, -12V/+5V and +5 volt only.

The AIM hybrids contain dual low power transceivers and encoder/decoders. The active components for the 15V and 12V transceivers are integrated on a single chip for each bus channel. The Manchester II decoders sample the received signal with a 16 MHz clock, achieving better noise rejection and zero crossing distortion tolerance than 10 MHz or 12 MHz decoders. The RT protocol in the AIM series hybrids is an industry standard design, implementing all MIL-STD-1553B message formats and dual redundant mode codes. Likewise, the BC protocol supports all options of 1553. In monitor mode, each 16-bit word plus an associated identification word is stored for each word received.

The AIM hybrids include 8k X 16 of shared RAM, a shared RAM interface and memory management. The interface implements a wait state type of handshake, simplifying connection to 16-bit or 8-bit microprocessors. The AIM internal memory management logic maintains a stack data structure.

In addition to facilitating multi-message BC frame scheduling, the stack provides a chronology of all messages processed for both BC and RT modes. For RT mode, messages are stored in data blocks, indexed by TR/subaddress via lookup tables in the shared RAM.

Maskable interrupts are provided for end-of-message, end of BC message list and message error conditions.

The protocol, memory management and interrupt structures of the AIM series hybrids provide a robust platform for 1553 software design and system integration. In addition to comprising a thoroughly proven and easily mastered architecture, the AIM provides compatibility to earlier generation multi-hybrid implementations as well as to DDC's PC-BUS and VME-BUS board level products.

The AIM hybrids consume very low power, particularly the 5 volt only version, the BUS-61555. The BUS-61553 has passed SEAFAC validation testing, ensuring full compliance to MIL-STD-1553B. The BUS-61553 (15V) and BUS-61554 (12V) have a DESC drawing pending. All of the AIM hybrids are manufactured in DDC's DOD-STD-1772 facility. 1772 processing is required in order to screen hybrids to 883B. The hybrids are available in 0 to 70 degrees C. and "B" screening (similar to 883B but without QCI testing) as well as 883.

Going beyond low power consumption/dissipation, the AIM series hybrids provide a further advantage in the area of thermal management. This results from the larger surface area of the AIM hybrid package. The larger package surface area, 3.93 sq. inches vs. 1.32 for a 36-pin DDIP transceiver, results in a lower junction-to-case thermal resistance, and thus improved reliability for the AIM over a multi-component implementation. The junction-to-case thermal resistance of the AIM series hybrids is 6.13 degrees C per watt; for the current generation 36-pin DDIP transceiver, the thermal resistance is 7.00 degrees C per watt. Since most of the dissipation (and thus a significant portion of the failure rate) of a 1553 interface is concentrated in the transceiver section, this factor should not be taken lightly.

The power dissipation comparison of the AIM series hybrids to a discrete component 1553 interface is as indicated in Table 3. Typical and maximum power dissipation values are indicated for 25% transmit duty cycle. At this duty cycle, it should be noted that the total power consumed by the 1553 interface is about 0.3 watts higher than the power dissipated.

The 0.3 watts are dissipated in bus isolation and termination resistors.

TABLE 3. POWER DISSIPATION COMPARISON		
AIM series hybrids vs a discrete component 1553 interface		
AIM Series Integrated Hybrids	typ	max
BUS-61553 (5V/-15V):	1.325	2.155
BUS-61554 (5V/-12V):	1.213	1.975
BUS-61555 (5V):	0.725	1.250
"Discrete" 1553 Terminal Solution		
Protocol/Interface PGA:	0.175	0.250
Two IDT 7164S55DB		
8K X 16 Static RAM		
Chips: 2 X 0.080/0.110 =	0.160	0.220
BUS-63125II Transceiver (+5/-15V):	1.162	1.800
BUS-63127II Transceiver (+5/-12V):	1.050	1.620
BUS-63147 Transceiver (+5V):	0.485	0.940
Total "Discrete" Terminal:		
+5V/-15V:	1.497	2.270
+5V/-12V:	1.385	2.090
+5V only:	0.820	1.410

For each supply voltage category, the AIM integrated solution requires less power than the discrete 1553 interface.

To summarize, the low levels of power consumption/dissipation and inherent heatsinking of the AIM series hybrids provide several advantages. Decreased power supply requirements serve to reduce size, complexity, weight and heatsinking. Furthermore, the task of thermal management for the 1553 interface (transceiver) simplifies mechanical design and assembly costs by reducing the need for heatsinking rails and cooling fans.

**P.C. Board Space, Cost.** The recurring cost for a P.C. board accommodating a multi-component discrete 1553 terminal design will be inevitably higher than for a board incorporating a single bus interface hybrid. As a bare minimum, the board for the multiple components will need to have at least 100 additional holes. This is just to accommodate components; moreover, additional holes will be required for vias (feedthroughs) to interconnect the multiple components. An even larger increase in recurring

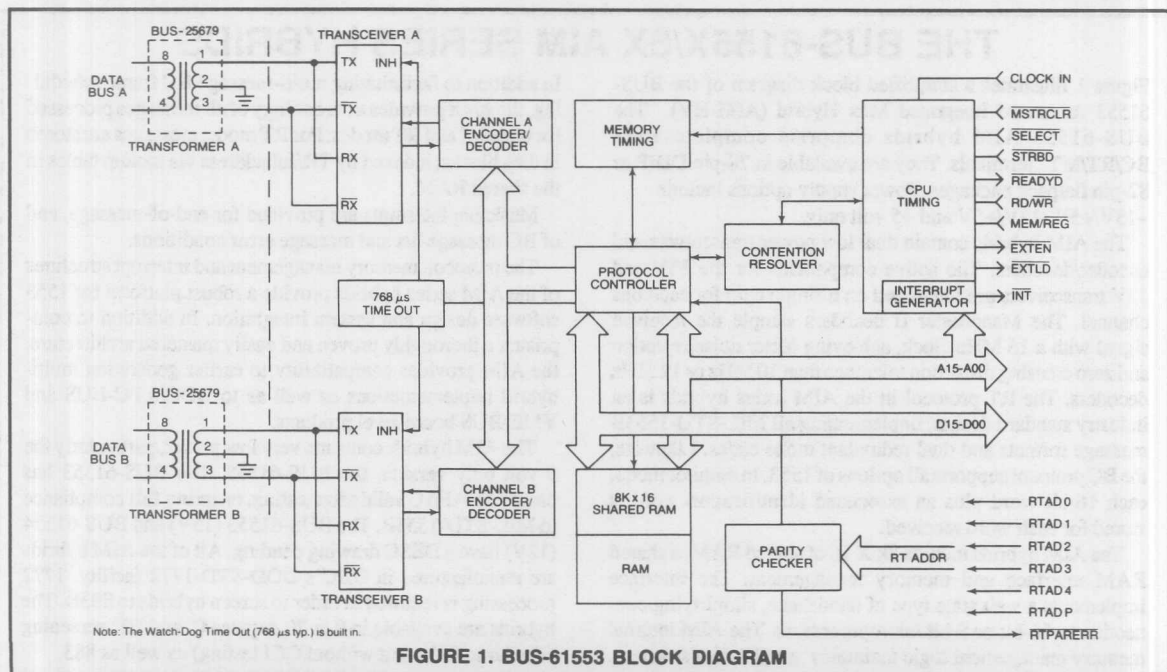


FIGURE 1. BUS-61553 BLOCK DIAGRAM

board cost will be incurred if additional layers are required to accommodate the multi-component terminal. This is likely to be the case. In terms of yield and reliability, the board for the multi-component 1553 terminal, with its greater number of layers, holes and routing density will have the greater chance of failure due to faulty solder lands, joints or solder bridging.

The board space analysis in Table 4 assumes 0.1 inch component spacing. For surface-mounted (flatpack) components, a formed lead length of 0.035 inch on each lead side is assumed. The analyses do not consider the board space required for transformers, tri-state buffers or clock oscillators, which are common to both approaches.

TABLE 4. BOARD SPACE ANALYSIS AIM series hybrids vs "Discrete" 1553 terminal	
AIM Series Hybrids:	sq.in.
(DDIP)((2.1 + 0.1)x(1.87 + 0.1)) =	4.33
(Flatpack)((2.19 + 0.1)x(1.6 + .17))=	4.05
<b>"Discrete" 1553 Terminal Solution:</b>	
Total Board Space =	
Protocol/Interface PGA:	
((1.1 + 0.1)x(1.1 + 0.1))	
+ Dual 36-pin DDIP Transceiver:	
((0.775 + 0.1)x(1.7 + 0.1))	
+ Two 28-pin DDIP RAM Chips:	
((2)x(1.465 + 0.1)x(0.605+0.1))	
Total Board Space =	5.22
<b>Surface mounted "discrete" solution:</b>	
Total Board Space (Flatpack)=	
Protocol/Interface :	
((1.15 + 0.17)x(1.15+0.17))	
+ Dual 36-pin DDIP Transceiver:	
((0.785 + 0.17)x(1.905 + 0.1))	
+ Two 28-pin DDIP RAM Chips:	
((2)x((0.725+0.1)x(0.500+0.17))	
Total Board Space (Flatpack)=	4.76

**System Production Costs.** The use of a single component rather than several components results in a number of cost advantages in the labor intensive areas of system manufacturing. The various costs of component procurement are reduced in proportion to the number of line items on the parts list. This includes the overhead associated with purchasing, paperwork and material handling. Similarly, the costs of incoming inspection

and component test labor are held to a minimum by the use of the integrated hybrid. The efforts required for P.C. board assembly and inspection are similarly minimized. This can result in significant cost savings. If the 1553 protocol device for the discrete 1553 terminal is packaged in a pin grid array (PGA) package, inspection of P.C. boards becomes difficult. In all likelihood, the added complexity of the multi-component 1553 terminal will produce lower initial yield at board level assembly, resulting in higher re-work costs.

**Testing and Troubleshooting.** In terms of system costs, testing is a critical, labor intensive operation. This being the case, testability assumes an important role not only in production economics but also in terms of the total system life cycle costs. These costs are both non-recurring and recurring. NRE test costs include test equipment, fixturing design/build, test software development and documentation. Since system and subsystem test methodologies are typically developed independently at factory, maintenance depot and weapons platform sites, these development efforts represent a significant portion of the total support cost associated with any given system. The availability of 1553 protocol testers as well as general purpose analog and digital test equipment facilitates the development of end-to-end functional tests. Nevertheless, the need for diagnostic fixturing, procedures and software can add significantly to development costs.

In terms of testing and troubleshooting, the AIM series hybrids provide advantages over multi-component 1553 interfaces. It is clearly evident that the use of an integrated 1553 hybrid greatly reduces these NRE costs by eliminating the need for diagnostic hardware/software.

Recurring costs are substantially reduced by eliminating the potentially tedious and lengthy troubleshooting efforts required to fault isolate from among a 1553 protocol chip, a transceiver and discrete RAM chips. Some receiver/decoder problems can present subtleties in isolating the bad com-

ponent; in many instances, identifying the faulty component on 16-bit data/address buses involves trial and error. These time consuming troubleshooting situations are eliminated by the use of an integrated 1553 hybrid; if the 1553 interface does fail, there is only the single component to replace.

The AIM hybrids contain a number of built-in self-test features. In addition to supporting the RT "wraparound" test required by Notice II of MIL-STD-1553B, these include internal read/write registers and RAM, which are inherently self-testable, as well as loopback capability for the 1553 "front end". This latter feature, which supports both on-line testing for BC and RT modes as well as an off-line self-test, entails a comparison and validity check of the last transmitted word. This facilitates an "end-to-end" self-test, encompassing the processor interface logic, parallel and serial data paths, internal RAM, encoder/decoder, state machine and (optionally) the transceiver. Since self-test is a requisite element of modern systems design, the inclusion of these features is an important attribute to consider.

**Reliability.** For reasons of both cost and system availability, reliability is a very important parameter in military systems. For 1553-based systems, it is instructive to compare the mean time to failure (MTBF) of a hybridized integrated terminal to that of a "discrete" terminal design.

The reliability analyses, whose results are listed in Tables 5&6, compare the MTBF of a BUS-61553 AIM hybrid to that of a comparable "discrete" 1553 terminal. For each implementation, the failure rate of each component, including the respective P.C. board area, is factored in. The BUS-61553 is screened to MIL-STD-883C Class B in DDC's QML-38510 (MIL-STD-1772 qualified) facility. The BUS-61553 is assumed to be assembled on to a four-layer printed circuit board. The "discrete" terminal is assumed to consist of a PGA protocol device that is screened fully compliant to 883, including qualification; a BUS-63125II DDIP transceiver hybrid manufactured in DDC's facility and two

chips in CERDIP packages. It is assumed that the "discrete" terminal is assembled on a six-layer board. This is due to the additional layers required to accommodate the larger number of interconnects for the "discrete" terminal design. The analyses are performed in accordance with MIL-HDBK-217E. For both cases, 50% transmitter duty cycle is assumed at 25 and 125 degrees C. in a ground benign environment.

Note that the BUS-61553 has a significantly higher MTBF estimate: about 56% better at 25 degrees C.; about 39% better at 125 degrees C. The reliability advantage is primarily attributable to the processing of the hermetically sealed AIM hybrids in DDC's Qualified Manufacturers List (QML) facility. Additional factors favoring the AIM hybrid are the lower failure rate of the associated circuit board as well as the lower overall power dissipation and lower thermal resistance of the AIM hybrid in comparison to the 36-pin DDIP transceiver used in the "discrete" terminal design.

**Logistics and Life Cycle Costs.** In military system proposals, life cycle costs are assuming an increasing level of importance. In addition to raw component cost, there are a number of logistics related elements in total system life cost. These include component weight, power consumption, testability and ease of troubleshooting, MTBF and MTTR. The number of different types of components required to be stocked for spare parts is viewed as a very important parameter by military logistics people. Such factors as reliability, spare parts count, commonality throughout inventory and troubleshooting cost assume greater importance than raw component cost. The "post-procurement" percentage of total system life cycle costs is typically in the range of 70 to 80 percent. In the case of MIL-STD-1553 terminal design, the single component hybrid solution has advantages over a multi-component implementation in all of these areas.

TABLE 5. RELIABILITY ANALYSES		
BUS-61553 AIM Hybrid MTBF vs "Discrete" 1553 Terminal MTBF.		
Component	Failures/10E6 hrs.	
	25 degrees C	125 degrees C
For the BUS-61553 integrated hybrid solution:		
BUS-61553	0.1282	18.1493
4-layer P.C. board	<u>0.0244</u>	<u>0.0244</u>
<b>TOTAL</b>	<b>0.1526</b>	<b>18.1737</b>
	(MTBF=6,553,000 hrs.)	(MTBF = 55,000 hrs.)
For the "discrete" terminal solution:		
Protocol Chip	0.0436	3.7253
BUS-63125II Transceiver	0.0205	1.9786
8K X 8 Static RAM	0.0577	9.7768
8K X 8 Static RAM	0.0577	9.7768
6-layer P.C. board	<u>0.0586</u>	<u>0.0586</u>
<b>TOTAL</b>	<b>0.2381</b>	<b>25.3161</b>
	(MTBF=4,200,000 hrs.)	(MTBF = 39,500 hrs.)
<b>SUMMARY</b>	<b>MTBF HOURS</b>	
	<b>25 degrees C</b>	<b>125 degrees C</b>
<b>BUS-61553</b>	<b>6,553,000</b>	<b>55,000</b>
<b>DISCRETE TERMINAL</b>	<b>4,200,000</b>	<b>39,500</b>

TABLE 6. MTBF COMPARISON SUMMARY		
Component	MTBF (HOURS)	
	25 degrees C	125 degrees C
<b>BUS-61553</b>	<b>6,553,000</b>	<b>55,000</b>
<b>DISCRETE TERMINAL</b>	<b>4,200,000</b>	<b>39,500</b>

## CONCLUSION

The choice is abundantly clear. The single component 1553 terminal solution provides a number of advantages over a multi-component design. The use of an integrated 1553 terminal such as DDC's BUS-6155X AIM series hybrids provides advantages in the three major phases of system life cycle: development, production and maintainance/logistics.

Advantages of the AIM series hybrids in the NRE phase include reduction of proposal effort, simplified circuit design, simplified board layout design and a reduction of the required effort for software development.

For the system production cycle, the use of the AIM integrated terminal provides significant advantages. In addition to lower component cost, these include reduced purchasing overhead, lower P.C. board costs and board space and a reduction in the labor-intensive areas of board assembly, troubleshooting and re-work.

In terms of maintainance/logistics, the most significant aspect of life cycle costs, the AIM series hybrids provide lower power consumption, higher MTBF, fewer parts to inventory and reduced troubleshooting time and thus lower mean time to repair (MTTR).



## STREAMLINE YOUR MIL-STD-1553 DESIGN BY ELIMINATING THE CPU



That's right, eliminate the CPU. A new device, the BUS-65612 from ILC Data Device Corporation (DDC), allows a designer to interface minimal complexity systems, such as switches, pressure transducers, D/A converters, etc. to the MIL-STD-1553 bus without requiring the use of a CPU. This minimizes the board space required to interface to the military bus, and eliminates the need for software.

MIL-STD-1553 is a serial data bus developed initially for use in military avionic systems. Its reliability is one reason it is now being used in many other military systems such as tanks, submarines, the Space Station, and naval vessels. Many of these applications require communicating with sensors or gauges across the MIL-STD-1553 bus.

However, many engineers quake at the thought of having to interface a previously simple design, such as a D/A converter, to the MIL-STD-1553 bus. They envision having to tie up valuable board space for the multiple components needed to support the protocol. They shudder at the thought that they now have to add a microprocessor and write (and document) software to control their board.



Engineers need fear no more !!! A new monolithic device from DDC, the BUS-65612, incorporates the MIL-STD-1553 protocol into a single radiation hardened chip. The BUS-65612 supports Bus Controller, Remote Terminal, or Bus Monitor mode of operation.

It offers a 16 bit DMA interface to the subsystem, making it possible to interface minimal complexity systems (such as pressure transducers, D/A converters, switches, etc.) to the MIL-STD-1553 bus, without requiring a CPU. With the addition of a dual transceiver, two bus transformers, and a small amount of miscellaneous logic, the circuit is complete.

No software is necessary to implement the design !!!

This paper will examine this device and illustrate a direct method of controlling multiple D/A converters (to output analog values), a Synchro to Digital converter (to measure positioning information) and an LVDT/RVDT converter (to measure velocity) over the MIL-STD-1553 bus with the use of a single protocol chip.

## IMPLEMENTING MIL-STD-1553

The BUS-65612 is a new monolithic protocol unit from ILC Data Device Corporation (DDC). It is capable of implementing Bus Controller (BC), Remote Terminal (RT) or Bus Monitor (MT) operation. Fabricated using Silicon-On-Sapphire technology, it is radiation hardened to tactical levels. It is available as a pin grid array, in a 78 pin DDIP (the BUS-65610) or packaged with a dual transceiver as a 78 pin DDIP (the BUS-65142). The BUS-65612 utilizes a 16MHz clock, rather than the 12 MHz clock typically used in MIL-STD-1553 designs. The higher clock rate allows the BUS-65612 to sample the MIL-STD-1553 waveforms at more frequent intervals, providing superior bit error rates. See the block diagram of Figure 1.

## SAMPLE CIRCUITS

In the examples given in this paper, the BUS-65612 will be operating as an RT. This monolithic protocol unit has successfully passed the stringent RT Validation tests performed by SEAFAC at Wright Patterson Air Force base.

Thus a designer can rest assured that any design utilizing this part will fully meet the MIL-STD-1553 protocol requirements for Remote Terminals. For purposes of clarity, the Receive circuitry will be discussed separately from the Transmit logic.

## OPERATION OF THE BUS-65612 AS AN RT

Upon detection of a valid command which matches the user defined RT address as indicated by pins ADDRA - ADDRE and the address parity ADDR P, the BUS-65612 asserts the signal New Bus Grant, NBGT. This indicates the start of a new message transfer. 825-925 nanoseconds later, bits 0-10 of the command word can be obtained from the data bus. The subaddress and T/R values are also available on the address bus, pins A5 - A10. These values will remain latched on the address bus until receipt of the next valid command for this RT address.

The signal INCMD indicates that the BUS-65612 is presently handling a MIL-STD-1553 message transfer. See the timing diagram shown in Figures 3 & 4.

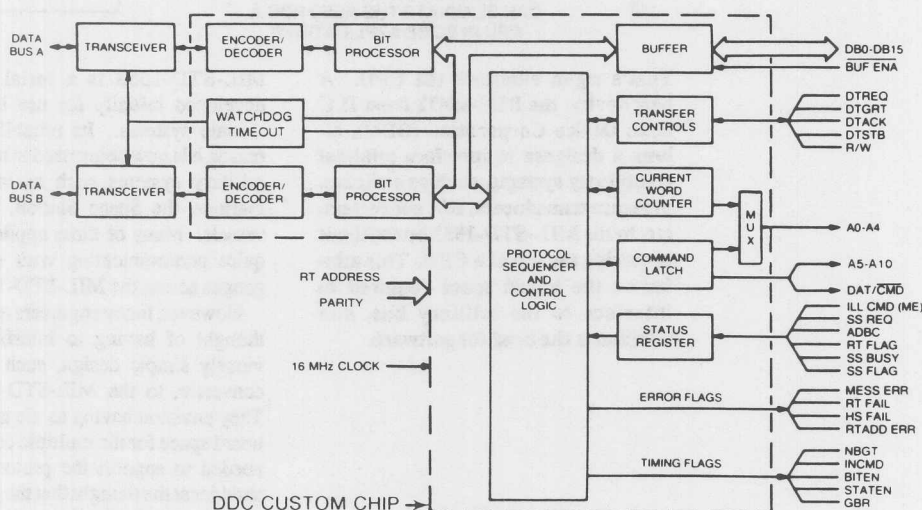


FIGURE 1. BLOCK DIAGRAM OF BUS-65612

## DMA OPERATION

Transfers to/from the subsystem are performed over the 16 bit data bus using a standard DMA handshake. The signal **DAT/CMD** indicates whether the word being transferred to the subsystem is a command or a data word. The signal **RD/WR** indicates the direction of the transfer. (A logic '1' indicates a transfer from the subsystem to the BUS-65612. A logic '0' indicates a transfer from the BUS-65612 to the subsystem.)

## RECEIVE COMMANDS

The signal **DTREQ** is asserted to initiate the DMA transfer cycle. The subsystem responds with **DTGRT**. The subsystem must respond with **DTGRT** within 2.10 microseconds for a command word transfer, and within 2.85 microseconds for a data word transfer. The BUS-65612 acknowledges acceptance of the data bus by asserting the signal **DTACK**. This signal should be connected to the **BUFEN** input pin to insure correct operation of the internal tristate buffers.

225 - 275 nanoseconds later, the signal **DTSTR** is asserted by the BUS-65612. The rising edge of this signal can be used to latch the word being transferred from the MIL-STD-1553 bus. Approximately 200 nanoseconds later, **DTACK** is removed, and the cycle is completed. See Figure 3.

## TRANSMIT COMMANDS

The signal **DTREQ** is asserted to initiate the DMA transfer cycle. The subsystem responds with **DTGRT**. The subsystem must respond with **DTGRT** within 2.10 microseconds for a command word transfer, and within 9.35 microseconds for a data word transfer. The BUS-65612 acknowledges acceptance of the data bus by asserting the signal **DTACK**. Once again, this signal should be connected to the **BUFEN** pin.

225 - 275 nanoseconds later, the signal **DTSTR** is asserted. The rising edge of this signal is used to latch the word being transferred to the MIL-STD-1553 bus into the internal buffers of the BUS-65612.

Approximately 200 nanoseconds later, **DTACK** is removed, and the cycle is completed. See Figure 4.

## MULTIPLE WORD TRANSFERS

If the received command word contained a word count greater than 1, the 5 least significant bits of the address bus will automatically be incremented when **DTACK** is removed. On the BUS-65612, the signal **ADRINC** will be asserted on the rising edge of **DTSTR**. (This signal is not available on the BUS-65142 package.) These signals allow the user to easily transfer blocks of data to/from sequential locations in RAM, without the need for additional circuitry. See the timing diagrams of Figures 2&3.

## SAMPLE RECEIVE CIRCUITRY

The circuit shown in Figure 2 interfaces multiple (2) D/A converters to the MIL-STD-1553 bus. The value to be converted to analog is downloaded by the BC as a receive command to the

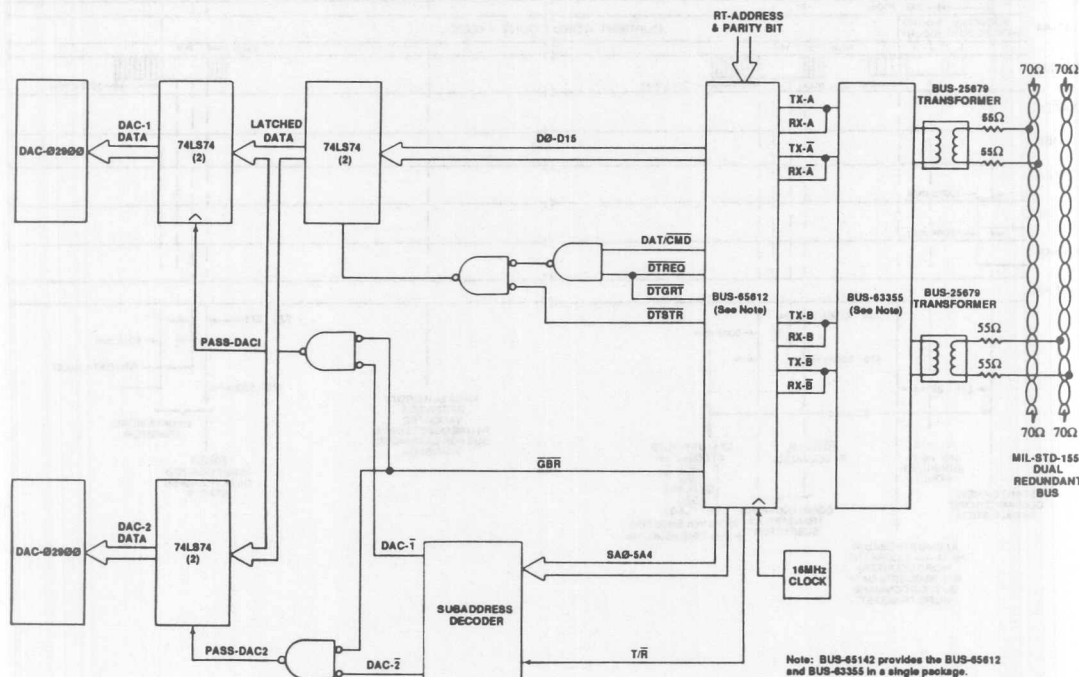
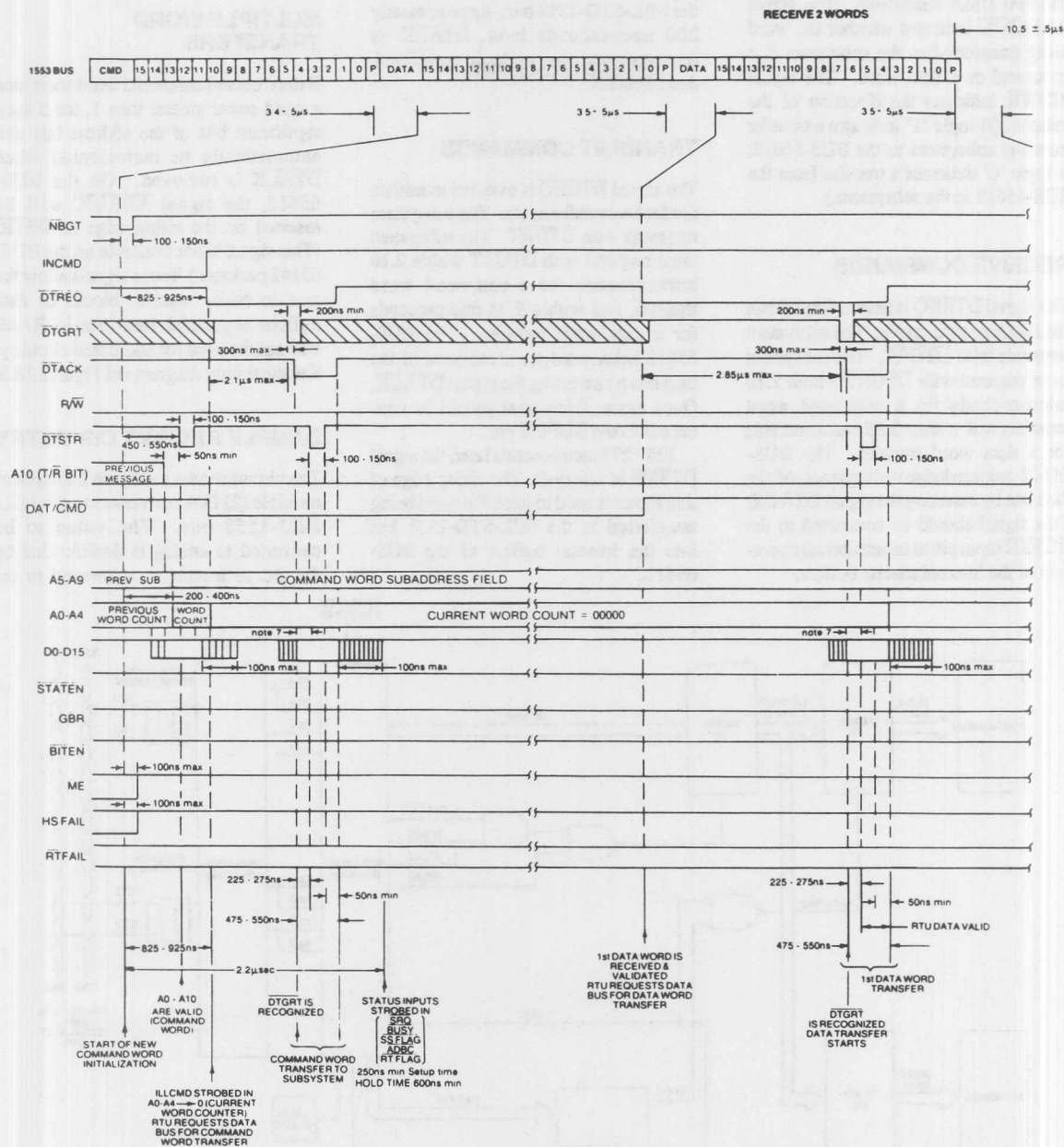


FIGURE 2. SAMPLE RECEIVE CIRCUIT



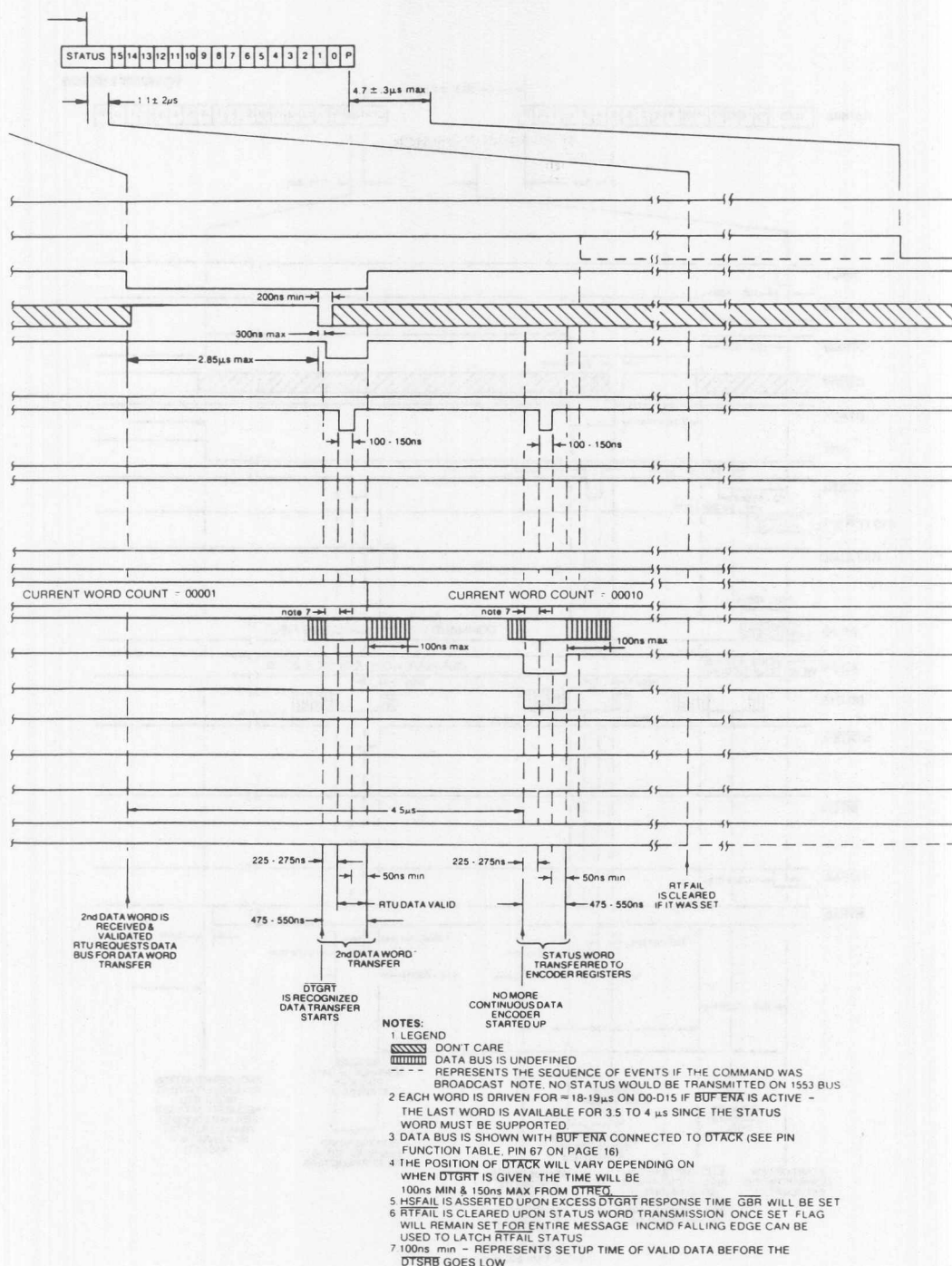
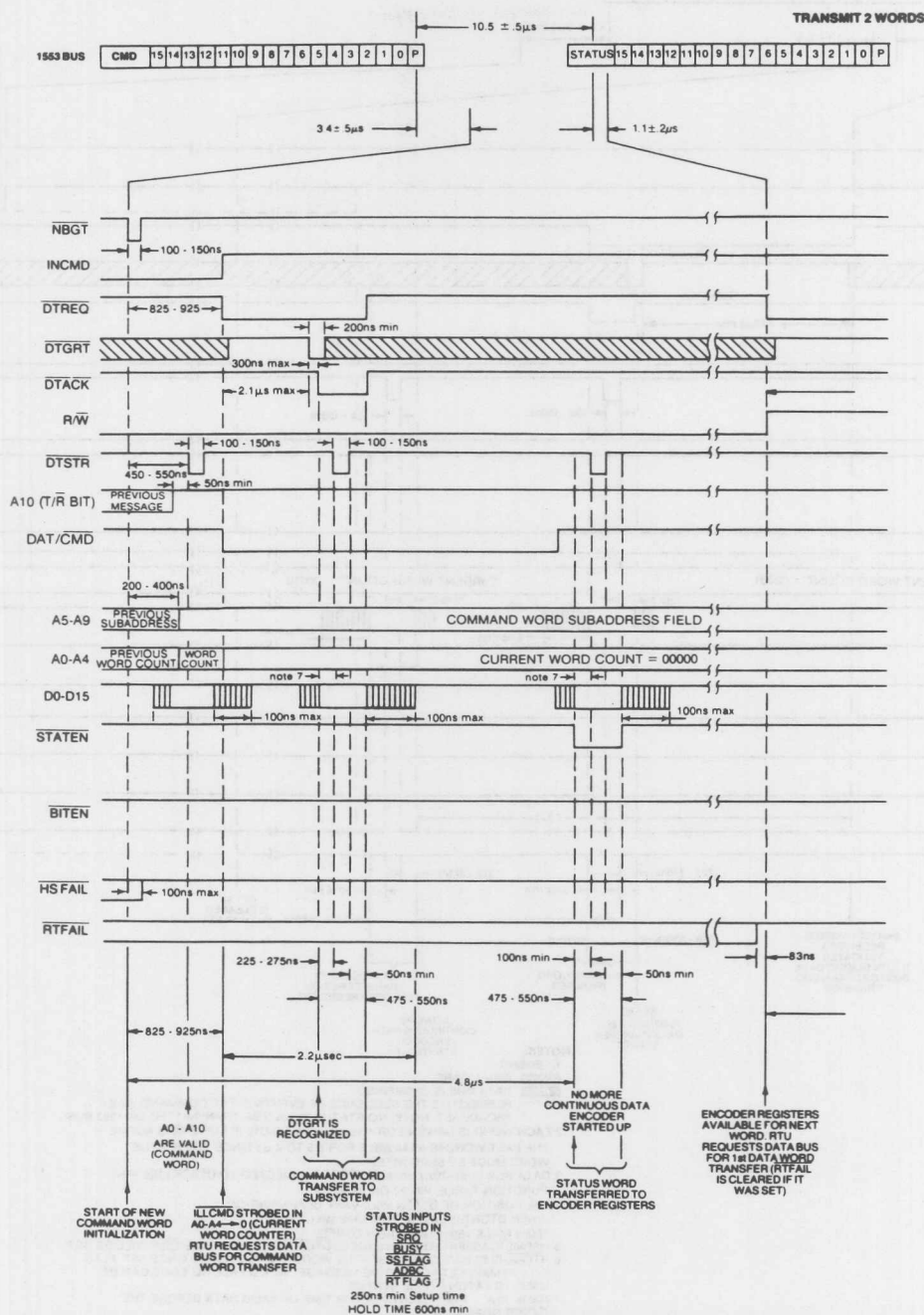
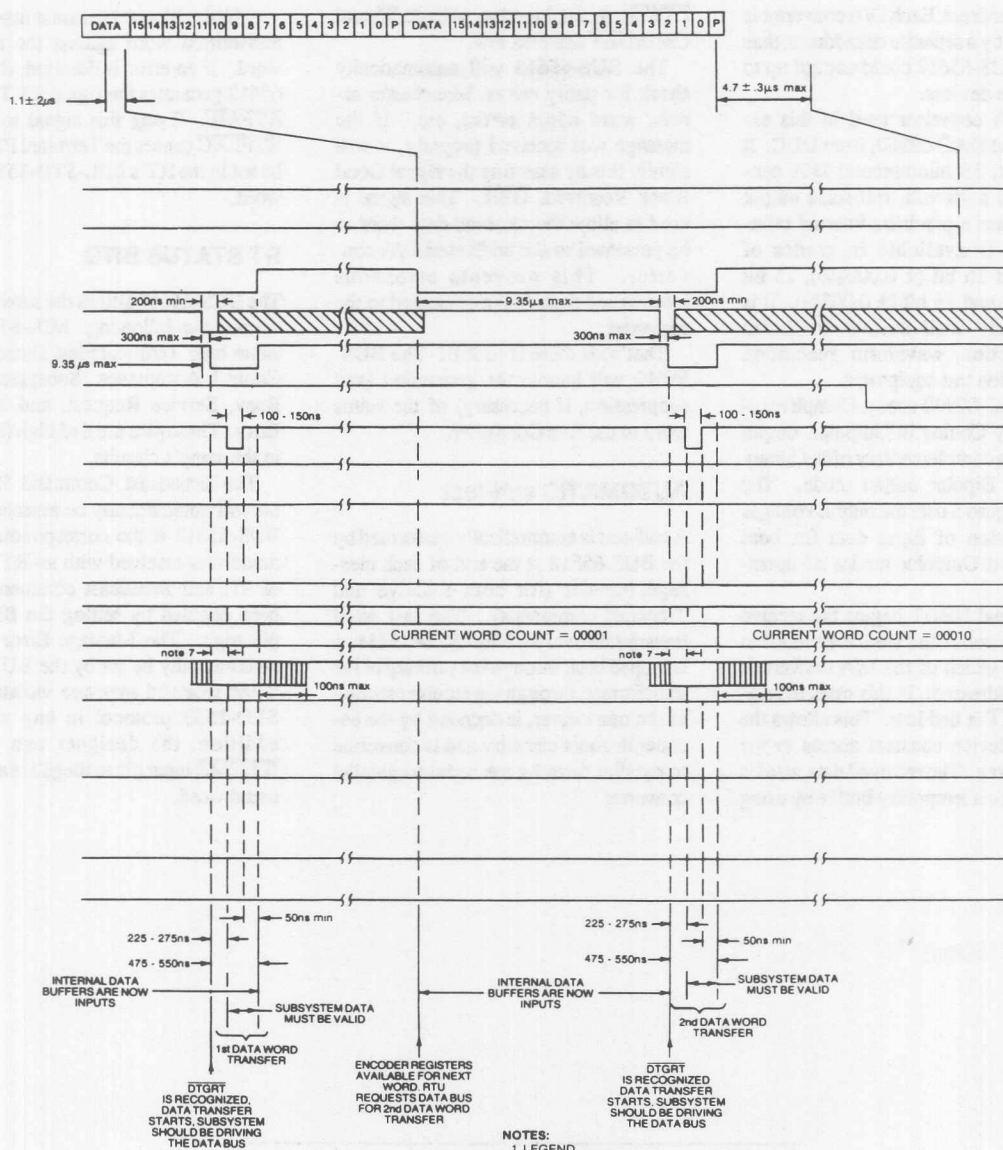



FIGURE 3. BUS-65612 RECEIVE TIMING







- NOTES:** THE DATABUS
1. **LEGEND**  
 DON'T CARE  
DATA BUS IS UNDEFINED
2. EACH WORD IS DRIVEN FOR  $t_{RD} = 18-19 \mu s$  ON D0-D15 IF  $\overline{BUEFEN_A}$  IS ACTIVE - THE LAST WORD IS AVAILABLE FOR 3.5 TO 4  $\mu s$  SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH  $\overline{BUEFEN_A}$  CONNECTED TO  $\overline{DTACK}$  (SEE PIN FUNCTION TABLE, PIN 67 ON PAGE 16)
4. THE POSITION OF  $\overline{DTACK}$  WILL VARY DEPENDING ON WHEN  $\overline{DTGRT}$  IS GIVEN. THE TIME WILL BE 100ns MIN & 150ns MAX FROM  $\overline{DTREQ}$
5.  $\overline{HSFALL}$  IS ASSERTED UPON EXCESS  $\overline{DTGRT}$  RESPONSE TIME. INCMD WILL SUBSEQUENTLY GO LOW AND NO FURTHER WORD TRANSFERS WILL OCCUR
6.  $\overline{RTFALL}$  IS CLEARED UPON STATUS WORD TRANSMISSION. ONCE SET, FLAG WILL REMAIN SET FOR ENTIRE MESSAGE. INCMD FALLING EDGE CAN BE USED TO LATCH  $\overline{RTFALL}$  STATUS.
7. 100ns min - REPRESENTS SETUP TIME OF VALID DATA BEFORE THE  $\overline{DTSRB}$  GOES LOW FOR A WRITE CYCLE. A READ CYCLE REQUIRES VALID DATA 150ns MAX AFTER  $\overline{DTACK}$  GOES LOW

**FIGURE 4. BUS-65612 TRANSMIT TIMING**

unit's RT address. Each D/A converter is controlled by a separate subaddress, thus a single BUS-65612 could control up to 30 separate devices.

The D/A converter used in this example is the DAC-02900, from DDC. It is a 16 bit, 15 microsecond D/A converter with a 10 volt, full scale output range. It has a precision internal reference and is available in grades of linearity of 16 bit ( $\pm 0.0008\%$ ), 15 bit ( $0.0015\%$ ) and 14 bit ( $\pm 0.003\%$ ). It is particularly well suited for audio reconstruction, waveform generation and precision test equipment.

The DAC-02900 uses a Complementary Binary Coding in Unipolar output mode and a complementary offset binary coding in Bipolar output mode. The table in Figure 5 lists the output voltages as a function of input data for both Bipolar and Unipolar modes of operation.

The signal NBGT begins the receive cycle. The command word is decoded to determine which of the D/A converters is being addressed. In this case, the signal DTGRT is tied low. This allows the protocol device constant access to the data highway. The received data word is strobed into a temporary buffer by using

DTSTR in conjunction with R/W and CMD/DAT asserted low.

The BUS-65612 will automatically check for parity errors, Manchester errors, word count errors, etc. If the message was received properly, it will signify this by asserting the signal Good Block Received, GBR. This signal is used to allow the received data word to be presented to the addressed D/A converter. This prevents erroneous information from being presented to the converter.

That's all there is to it !!! The BUS-65612 will handle the generation (and suppression, if necessary) of the status word to the Bus Controller.

### AUTOMATIC self-test

A self-test is automatically performed by the BUS-65612 at the end of each message transfer (for both Receive and Transmit commands). The last word transmitted over the MIL-STD-1553 bus is looped back through the primary of the transformer, through the receiver section of the transceiver, is decoded by the encoder/decoder circuitry and is converted to parallel form by the serial to parallel converter.

A bit-by-bit comparison is made of the transmitted word against the received word. If an error is detected, the BUS-65612 generates the signal RT Test Fail, RTFAIL. Tying this signal to the pin RTFLAG causes the Terminal Flag bit to be set in the RT's MIL-STD-1553 status word.

### RT STATUS BITS

The BUS-65612 allows the subsystem to control the following MIL-STD-1553 status bits: Terminal Flag, Dynamic Bus Control Acceptance, Subsystem Flag, Busy, Service Request, and Message Error. These pins are tied high (inactive) in the sample circuits.

The Broadcast Command Received bit will automatically be asserted by the BUS-65612 if the corresponding command was received with an RT address of 31, and Broadcast commands have been enabled by setting the BROENA pin high. The Message Error bit will automatically be set by the BUS-65612 if the received message violates MIL-STD-1553 protocol in any way. In addition, the designer can use the ILLCMD input pin to illegalize any command word.

INPUT DATA CODING					
INPUT DATA				OUTPUT VOLTAGE	
				BIPOLAR	UNIPOLAR
00	0000	0000	000000	+4.99985	9.99985
01	1111	1111	111111	0.00000	5.00000
10	0000	0000	000000	-0.00015	4.99985
11	1111	1111	111111	-5.0000	0

FIGURE 5. PROGRAMMING TABLE FOR DAC-02900

## COMMAND ILLEGALIZATION

The BUS-65612 supports all dual redundant mode code commands defined by MIL-STD-1553, including Transmit Last Command Word, Transmit Last Status Word, Transmitter Shutdown, etc., without requiring any support from the subsystem.

In addition, the user can illegalize any command with the use of a single PROM. The Command word is simply used as the address inputs to the PROM. The Prom itself is constantly enabled. The output will only be sampled by the BUS-65612 at the appropriate point in the message transfer. (See the timing

diagrams for details.)

The corresponding data word is programmed by the user to a '0' if the command is to be allowed, and to an 'FF' if it is to be illegalized. The least significant data bit output is then connected to the ILLCMD pin of the BUS-65612. This causes the BUS-65612 to set the Message Error bit in the status word. No data will be transmitted.

## SAMPLE TRANSMIT CIRCUITRY

The BUS-65612 can be used just as easily in designs where the subsystem must

transmit data to the Bus Controller. One example would be a Synchro to Digital converter, where the subsystem's function is to monitor flap position, and report it to the Bus Controller. Another example is using an LVDT converter to report velocity information to the Bus Controller.

The circuit shown in Figure 6 illustrates a method of interfacing a synchro converter and an LVDT to the MIL-STD-1553 bus without requiring the use of a microprocessor. Each is controlled via a separate subaddress. Upon command from the Bus Controller, it will transmit the latest value from the addressed converter.

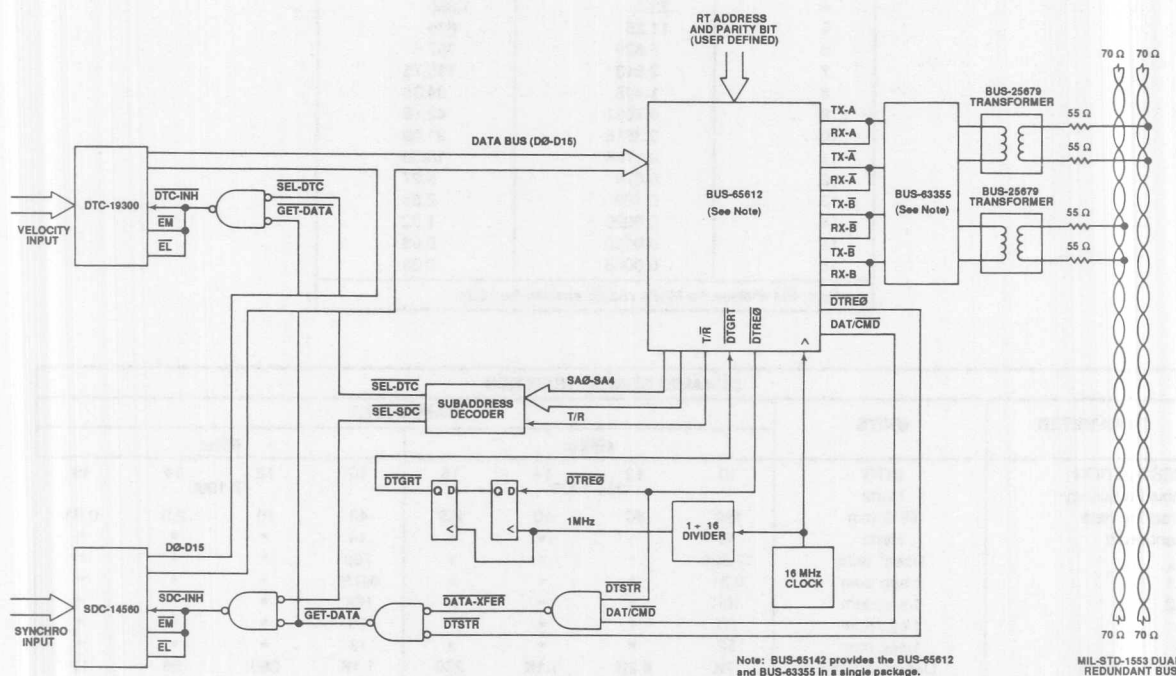


FIGURE 6. SAMPLE TRANSMIT CIRCUIT

## S/D CONVERTER

The S/D converter used in this example is the SDC-14560 from DDC. It offers programmable resolution of 10, 12, 14, or 16 bits coupled with the fast tracking of a 10 bit device. See the programming information detailed in Figure 7. For this application we will use 16 bit resolution.

## LVDT CONVERTER

The LVDT converter used in this example is the DTC-19300 Linear Variable Differential Transformer to digital converter from DDC. The converter's reference voltage is derived from, and is

in phase with, the LVDT output signal. The DTC-19300 can be programmed to accommodate the broadest range of LVDT's available. (See the table in Figure 8.) An analog velocity voltage is a standard output. This signal is a DC level proportional to the core's linear rate of change, and can be used for velocity feedback.

## INTERFACING TO THE CONVERTERS

Both converters provide the digital output as separate tristatable bytes. The most significant and least significant bytes are enabled with the signals  $\overline{EM}$

and  $\overline{EL}$ , respectively. The signal  $\overline{INH}$  locks the output transparent latch so the bits will remain stable while data is being transferred. The output is stable 0.5 microsecond after  $\overline{INH}$  is driven to a logic 0. See the timing diagram shown in Figure 9.

In the example circuit shown in Figure 6, both  $\overline{EM}$  and  $\overline{EL}$  are enabled when the particular converted is selected. This allows a full 16 bits to be transferred in one operation.

Upon detection of a command containing the circuit's RT address, the BUS-65612 asserts the signal  $\overline{NBGT}$ . The command is decoded to determine which of the converters is being addressed. (Note: since this application is

DIGITAL ANGLE OUTPUTS		
BIT	DEG/BIT	MIN/BIT
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	387.5
7	2.813	168.75
8	1.405	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.879	5.27
13	0.439	2.64
14	0.0220	1.32
15	0.0110	0.66
16	0.0055	0.33

Note:  $\overline{EM}$  enables the MSBs and  $\overline{EL}$  enables the LSBs.

DYNAMIC CHARACTERISTICS								
PARAMETER	UNITS	BANDWIDTH						
		400Hz				60Hz		
RESOLUTION	BITS	10	12	14	16	10	12	14
Input Frequency	Hertz	360-1000				47-1000		
Tracking Rate	RPS min	160	40	10	2.5	40	10	2.5
Bandwidth	Hertz	54	*	*	*	14	*	*
$K_a$	1/sec <sup>2</sup> nom	12,500	*	*	*	780	*	*
A1	1/sec nom	0.31	*	*	*	0.078	*	*
A2	1/sec nom	40K	*	*	*	10K	*	*
A	1/sec nom	112	*	*	*	28	*	*
B	1/sec nom	52	*	*	*	13	*	*
acc-1 LSB lag	Deg/sec <sup>2</sup> nom	17K	4.2K	1.1K	260	1.1K	260	66
Settling Time	ms max	90	90	150	350	350	360	600

Note: \* means same as value to the left.

FIGURE 7. PROGRAMMING INFORMATION FOR SDC-14560

only supporting Transmit commands, the T/R must be a logic 1 to enable the converters.)

The signal DTREQ, in conjunction with the R/W and DAT/CMD signals asserted high, is used to generate the INH input to the addressed converter. The signal DTGRT is not tied low as it is in the sample Receive circuitry. It is generated by using the DTREQ signal as an input to a "D" type flip-flop clocked at a 1 MHz rate. The output of this flip-flop is connected to the DTGRT pin of the BUS-65612. This allows the output of the converter time to settle before it is presented to the BUS-65612.

That's it!! As previously discussed, the BUS-65612 handles all protocol related issues, such as the generation or suppression of the status word, mode code commands, dual redundant bus operation, self-test, etc. If desired, the

Built-In-Test output of the converters can be connected to SSFLAG pin of the BUS-65612. This will cause the subsystem flag bit to be set in the RT's status word should one of the converters detect a problem.

## BOARD SPACE

Interfacing the BUS-65612 to the MIL-STD-1553 simply requires a dual transceiver, 2 transformers and 2 55-ohm isolation resistors. Board space can be saved by selecting the new 24 pin dual transceiver from DDC, the BUS-63355. This new device occupies a mere 0.97 square inches, as opposed to the 1.55 square inches required for the 36 pin transceivers typically used. The required board space can be reduced even further with the selection of the BUS-65142 from DDC. This new component util-

izes hybrid processing technology to combine the BUS-65612 die with a dual transceiver. The result is a 78 pin, 1.9 by 2.1 inch package. With the addition of a 16 MHz clock, two transformers and the two 55-ohm isolation resistors, the MIL-STD-1553 interface is complete.

## CONCLUSION

The BUS-65612 opens up a new category of devices which can be economically controlled over the MIL-STD-1553 bus. By incorporating full protocol handling with a non-register based architecture, the BUS-65612 and BUS-65142 allow minimal complexity devices to be interfaced to the MIL-STD-1553 bus without requiring the use of a microprocessor. Contact ILC Data Device Corporation for complete information on these products.

DIGITAL OUTPUT CODES												
SCALE	(MSB)	DIGITAL OUTPUT										(LSB)
+FS – 1LSB	0	1	1	1	1	1	1	1	1	1	1	1
+HS	0	1	0	0	0	0	0	0	0	0	0	0
+1LSB	0	0	0	0	0	0	0	0	0	0	0	1
ZERO	0	0	0	0	0	0	0	0	0	0	0	0
– LSB	1	1	1	1	1	1	1	1	1	1	1	1
–HS	1	1	0	0	0	0	0	0	0	0	0	0
–FS	1	0	0	0	0	0	0	0	0	0	0	0

DTC-19300 full scale (FS) and half scale (HS) digital output codes.

BIT WEIGHTS	
BIT	WEIGHT
1 (MSB)	0.5 full range = FS
2	0.25 full range = HS
3	0.125 full range
4	0.0625 full range
5	0.03125 full range
6	0.015625 full range
7	0.0078125 full range
8	0.0039063 full range
9	0.0019531 full range
10	0.0009766 full range
11	0.0004833 full range
12	0.0002441 full range
13	0.0001221 full range
14 (LSB)	0.0000611 full range

The weight of each bit with respect to the full scale output.

FIGURE 8. PROGRAMMING INFORMATION FOR DTC-19300

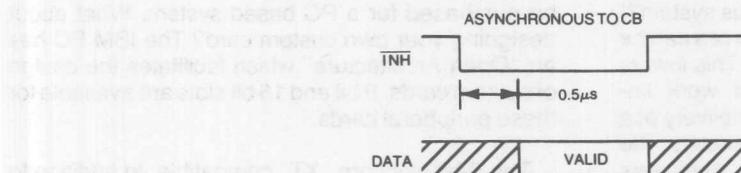


FIGURE 9. INHIBIT TIMING DIAGRAM FOR SDC-14560 & DTC-19300



## FACTORS TO CONSIDER WHEN USING A PC IN A MIL-STD-1553 ENVIRONMENT

### WHY USE A PC?

VME, MULTIBUS, UNIBUS - these are the systems that are typically considered when choosing a platform for 1553 development. However, it is well worth a system designer's time to consider the use of the IBM PC or compatible. One reason is the amount of software that is available for the PC. Just about any language, from assembler through Pascal and LISP can be hosted on a PC.

Another reason is the large number of interface cards that are available for the PC. There are cards available to allow the PC to communicate over Ethernet, IEEE-488 and VME busses, to name just a few. There are also cards already available to allow the PC to communicate over the 1553 bus.

But, you're asking yourself, "what makes the PC different to say, the Multibus system? Many of these same caveats can be equally well applied to an established system such as that one." One factor that allows the PC to stand out is the fact that it has so many other uses in an engineer's day. It can be used for word processing, electronic mail, etc.

### EFFICIENT USE OF COMPANY RESOURCES

In fact, it's quite possible that your engineers already have access to PC's - possible right on their desks. (Can you say that about a Multibus system?) This means that existing company resources can be used for the 1553 development activity. This lowers initial costs and allows you to begin work immediately, without having to wait for the delivery of a VME or Multibus system. It also reduces the problems associated with time-slicing engineers onto a scarce resource (such as a VME development system).

Another reason is that the PC comes in so many easily acquired configurations. Ruggedized versions are available, making the PC ideal for such applications as "suitcase" type testers. Single board versions are available to allow you to meet even more stringent packaging requirements.

A world of peripherals is available for the PC. The system designer can choose the graphics card which provides the best human interface for the particular application. This can vary from a standard monochrome character display, to a high resolution Enhanced Graphics Adapter (EGA) system, to a flat plasma display for highly portable systems. Software packages are available to allow the user to develop highly sophisticated graphic interfaces in a fraction of the time it would otherwise take.

A RAM disk architecture is supported by DOS 3.0 and higher. This feature allows you to simulate a disk drive with RAM. It dramatically decreases the time the PC spends performing data retrieval. (It's a lot faster to retrieve data from RAM than from a mechanical floppy or hard disk.) The PC's system memory can be used, or special purpose RAM disk cards can be purchased.

### MAKE vs. BUY DECISION

So far we've only talked about the options that can be purchased for a PC based system. What about designing your own custom card? The IBM PC has an "Open Architecture" which facilitates the design of custom cards. 8 bit and 16 bit slots are available for these peripheral cards.

The 8 bit slots are "XT" compatible. In addition to performing data transfers a byte at a time, these slots only decode address bits A0-A19. The 16 bit slots are

AT compatible, and they decode an extra 4 bits of addressing, from A0-A23. It is important that the system designer takes this into account when configuring the system. For instance, a board which decodes 20 bits of addressing that sits at address C000 will crash with a board which decodes 23 bits and sits at address 1C000. Many graphics boards are memory mapped only up to the 1Mbyte boundary, so the entire system, including purchased peripherals, must be carefully configured.

The use of the memory mapped architecture provided by the PC allows the user to simplify the software development and integration of the PC based system. A memory mapped card appears to the application program as RAM. Normal read/write statements can be used to access the card - no hardware driver is necessary.

This means that if there is a problem, there are only 2 variables: the board could be bad, or there is a problem with the user's application software. There's no mysterious piece of code sitting between the application code and the board. (To make things even more complicated, the driver is usually not written by the person who is writing the application program. It's often not even written by someone in the same company, and is usually written in assembly language. This makes it very difficult to debug the system.)

Another advantage of a memory mapped card is that application software can be written and tested without the card being installed. (Simply assign the starting address of the program to an existing area of system memory.) This allows the engineer to begin development while the custom card is still being designed, or while waiting for the card to be delivered from the vendor.

#### **EXAMPLE OF A MEMORY MAPPED PC TO 1553 INTERFACE CARD**

The BUS-65515 is an example of a memory mapped card that allows the PC to act as either a 1553 Bus Controller (BC), Remote Terminal Unit (RTU) or Bus Monitor (MT). Since it is memory mapped, the engineer utilizes normal read/write statements from Pascal, Fortran, even BASIC to load the 1553 messages into the board's onboard RAM.

The engineer loads either a stack or a Look Up table with the addresses of the messages. If the card has been programmed by the user to act as a BC, the engineer loads a message count into a reserved

word of the onboard RAM. The user issues a start command by setting a particular bit in another reserved word, and the 1553 transmission begins.

In BC mode, the board will automatically issue commands over the 1553 bus, and interrogate the response from the RTU. In RTU mode, it responds to commands containing the boards' user-programmed RTU address. The card automatically transfers data to/from the onboard RAM, without requiring any overhead from the CPU. Upon completion of a 1553 message, a user maskable interrupt is generated to the PC. Other interrupts are also available to inform the PC of extraordinary events, such as error conditions.

#### **INTERRUPT HANDLING**

An elegant feature of the PC is its interrupt handling capability. The PC utilizes the INTEL 8259A Programmable Interrupt Controller. It handles 8 interrupts, with IR0 having the highest priority. IR2 is typically used for specialized interface cards. The system designer defines the interrupt routine for the particular interrupt by loading it's starting address in the location 4\*Interrupt number.

The PC has reserved 6 of these interrupt levels for itself, leaving IR2 for the user. This is generally not a problem, as each interrupt line can support multiple devices. However, the interrupt handler must then poll each device sharing the interrupt to determine which unit requested service.

If this proves to be a hindrance for very time critical events, the user can take over one of the "reserved" interrupt lines. For instance, DOS uses a discrete interrupt to indicate that a key has been pressed on the keyboard. The user can take over this interrupt for the custom board, and poll the keyboard using the Real Time Clock interrupt. Since most engineers cannot type faster than 18.2 keystrokes a second (the polling rate using the real time clock), there will be no noticeable difference in the human interface.

#### **TYPICAL 1553 APPLICATION: ATE SYSTEM**

The availability of IEEE-488 interface cards, plus the computing power of the PC itself, makes the PC an ideal platform for 1553 ATE applications. An example of this is the BUS-69005 software package. This software, written in Turbo Pascal, generates and runs the RTU Production Test Plan (PTP). It characterizes the particular RTU through user friendly menus. Once the capability of the particular

RTU has been logged, the program automatically generates the IEEE commands necessary to run the RTU PTP. The user may run the entire test plan, or any subset. Low cost test equipment is used to implement the most economical solution.

Ruggedized, and portable PC's can be used to implement "suitcase" tester applications. A truly portable ATE system can be developed using a single board or portable PC and a 1553 interface card with error injection capabilities, such as the BUS-65517. This card can also be used in a full PC to simulate the entire 1553 bus.

## **TYPICAL 1553 APPLICATION: SIMULATION/TESTING**

The BUS-65517 allows the PC to simultaneously act as a 1553 BC, multiple RTU's and an intelligent 1553 message monitor. Error injection capability is supported in both BC and RTU modes. Each message may be programmed with a different type of error condition. These include bit and word count errors, response timing errors, no responses, Manchester, parity and encoding errors.

Thus, the user can simulate an entire 1553 system, using just one card and one PC. The board can also be used as a tester, to evaluate an external

BC or RTU. The intelligent message monitor re-constructs the 1553 traffic, indicating error conditions where applicable.

User friendly menus allow the engineer to quickly "get up and go" with the BUS-65517. The BUS-65517 is memory mapped, thus the application software can be run without the board being installed. This allows the user to become familiar with the system and begin development work while waiting for the card to be delivered.

## **CONCLUSION**

Due to the wealth of the software and hardware options that are available for the PC, it is well worth the system designer's time to consider the use of a PC in a 1553 application. The open architecture and interrupt handling available facilitates the use of custom cards. The use of memory mapping eases software development, test and interrogation. The availability of 1553 interface cards and software packages for the PC allows the system designer to mix and match available products with custom designed boards and software. The low cost of PC's reduces the problem of providing enough development tools for the project, as existing PC's can be used. Finally, the human interface can be tailored to utilize either highly sophisticated graphics, or simple monochrome screens, depending on what suits the particular application. The PC is definitely a contender for a MIL-STD-1553 CPU. ■

# APPLICATION NOTES

The following Application Notes are available. Send your request on company letterhead to:

**ILC Data Device Corporation**  
105 Wilbur Place  
Bohemia, N.Y. 11716

**Attention: Literature Department**

## MIL-STD-1553 DATA BUS:

Order Number	Title
AN/B-1	Designing a Remote Terminal to Talk with a MIL-STD-1553 Network.
AN/B-2	Manchester Coding Data Bus.
AN/B-3	MIL-STD-1553 B: Military Standard for Avionics Integration.
AN/B-5	MIL-STD-1553 Bus Monitor.
AN/B-6	Hybrid Trio Takes Charge of the Bus-to-CPU Interface in Military Avionics Gear.
AN/B-7	Avoiding Pitfalls in MIL-STD-1553 Transceivers.
AN/B-8	A Standard Local Network for Industrial Use.
AN/B-10	Monolithic/Superhybrids Support 1553 Interfaces.
AN/B-11	Low Cost Implementation of the SAE-AE9 RTU Production Test Plan.
AN/B-12	Test Whether a Noise Source is Gaussian.
AN/B-13	Hybrid modules help you implement a 1553B interface.
AN/B-14	Processor Interfaces To 1553 Buses.
AN/B-15	Streamline Your MIL-STD-1553 Design By Eliminating The CPU.
AN/B-16	A Systems Approach To MIL-STD-1553 Terminal Design.
AN/B-17	8088 Microprocessor To BUS-61553 Interface.

## LINEAR DATA CONVERTERS:

Order Number	Title
AN/L-3	Getting the Best from A-D Converters.
AN/L-7	Optimizing D/A Converter Performance.
AN/L-8	High Resolution A/D Works Better with Track-Hold.
AN/L-10	Mend Flash-Converter Flaws with a Track/Hold Cure.
AN/L-11	Watch for Superposition Errors in Data Converter Applications.
AN/L-12	A/D Simulation Programs Predicts Signal-to-Noise Ratio.
AN/L-13	Deglitched DACs Improve Vector-Stroke Displays.
AN/L-14	Fast Fourier Transform Speed Signal to Noise Analysis for A/D Converters.
AN/L-15	2-Step Conversion Increases ADC Speed.
AN/L-17	Design do's and don'ts polish 16-bit D/A performance.
AN/L-18	Histograms Simplify A/D Converter Testing.
AN/L-19	Spreadsheet Helps You Evaluate System Noise.
AN/L-20	Analog/Digital Dynamic Testing Of High-Speed A/D.
AN/L-21	Noise Power Ratio Characterizes A/D Performance For Communications.

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# **SYNCHRO CONVERTERS:**

Order Number	Title
AN/S-4	Consider Basic Parameters When Choosing S/D Converters.
AN/S-8	Shaft Position Encoders for Industrial Applications.
AN/S-12	Choosing the Right Encoder Simplifies Motor Control.
AN/S-14	A Reliable, Low Cost Approach to Shaft Position Control.
AN/S-16	Let a Modern R/D Converter Simplify Your Design Effort!
AN/S-18	Testing Of S/D Converters.

# **HYBRID PROCESSING:**

Order Number	Title
AN/QC-2	Certification Requirements for Hybrid Microcircuit Facilities.
AN/QC-5	Application and Use of Acceleration Factors in Microelectronics Testing.
AN/QC-6	Volume Resistivity Techniques for I-A Process Evaluation of Conductive Epoxies.
AN/QC-7	Recovering Precious Metal from Scrap Generated by the Hybrid Manufacturing Process.
AN/QC-8	Understanding Quality Conformance Inspection of Hybrid Microcircuits.
AN/QC-9	Effective Hybrid Process Controls on Assembly Operations.

# **POWER HYBRIDS:**

Order Number	Title
AN/H-1	Hybrids Take on Power.
AN/H-2	Custom Power Hybrids.



[REDACTED]

[REDACTED]

DESCRIPTION	QTY	UNIT PRICE	TOTAL
1. [REDACTED]	100	1.00	100.00
2. [REDACTED]	50	2.00	100.00
3. [REDACTED]	25	4.00	100.00
4. [REDACTED]	10	10.00	100.00
5. [REDACTED]	5	20.00	100.00
6. [REDACTED]	2	50.00	100.00
7. [REDACTED]	1	100.00	100.00
8. [REDACTED]	1	100.00	100.00
9. [REDACTED]	1	100.00	100.00
10. [REDACTED]	1	100.00	100.00
11. [REDACTED]	1	100.00	100.00
12. [REDACTED]	1	100.00	100.00
13. [REDACTED]	1	100.00	100.00
14. [REDACTED]	1	100.00	100.00
15. [REDACTED]	1	100.00	100.00
16. [REDACTED]	1	100.00	100.00
17. [REDACTED]	1	100.00	100.00
18. [REDACTED]	1	100.00	100.00
19. [REDACTED]	1	100.00	100.00
20. [REDACTED]	1	100.00	100.00
21. [REDACTED]	1	100.00	100.00
22. [REDACTED]	1	100.00	100.00
23. [REDACTED]	1	100.00	100.00
24. [REDACTED]	1	100.00	100.00
25. [REDACTED]	1	100.00	100.00
26. [REDACTED]	1	100.00	100.00
27. [REDACTED]	1	100.00	100.00
28. [REDACTED]	1	100.00	100.00
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30. [REDACTED]	1	100.00	100.00
31. [REDACTED]	1	100.00	100.00
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33. [REDACTED]	1	100.00	100.00
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59. [REDACTED]	1	100.00	100.00
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63. [REDACTED]	1	100.00	100.00
64. [REDACTED]	1	100.00	100.00
65. [REDACTED]	1	100.00	100.00
66. [REDACTED]	1	100.00	100.00
67. [REDACTED]	1	100.00	100.00
68. [REDACTED]	1	100.00	100.00
69. [REDACTED]	1	100.00	100.00
70. [REDACTED]	1	100.00	100.00
71. [REDACTED]	1	100.00	100.00
72. [REDACTED]	1	100.00	100.00
73. [REDACTED]	1	100.00	100.00
74. [REDACTED]	1	100.00	100.00
75. [REDACTED]	1	100.00	100.00
76. [REDACTED]	1	100.00	100.00
77. [REDACTED]	1	100.00	100.00
78. [REDACTED]	1	100.00	100.00
79. [REDACTED]	1	100.00	100.00
80. [REDACTED]	1	100.00	100.00
81. [REDACTED]	1	100.00	100.00
82. [REDACTED]	1	100.00	100.00
83. [REDACTED]	1	100.00	100.00
84. [REDACTED]	1	100.00	100.00
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87. [REDACTED]	1	100.00	100.00
88. [REDACTED]	1	100.00	100.00
89. [REDACTED]	1	100.00	100.00
90. [REDACTED]	1	100.00	100.00
91. [REDACTED]	1	100.00	100.00
92. [REDACTED]	1	100.00	100.00
93. [REDACTED]	1	100.00	100.00
94. [REDACTED]	1	100.00	100.00
95. [REDACTED]	1	100.00	100.00
96. [REDACTED]	1	100.00	100.00
97. [REDACTED]	1	100.00	100.00
98. [REDACTED]	1	100.00	100.00
99. [REDACTED]	1	100.00	100.00
100. [REDACTED]	1	100.00	100.00

[REDACTED]

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# 1553 DATA BUS PRODUCTS

## • TRANSCEIVERS - Single

MODEL	TYPE	PACKAGE	DESCRIPTION/FEATURES
BUS-8553	Transceiver	24 Pin DDIP Hybrid 1.4x0.8x0.20"	Featuring low power dissipation and improved filtering to enhance bit error rate of system. Directly interfaces to Harris 15530 Encoder/Decoder.
BUS-63102 II	Universal Transceiver	1.26 x 1.26 x 0.17" Hybrid	Universal transceiver conforms to MIL-STD-1553 A/B and McDonnell Douglas A-3818, A-5232, A-4905, and A-5690.
BUS-63104 II	Transceiver	1.26 x 1.26 x 0.17" Hybrid	Conforms to MIL-STD-1553 A/B. Improved filtering to enhance bit error rate.
BUS-63105II(-15V) BUS-63107II(-12V)	Transceiver	24 Pin DDIP Hybrid 1.4 x 0.8 x 0.20"	Monolithic Transceiver. Listed on MIL.DWG.No.5962-86049-02XC. Conforms to MIL-STD-1553 A/B. High S/N ratio, internal filtering. Drives Harris 15530 directly. SEAFAC tested. Eliminates non-standard part approval when specified by the Military Drawing number.
BUS-63115 II BUS-63117 II			Same as BUS-63105 II but has inverted RX and $\overline{RX}$ outputs. Same as BUS-63107 II but has inverted RX and $\overline{RX}$ outputs.

## • TRANSCEIVERS - Dual

BUS-63125II(-15V) BUS-63127II(-12V)	Dual Transceiver	36 Pin DDIP Hybrid 1.9 x 0.78 x 0.2"	Dual redundant monolithic transceivers in a single hybrid. Conforms to MIL-STD-1553 A/B. High S/N ratio, internal filtering. Drives Harris 15530 directly. Complete isolation, including separate power and signal connections. SEAFAC tested. Eliminates non-standard part approval when specified by the MIL. DWG. No. 5962-87579-02XC.
BUS-63135 II BUS-63137 II			Same as BUS-63125 II but has inverted RX and $\overline{RX}$ outputs. Same as BUS-63127 II but has inverted RX and $\overline{RX}$ outputs.
BUS-63147 BUS-63148	Dual 5V Transceiver	36 Pin DDIP Hybrid 1.9 x 7.6 x 0.210"	Complete transmitter and receiver pair conforming fully to MIL-STD-1553 A/B. Features + 5V power supply, Dual Redundant packaging, and Harris I/O compatibility. BUS-63148 is BUS-65612 compatible. DESC #5962-89522
BUS-63355 BUS-63357	Dual Transceiver	24 Pin DDIP Hybrid 1.31 x 0.80 x 0.17"	Smallest MIL-STD-1553A/B dual redundant monolithic low power transceiver which is designed to be directly compatible with the BUS-65612 DDC protocol. BUS-63355 is -15V and BUS-63357 is -12V power supply option.

## • COMPLETE TERMINALS

BUS-61553(-15V) SERIES BUS-61554(-12V) BUS-61555(+ 5V)	Advanced Integrated MUX (AIM) Hybrid AIM-HY	2.1 x 1.9 x 0.25" (DDIP)	Complete MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU), or Bus Monitor (MT) device. Contains dual low power transceivers, complete BC/RTU/MT protocol logic, MIL-STD-1553-to-host interface unit, and an 8K x 16 shared RAM. Provides memory mapped 1553 interface, on-line and off-line Self Test, and is SEAFAC Tested. Eliminates non-standard part approval when specified by the MIL. DWG No. 5962-88692-01XC.
BUS-61556(-15V) BUS-61563(-15V) BUS-61564(-12V) BUS-61565(+ 5V)		2.2 x 1.6 x 0.17" (Flatpack)	Same as above but it is transceiverless and is used with BUS-63102 II. Flatpack version of BUS-61553. Flatpack version of BUS-61554. Flatpack version of BUS-61555.
BUS-61559	Advanced Integrated MUX (AIM) Hybrid AIM-HY	2.1 x 1.9 x 0.25" (DDIP) 2.2 x 1.6 x 0.17" (Flatpack)	Complete MIL-STD-1553B Notice 2 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT) device. Supports STANAG-3910 and provides a direct interface to SEL's RT3910 high-speed protocol (STANAG-3910) unit. Pin, functional, and software compatible to BUS-61553 Series including data and address buffers selection, Subaddress Memory Management, and additional interrupts. BUS-61569 is Flatpack version.
BUS-65110(-15V) BUS-65111(-12V)	Dual Redundant RTU	1.9 x 2.1 x 0.25" (DDIP)	Complete dual redundant RTU package in either DDIP or Flatpack hybrid packages. Includes two low power Mark II transceivers, two encoder/decoders, two bit processors, RTU protocol, data buffers, timing control logic, supports 13 mode codes, and is a pin-for-pin and Functional BUS-65112 Replacement. BUS-65111 listed on MIL.DWG.No.5962-87632.
BUS-65120(-15V) BUS-65121(-12V)		1.6 x 2.2 x 0.17" (Flatpack)	

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

Data Bus Products continued.

## 1553 DATA BUS PRODUCTS

(continued)

• COMPLETE TERMINALS – continued			
MODEL	TYPE	PACKAGE	DESCRIPTION/FEATURES
BUS-65112	Dual Redundant RTU	2.1 x 1.9 x 0.25" (DDIP)	MIL-STD-1553 dual redundant RTU includes transceivers, encoder/decoder and protocol. Supports 13 mode codes and has DMA type interface handshake. SEAFAC tested. Eliminated non-standard part approval when specified by the Military Drawing number (DESC) 5962-87535-01XC
BUS-65117		2.2 x 1.6 x 0.17" (Flatpack) Hybrid	
BUS-65142	Dual Redundant RTU	1.9 x 2.1 x 0.25" (DDIP)	Complete dual redundant RTU package in either DDIP or Flatpack hybrid packages. Includes CMOS-SOS Monolithic RTU protocol and BiPolar low power Mark II transceivers, data buffers, timing control logic, supports mode codes, 16MHz decoders that offer improved noise rejection and zero crossing detection, and has SEAFAC tested components.
BUS-65144		1.6 x 2.2 x 0.17" (Flatpack)	
BUS-65600	Dual Redundant Bus Controller, Remote Terminal, or Bus Monitor	2.1 x 1.9 x 0.25" (78 Pin DDIP) 2.2 x 1.6 x 0.17" (82 Pin Flatpack)	Dual Redundant Bus Controller, Remote Terminal Unit, or Bus Monitor. Supports all -1553 mode codes, selective mode code illegalization available, complete error detection capability is provided for both BC and RTU operation, has 16 bit microprocessor compatibility, uses DMA handshaking for subsystem message transfers, and has continuous on-line built-in-test. DESC DWG # 5962-88585-01XC. (12MHz clock operation)
BUS-65612	Bus Controller, Remote Terminal, or Bus Monitor	1.32 x 1.32 x 0.125" (PGA)	Pin grid array (BUS-65612). Dual redundant MIL-STD-1553 Bus Controller, Monitor or RTU hybrid with error detection and complete mode code capability. Includes 16MHz dual encoder/decoder, dual bit processor, RTU protocol, BC protocol and DMA subsystem interface.
BUS-66300 II	1750 or STD CPU Interface	2.1 x 1.9 x 0.25" (78 Pin DDIP)	Single chip hybrid. Also available in pin grid array package (BUS-66312). Interfaces STD or 1750 CPUs (F9450 or PACE 1750A) and 1553 BC/RTUs (BUS-65600 and BUS-65612) for minimum CPU overhead; internal microcode controller; buffer controls for 1750 address bus and data bus; registers for command, interrupt and mode control words. DESC DWG # 5962-88586-01XC
BUS-66312		2.2 x 1.6 x 0.17" (Flatpack) 1.32 x 1.32 x 0.125" (PGA)	
• CARD ASSEMBLIES			
BUS-65505 (-12V) BUS-65506 (-15V)	Unibus Bus Controller, Remote Terminal or Bus Monitor	15.6 x 8.4" Unibus Hex Card	Dual redundant Bus Controller Remote Terminal Unit, or Bus Monitor with Unibus ® interface. Supports all MIL-STD-1553 message formats, 12 Mode Codes, and provides Built-in-test capability. Its 4K x 16 bit dual access RAM and command registers minimize CPU overhead.
BUS-65508 (-15V) BUS-65509 (-12V)	Multibus I Bus Controller, Remote Terminal or Bus Monitor	6.75 x 12" Multibus ® Card	Dual redundant Bus Controller, Remote Terminal, or Bus Monitor with Multibus ® interface. Supports all MIL-STD-1553 message formats; 12 Mode Codes, and provides built-in-test capability. Its 4K x 16 bit dual access RAM and command registers minimize CPU overhead.
BUS-65512	Q-bus Bus Controller, Remote Terminal or Bus Monitor	8.43x10.5x0.44" Printed Circuit Card	Dual redundant Bus Controller, Remote Terminal, or Bus Monitor with Q-bus ® interface. Supports all MIL-STD-1553B message formats, mode codes, and provides built-in-test capability. Its on-board 8K x 16 memory, data transfers, and vectored interrupts with priority level selection minimize CPU overhead.
BUS-65515	IBM PC® Bus Controller or Remote Terminal	13.125 x 4.9" IBM PC Card	Dual redundant Bus Controller, Remote Terminal Unit, or Bus Monitor with IBM PC interface. Supports all MIL-STD-1553 message formats, 13 mode codes, and provides built-in-test capability. Its 4K x 16 bit dual access RAM and command registers minimize CPU overhead.
BUS-65517 (PC) BUS-65517 II (AT)	IBM PC Card for Test and Simulation	13.125 x 4.6" IBM PC Card	Simultaneously simulates a Bus Controller, and active Monitor and up to 31 Remote Terminals. Provides comprehensive Error injection with Bit/Word resolution. Fully dual redundant. Includes user friendly menu driven software.
BUS-65522 BUS-65523	VME/VXI Bus Controller, Remote Terminal or Bus Monitor	9.2 x 6.3 x 0.4" VME Eurocard	Dual redundant Bus Controller, Remote Terminal Unit, or Bus Monitor with VME/VXI interface. Supports all MIL-STD-1553 message formats, mode codes, and provides built-in-test capability. Its 8K x 16 dual access RAM and four types of interrupts minimize CPU overhead. BUS-65523 is McAir option.

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

Data Bus Products continued.

® Multibus is a registered trademark of Intel Corporation.

® IBM XT/AT is a registered trademark of International Business Machines

® Unibus and Q-bus are a registered trademarks of Digital Equipment Corporation.

## 1553 DATA BUS PRODUCTS

(continued )

● <i>CARD ASSEMBLIES - continued</i>			
MODEL	TYPE	PACKAGE	DESCRIPTION/FEATURES
BUS-65555	MIL-STD-1553 RTU/BC/MT interface unit for GRiD <sup>®</sup> laptop	GRiD internal battery cartridge 2.9 x 1.45 x 5.5" Module	Full, intelligent interfacing between MIL-STD-1553B Data Bus and the rugged GRiD 1520, 1530, and 1535 series laptop XT/AT <sup>®</sup> compatible computers. Software controls operation as either a 1553 Bus Controller (BC), Remote Terminal Unit (RTU), or Bus Monitor (MT). It offers the Dual 1553 ports through standard 1553 triaxial connectors.
BUS-69007 BUS-69008 BUS-69009	Software upgrades for BUS-65517	Flexible Disk	BUS-69007 is a MIL-STD-1553A Response Time Software package that allows the BUS-65517 to emulate multiple (up to 31) MIL-STD-1553A RTs. BUS-69008 is Real Time Software package that allows direct BUS-65517 control through Microsoft C and Turbo Pascal.
● <i>TERMINAL BIT PROCESSORS, DUMB RTU'S, and MCE SMITHS</i>			
BUS-64100 II	Bit Processor	1.15 x 2.15 x 0.2" Hybrid	LSI based Manchester II encoder/decoder. Wrap-around self-test, 16 bit parallel tri-state output, mode codes, address recognition, time out.
BUS-65101 II BUS-65102 II BUS-65201 II	Dumb RTU (1553 and MACAIR)	1.8 x 1.6 x 0.2" Hybrid	MIL-STD-1553 dumb RTU with transceiver, encoder/decoder, control logic dual rank I/O registers, and internal clock oscillator. Provides all interface functions between the Data Bus and a subsystem parallel data highway. May operate as an RTU, BC or Bus Monitor, in either single or dual redundant configurations. SEAFAC tested.
MT32017 MT32018	RTU LSI Chip Set MCE Smiths	DIP, FP and LCC 2.5 x .910 x 0.25" 2.5 x .625 x 0.20"	A complete (less transceivers) dual redundant RTU implemented in 3 packages. Conforms to MIL-STD-1553B and features all mode codes, wrap around self test and a 32 word by 16 bit FIFO. The MT32018 is an encoder/decoder.
● <i>TESTERS</i>			
BUS-68005	Data Bus Exerciser	17 x 14.5 x 3.5" Instrument	Enhanced version of BUS-68003; provides full function simulation of RTU and BC operation; implements protocol test of SAE AE-9 proposed production test plan; has 1553 A/B System Tests; Real-Time Monitor output; programmable transmitter output level and channel A/B selection; can do superceding command test; error generation/detection; RS-232 and GPIB-488 external control.
BUS-68010	Data Bus Tester	8.5 x 3.5 x 9.3" Instrument	Low cost, bench top error generating and detecting instrument for functional testing of MIL-STD-1553 Data Bus systems. Operational as Bus Controller, Remote Terminal and Bus Monitor.
BUS-68015	Noise Tester	8.25 x 14.5 x 3.5"	Programmable bit error rate tester; self contained Bus Controller and noise source which correlates with SEAFAC; auto self test & diagnostics. Programmable via IEEE 488; pass/fail or continuous run.
BUS-69005	MIL-STD-1553 Test Software	Flexible Disk	Used with the BUS-68005 Data Bus Tester, BUS-68015 Noise Tester and an IBM PC/XT/AT to perform all protocol tests specified in the SAE AE-9 RTU Production Test Plan. Menu-driven complete/partial PTP execution; disk storage of PTP-subset and RTU configurations; single, continuous and Halt-on-Error execution. Selectable test data printout.
BUS-69006	MIL-STD-1553 Test Software	Flexible Disk	Provides a menu-driver ATE environment using an IBM PC/XT/AT host along with two of DDC's BUS-68005 Data Bus Exerciser to perform all protocol tests specified in the SAE RTU Production Test.
● <i>SPECIAL TEST EQUIPMENT</i>			
BUS-8559	Var. Output Transceiver	24 Pin DDIP Hybrid 1.4 x 0.8 x 0.20"	Conforms to MIL-STD-1553 A/B. Has variable output level for use in test applications. Receiver has internal filtering for high S/N ratio.
BUS-1555	Manchester II decoder	Encapsulated Module 3.1 x 2.6 x 0.8"	Decodes serial Manchester into 16 bit parallel and NRZ serial data output. Error detection capability.(16MHz clock operation)
BUS-1556	MIL-STD-1553 Encoder	Encapsulated Module 3.1 x 2.6 x 0.8"	Encodes parallel data into Manchester. Errors include: Manchester coding, parity, high and low bit count, and sync field.(2MHz clock operation)

NOTES: Most hybrid products are available with Military Processing (Contact Factory).  
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Data Bus Products continued.



## 1553 DATA BUS PRODUCTS

(continued)

• SEMS			
MODEL	TYPE	PACKAGE	DESCRIPTION/FEATURES
BUS-67001(UKT) BUS-67002(UKU) BUS-67003(UKS) BUS-67007	SEM Family	ISEM 2A Format B  Format E	Family of SEM modules to configure dumb RTU, complete RTU or Bus Controller.  A complete MIL-STD-1553 & 1750A computer I/O, RT/BC/MT mode selectable, with on board shared ram support. L.E.D.'s indicate the board activity and status.
BUS-25679 BUS-27765 BUS-29854 BUS-41429 B-2396	Isolation Transformers	0.63 x 0.63 x 0.3" Module	Provides all of the turns ratio configurations, component isolation, and common mode rejection ratio characteristics necessary for MIL-STD-1553 A/B. Low profile, modular units that are multitapped to accommodate existing system configurations.
• TRANSFORMERS			
B-2200/2300 Series*	Interface Transformers (BETA) *see footnote	0.63 x 0.63 x 0.3" or 0.5 x 0.35 x 0.25" Modules	Interface transformers listed on DESC Spec. No. M21038/27. Designed to couple MIL-STD-1553 A/B compatible drivers to the bus. Low profile devices multi-tapped to accommodate existing system configurations. Eliminates non-standard part approval when specified by the Military Drawing number. Listed on QPL-21032-31 from BETA transformers.

## ANALOG TO DIGITAL (A/D) CONVERTERS

MODEL	RESOLUTION	CONVERSION TIME	LINEARITY ERROR	PACKAGE	OPERATING TEMP. RANGE	POWER DISSIPATION	DESCRIPTION/FEATURES
ADC-00110 ADC-00012	12 Bit	100 nsec	± 0.025% FSR	46 Pin Plug-in Hybrid 1.6X2.4X0.2"	-55°C to + 125°C	7W	10 MHz word rate, containing T/H, A/D converter, data registers, Tri-State output registers, and timing circuits.
ADC-00115	12 Bit	200 nsec	± 1/2 LSB	5.0 x 5.43X0.5" Card	0°C to + 70°C	7.25 W	5 MHz word rate, containing T/H, A/D converter, data registers, Tri-State output registers, and timing circuits. Pin-for-pin low power MOD-1205 replacement.
ADC-00300 ADC-00302	12 Bit	500 nsec	± 0.012% FSR	40 Pin TDIP 40 Pin Flatpack 1.2X2.2X0.25"	-55°C to + 125°C	3W	2MHz word rate; includes T/H and all timing circuits. Very high speed.
ADC-00305	12 Bit	500 nsec	± 0.012% FSR	40 Pin TDIP Hybrid	0°C to + 70°C	2.6W	2 MHz word rate; containing T/H, A/D converter, Tri-State output registers, and timing circuits. Low cost.
ADC-00403 ADC-00404	12 Bit	2µsec	± 1/2 LSB	32 Pin TDIP 1.14X1.93X0.2"	-55°C to + 125°C	2.4W	High-speed, pin-for-pin replacement for ADC87 and ADC85. Military applications. Hermetic seal.

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

\* Order B-2200/2300 Series directly from Beta Transformers Technology Corporation

1 Comac Loop, Ronkonkoma, N. Y. 11779. (516) 588-2505



## DIGITAL TO ANALOG (D/A) CONVERTERS

MODEL	RESOLUTION	F.S. SETTLING TIME		LINEARITY ERROR	PACKAGE	OPERATING TEMP. RANGE	POWER DISSIPATION	DESCRIPTION/FEATURES
		VOLTAGE	CURRENT					
ADH-030 II	12 Bit	—	35 nsec	$\pm 1/2\text{LSB}$	24 Pin DDIP Hybrid 1.4x0.8x0.2"	-55°C to +125°C	1.2 W	Low glitch energy 2.5mA · nsec . One monolithic active component. Very fast settling. ECL
DAC-02306 DAC-02307	14 Bit	— 350ns	50 nsec —	$\pm 0.01\%$ F.S.R.	24 Pin DDIP Hybrid 1.4x0.8x0.2"	-55°C to +125°C	1.8W	14 bit latched DAC with fast settling voltage output. Pin programmable output voltage, with trimmable gain and offset.
DAC-02310 DAC-02311	14 Bit	1.5μsec	—	$\pm 0.01\%$ F.S.R.	32 Pin TDIP 1.16x1.75x0.21" 32 Pin Flatpack 1.10x1.8x0.18"	-55°C to +125°C	1.7W	14 bit deglitched D/A converter with 10MHz update rate, pin programmable output ranges and 50mV · nsec differential glitch energy.
DAC-02315 DGL-02316	12 Bit	35ns	—	$\pm 0.01\%$ F.S.R.	24 Pin DDIP Hybrids 1.4x0.8x0.2"	-55°C to +125°C	3.3W	Deglitching D/A converter with 35 MHz update. 14mV PP glitch and 38ns glitch duration.

## SAMPLE/HOLD and TRACK/HOLD AMPLIFIERS

MODEL	ACQUISITION TIME (F.S.CHANGE)	LINEARITY ERROR	PACKAGE	APERTURE JITTER	SMALL SIGNAL BANDWIDTH	DROOP RATE	OPERATING TEMP. RANGE	POWER DISSIPATION	DESCRIPTION/FEATURES
TH-8530	10 nsec	$\pm 0.012\%$ F.S.R.	24 Pin DDIP Hybrid 1.4x0.8x0.2"	20psec	100MHz typ	1.0m V/μs	-55°C to +125°C	1.9W	Includes buffer amplifier, 50 MHz sample rate. -60db feedthrough.
THA-05203	150 nsec	$\pm 0.0005\%$ F.S.R.	24 Pin DDIP Hybrid 1.4x0.8x0.2"	50 psec	16MHz typ	0.5 μ V/μs	-55°C to +125°C	685mW	High speed and High accuracy. HTC-0300 and TP 4680 pin compatible. 74db feedthrough.

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

## SYNCHRO AND RESOLVER TO DIGITAL (S/D, R/D) CONVERTERS

• SINGLE-SPEED TRACKING					
MODEL	RESOLUTION	ACCURACY	PACKAGE	TRACKING RATE	DESCRIPTION/FEATURES
HSDC-8915 Monobrid Series	14 Bit	to $\pm 2.6'$	36 Pin DDIP 0.79x1.9x0.2"	10 rps	Low power S/D. 3 state output, tracks during output inhibit. LSI based hi rel. All common inputs. Can operate as CT.
* RDC-19200 Monobrid Series	10, 12, 14, or 16 Bit	$\pm 10'$ to $\pm 2'$ + 1 LSB	40 Pin TDIP 1.14x2.02x0.23"	3.2 to 800 rps	Provides resolver(sine and cosine) to digital conversion. Pin programmable for 10, 12, 14, or 16 bit resolution. Bandwidth and scalable Velocity Output voltage. Features BIT and LOS outputs. 2 and 11.8 VRMS inputs. Inductosyn compatible.
RDC-19210 Series	10, 12, or 14 Bits	to $\pm 5.3'$	28 Pin DDIP 1.4x0.6x0.2" 40 Pin DDIP 2.0x0.6x0.2"	to 640 rps	Low cost, monolithic programmable Resolver and LDVT to Digital converter with tach grade velocity output. Available in military and industrial models.
SDC-630	10 Bit	$\pm 21'$	2.6x3.1x2.6" Module	50 rps	Low profile, transformer isolated, industry standard pin out. 47 Hz to 1000 Hz.
SDC-632	12 Bit	$\pm 8.5'$	2.6x3.1x0.4" Module	40 rps	Low profile (0.4) industry standard. All common inputs. Transformer isolation.
SDC-634	14 Bit	to $\pm 2.6'$	2.6x3.1x0.4" Module	10 rps	Low profile (0.4) industry standard. All common inputs. Transformer isolated.
SDC-14520 Monobrid Series	16 Bit	to $\pm 1.3'$	36 Pin DDIP 1.9x0.79x0.21"	1.25 rps	Small, low power S/D. 3 state output, tracks during inhibit. All common inputs. Three accuracy options: $\pm 5.3$ , $\pm 2.6$ , or $\pm 1.3$ .
SDC-14531 Series	14 or 16 Bit	to $\pm 1.3'$	36 Pin DDIP 1.9x0.78x0.21" Hybrid	0.61 to 10 rps	Low cost, high reliability synchro or resolver to digital converter. Built-in-test (BIT). Internal Synthesized Reference, and single 5V power supply.
SDC-14532 Series	12 or 14 Bit	$\pm 8.5'$ or $\pm 5.3'$	32 Pin TDIP 1.74x1.14x0.28"	12 to 48 rps	Low cost programmable R/D converter. It has CT Mode capability, three-state latched outputs, and the inhibit does not interrupt tracking.
SDC-14560 Series	10, 12, 14, or 16 Bit	$\pm 6'$ to $\pm 1'$ + 1 LSB	36 Pin DDIP 1.9x0.78x0.21"	0.61 to 160 rps	Military grade synchro or resolver input. Synthesized reference. Programmable resolution and tach-like velocity output. Packaged in a hermetic case. Can operate as CT.
* SDC-14570	14 Bit	$\pm 5.3'$	1.0x0.8x0.2"	10 rps	Low cost S/D converters with tachometer quality velocity output.
* SDC-14600 Series	14 Bit	$\pm 5.3'$	28 Pin DDIP 1.5x0.8x0.2"	10 rps	Low cost dual independent S/D converters with tachometer quality velocity output.
* SDC-14610	14 Bit	$\pm 5.3'$	36 Pin DDIP 1.9x0.8x0.2"	10 rps	Low cost triple independent S/D converters with tachometer quality velocity output.
SDC-14700	5 decades	$\pm 0.03^0$	3.1x2.6x0.4"	180 <sup>0</sup> /sec	0.01 <sup>0</sup> synchro or resolver to BCD converter.
SDC-19204 Monobrid Series	10, 12, 14, or 16 Bit	$\pm 8'$ to $\pm 2'$ + 1 LSB	40 Pin TDIP 2.0x1.1x0.23"	2.5 to 160 rps	Low cost. Programmable resolution and BW. Velocity output eliminates tach.
• MULTI-SPEED TRACKING					
HSDC-360	16-20 Bit	Varies with speed ratio	36 Pin DDIP (x3) plus parts 1.9x0.79x0.21"	$\pm 2.5$ rps	A two speed S/D or R/D tracking converter composed of two hybrid control transformers, a hybrid data processor, plus discrete components. Connection diagram for other than 1:36 ratio supplied on request.
SDC-361	16 Bit	$\pm 1$ LSB	2.6x3.1x0.8" Module	1000 <sup>0</sup> /sec	1x, 36x 2 speed S/D. Transformer isolated, broadband 47 Hz to 3000 Hz. All common inputs.
SDC-362	16 Bit	$\pm 1$ LSB	2.6x3.1x0.8" Module	1000 <sup>0</sup> /sec	1x, 18x 2 speed S/D. Transformer isolated, broadband 47 Hz to 3000 Hz. All common inputs.

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

Synchro Products continued.

\* New product.

## SYNCHRO AND RESOLVER TO DIGITAL (S/D, R/D) CONVERTERS

(continue)

● MULTIPLEXED INPUT					
MODEL	RESOLUTION	ACCURACY	FREQUENCY	PACKAGE	DESCRIPTION/FEATURES
HMSDC-8700	14 Bit	± 4.6' ± 1/2 LSB	—	36 Pin DDIP 1.9x0.79x0.21" (x2)	Two hybrids or encapsulated modules are used for a 4-channel, multiplexed system. The two packages consist of a central converter and an input processor which accepts four signal channels and one reference channel. Multiple input processors can be accommodated with one central converter. 150 μsec conversion time per channel. Simultaneous sampling and random accessing. All common L-L voltages and frequencies.
MSDC-700	14 Bit	± 4.6' ± 1/2 LSB	—	2.6x3.1x0.4" (x2 Module)	
● REFERENCE OSCILLATORS					
OSC-15801	—	—	400Hz - 20kHz	1.0x0.8x0.2"	Synchro/Resolver/Inductosyn reference oscillator and has quadrature ref. output voltages (two outputs 90° out of phase) with programmable output freq. (400Hz - 20kHz).
REF-15001 Series	—	—	2.5kHz or 10kHz	1.52x1.78x0.35"	Synchro/Resolver/Inductosyn reference oscillator. 2.5 KHz or 10 KHz for high speed applications. Provides pin programmable AC reference for 11.8V, 4.4V, or 2.0V.

## DIGITAL TO SYNCHRO AND RESOLVER (D/S, D/R) CONVERTERS

MODEL	RESOLUTION	ACCURACY	PACKAGE	OUTPUT DRIVE	DESCRIPTION/FEATURES
DSC-10510	16 Bit	to $\pm 1'$	40 Pin TDIP 2.0x1.1x0.2"	7VA	High power D/S converter. Microprocessor compatible. BIT output and short circuit protected. AC or DC power supplies. 5VA drive available.
DRC-10520	16 Bit	to $\pm 1'$	32 Pin TDIP 1.14x1.74x0.18"	2 VA	High power D/R converter. 8 bit 2 byte double buffered transparent input latch. BIT output and short circuit output protection. AC or DC power amps. Replaces DRC-10500. Requires standard $\pm 15V$ supply.
DRC-11522	16 Bit	$\pm 1'$	36 Pin TDIP Hybrid 1.9x0.78x0.21"	2mA-rms	2 channel D/R. Each channel is independent from the other with the exception of the 16 digital lines. Pin programmable gain control.
DSC-644	14 Bit	$\pm 4'$	2.6x3.1x0.5" Module	1.5 VA	Low profile industry standard pin-out. Metal heat sink. current limited, and transient protected. Internal 400 Hz transformers. Low scale factor variation. CMOS and TTL digital input compatibility.
DSC-544	14 Bit	$\pm 4'$	2.6x3.1x0.8" Module	4.5 VA	Powered from reference, metal heat sink, all internal transformers. Short circuit proof and transient protected. Thermal cutoff. Output is transformer isolated 90V synchro at 400Hz and 60Hz.
DSC-11520	16 Bit	to $\pm 1'$	36 Pin DDIP 1.9x0.78x0.21"	2mA	16 bit programmable D/S and D/R converter. 8 bit 2 byte double buffered transparent latches. Output short circuit protection. 0.05% scale factor variation. Replaces HDSC-14.
TD-100	12 Bit	$\pm 10'$	5.4x5.3x0.7" PC Card	25 VA	Hi power torque receiver synchro driver. Options to 115 VA with external booster amp. Short circuit protected, thermal cutout, sequenced turn on, input registers.
TD-101	12 Bit	$\pm 10'$	5.4x5.3x0.7" PC Card	—	Same as above but designed for remote power stage.

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

## SYNCHRO AND RESOLVER INSTRUMENTS

MODEL	FUNCTION	RESOLUTION	ACCURACY	PACKAGE	DESCRIPTION/FEATURES
API-30602	Synchro Indicator	0.001°	to $\pm 0.03^\circ$	3.8x2x7.5" Panel Meter	Low cost, pin programmable for all common inputs, bright .43" display, tristate output, offset adjust for system zeroing, 47-1200Hz.
DBA-488	488 Bus Adapter	—	—	6.1x8.1x1.7" Assy	IEEE-488 interface adapter for instruments. Talk and listen. Interfacing information stored in a plug-in ROM.
HSR-103/203	Synchro Indicator	0.001°	$\pm 0.005^\circ$	1.7" High (103) 3.5" High (203) 1/2 Rack	Wideband 47-1000 Hz, automatic gain ranging, bit fault Monitor, synthesized reference, programmable 0-360° or $\pm 180^\circ$ , IEEE-488 option.
* IAC-37001	Synchro Simulator & Indicator	20/16 bits Programmable	18 arc sec	VXI 'C' size card 9.2x13.4x1.2"	Instrument on A Card. Combines the capabilities of both the HSR-203 and SIM-31200 on one card.
MSR-236	2 Speed Synchro indicator	0.01°	$\pm 0.01^\circ$	12x9.6x4.8" Combination Case	Converts single or dual (1:36 or 2:36) speed synchro or resolver signals to BCD angle. Transformer isolation. MIL-T-21200 case.
SR-103/203	Synchro Indicator	0.01°	$\pm 0.03^\circ$	1.7" High (103) 3.5" High (203) 1/2 Rack	0.01° version of the above.
SIM-31200	Angle Simulator	0.001°	to $\pm 0.003^\circ$	14.5x8.12x3.47" Instrument	Synchro or resolver angle simulator with high accuracy, wide band operation (47Hz to 11kHz). Front panel keyboard programmable (local mode), standard parallel I/O, or optional IEEE-488 I/O (remote mode).

## SYNCHRO AND RESOLVER CARDS

MODEL	RESOLUTION	ACCURACY	PACKAGE	DESCRIPTION/FEATURES
* IAC-37001	SEE SYNCHRO AND RESOLVER INSTRUMENTS FOR THE IAC-37001.			
SDC-36015	10,12,14, or 16 Bits	$\pm 3'$	4.5x13.5x0.44"	R/D-S/D CONVERTER CARD. Full size IBM card for 1 to 6 channel of Resolver or Synchro to Digital conversion. It uses either the RDC-19200 Series (for resolver inputs) or SDC-14560 (for synchro inputs) hybrid converters.

## SPECIAL FUNCTIONS

FUNCTION	RESOLUTION	MODEL	ACCURACY	PACKAGE	DESCRIPTION/FEATURES
CONTROL TRANSFORMER	14 Bit	HSCT-14	to $+2'$	36 Pin DDIP 0.78x1.9x0.21"	Control transformer. For new designs use HSDC-8915 or SDC-14560.
LVD/TVDT TO DIGITAL CONVERTER	12 Bit or 14 Bit	DTC-19300	0.25%, 0.05%	36 Pin DDIP 0.78x1.9x0.21"	12 or 14 Bit LVDT (Linear Variable Differential Transformer) or RVDT (Rotary VDT) to digital converter which also supplies the AC excitation; Frequency, signal gain, and resolution are all programmable. Also features velocity and Built-In-Test outputs.
* LVDT/RVDT TO DIGITAL CONVERTER	12 bit	DTC-19305	0.15%	1.0x0.8x0.2"	Low Cost. 12 Bit LVDT or RVDT to digital converter in a very small package. Based upon a monolithic ratiometric tracking converter. Resistor programmable sum and difference input range.
SYNCHRO BOOSTER AMPLIFIER	—	SBA-SERIES AMPLIFIER	$\pm 3'$	7.4x5.1x1.8" (400Hz) 7.4x5.1x2.6 (60Hz) Chassis	25 VA drive (6 $\Omega$ active load). Kick circuit prevents 180° hang-up. powered from reference. Short circuit, transient and overload protected.
U.S. NAVY STANDARD ELECTRONIC MODULES	—	SEM MODULES	—	—	Many S/D, D/S, A/D, D/A and 1553 Data Bus key codes. Consult factory.

NOTES: Most hybrid products are available with Military Processing (Contact Factory).

\* New product.

## POWER HYBRIDS

MODEL	PACKAGE	DESCRIPTION/FEATURES
● <b>H-BRIDGES</b>		
<b>PWR - 82320 SERIES</b>	1.370 x 1.800 x 0.375"	HIGH CURRENT (30A) H-BRIDGE WITH FLYBACK DIODES, contains four N-channel power mosfets connected into a full H-bridge configuration and shunted by anti-parallel fast recovery diodes, high current capability and small size. It has a very low forward voltage drop, high efficiency, low recovery charge and low junction to case thermal resistance.
<b>PWR - 82324 SERIES</b>	1.370 x 1.800 x 0.375"	HIGH CURRENT (12A) H-BRIDGE WITH FLYBACK DIODES, contains two N-channel and two P-channel power mosfets connected into a full H-bridge configuration and shunted by fast recovery diodes, high current capability and small size. It has a very low forward voltage drop, high efficiency, low recovery charge, low junction to case thermal resistance.
● <b>MOTOR DRIVERS</b>		
<b>PWR - 82331 SERIES</b>	3.0 x 2.1 x 0.395"	SMART POWER 3 PHASE MOTOR DRIVE BRIDGE WITH FLYBACK DIODES AND INTERNAL GATE DRIVE CIRCUITRY. 30A current capability at 200V and 600V Vcc. Each input is driven directly from a ground referenced signal with no bias voltage required. Thermal resistance of < 0.85°C/W.
<b>PWR - 82340 SERIES</b>	2.2 x 2.1 x 0.395"	SMART POWER MOTOR DRIVE H-BRIDGE WITH FLYBACK DIODES AND INTERNAL GATE DRIVE CIRCUITRY. 30A current capability at 200V and 600V Vcc. Each input is driven directly from a ground referenced signal with no bias voltage required. Thermal resistance of < 0.85°C/W.

## MEMORY HYBRIDS

MODEL	PACKAGE	DESCRIPTION/FEATURES
<b>MEM-84002</b>	46 Pin Square Flat Pack 1.25 x 1.25 x 0.15"	55ns 64K X 16 STATIC RAM organized as four 32K x 8 blocks with TTL compatible inputs and outputs. It has low power requirements, battery back-up with 2V data retention, fast access time, full CMOS construction, an external decoding option, operates from -55°C to +125°C.

## DC - DC CONVERTERS

MODEL	PACKAGE	DESCRIPTION/FEATURES
<b>PWR-82400 SERIES</b>	3.2 x 2.45 x 0.595" 10 pin plug in with mounting flange	± 15V & +5V, ± 12V & +5V 34W & 50W DC - DC converters. Features include high power density and 80% min operating efficiency. Operation over a wide operating temperature range and hermetically sealed.
● <b>LOW PROFILE</b>		
<b>PWR-82415</b>	1.82 x 3.085 x 0.4"	Same as above except that it is a +5V, 25W DC-DC Converter
<b>PWR-82416</b>	1.82 x 3.085 x 0.55"	Same as above except that it is a +5V, 75W DC-DC Converter
<b>PWR-82425</b>	1.82 x 3.085 x 0.4"	Same as above except that it is a ± 15V, 25W DC-DC Converter

NOTES: Most hybrid products are available with Military Processing (Contact Factory).



## SYSTEMS

MODEL	PACKAGE	DESCRIPTION/FEATURES
6514	Cabinet 78 x 22 x 24"	SOLID STATE SYNCHRO RETRANSMISSION SYSTEM (SRS) that provides power boosts as well as speed ratio, ratio transformation of ships navigation, and altitude synchro information. It has digital implementation and modular partitioning, BITE, fully protected outputs, high reliability and is expandable.
6480	Cabinet 67 x 21.6 x 21.6"	SOLID STATE SYNCHRO RETRANSMISSION SYSTEM (SRS) that provides power boosts as well as speed ratio, ratio transformation of ships navigation, and altitude synchro information. It has digital implementation and modular partitioning, BITE, fully protected outputs, high reliability and is expandable.
6322	Cabinet	SOLID STATE SYNCHRO RETRANSMISSION SYSTEM (SRS) that provides power boosts as well as speed ratio, ratio transformation of ships navigation, and altitude synchro information. It has digital implementation and modular partitioning, BITE, fully protected outputs, high reliability and is expandable.
6438 BR	Open frame chassis 20.25 x 23.21 x 13"	Seven channel, Hi - power, digital/synchro drive system
DDC-6498/5521	9.96 x 3.96 x 9.875" 2.81 x 3.90 x 7.59"(DDC-5521)	39 channel switchboard synchro panel meter
S-SERIES	Euro-Card	Building - block PC cards for SRS, IRS, and Custom system requirements

## SOLID-STATE POWER CONTROLLERS

MODEL	PACKAGE	DESCRIPTION/FEATURES
LMC-47002	3/4 ATR enclosure	The LMC-41002 is an electrical load management center that provides MIL-STD-704 power to aircraft electrical systems. Resident in the unit are two DDC BUS-67007s which provide the intelligence for load management functions such as fault detection, current overload protection, automatic resetting, and load shedding.
SSP21110 Series	—	The SSP21110 Series of 28 Vdc Solid- State Power Controllers are Remote Solid-State Relays with controlled trip characteristics and status outputs. Utilizing Power MOSFET switches, these Power Controllers offer low 'on' resistance, low voltage drop, high off impedance, and low power dissipation.

NOTES: Most hybrid products are available with Military Processing (Contact Factory).



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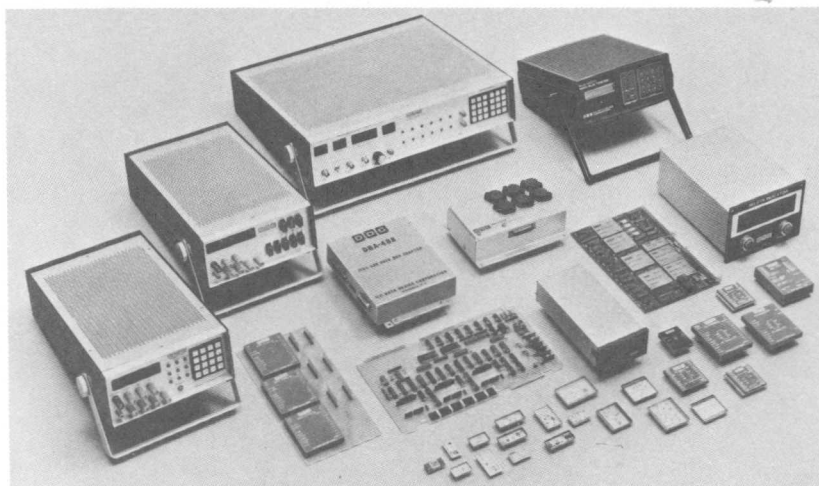
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**History and background.** ILC Data Device Corporation was incorporated in 1964 as a supplier of high performance operational amplifiers. From its inception, emphasis has been placed on state of the art, high quality data and signal conversion components and systems. In 1971 DDC was acquired by ILC Industries, sole supplier of the Apollo, Skylab and Shuttle space suits. Since its acquisition by ILC Industries, DDC has accelerated its progress in the data conversion field and is today the leading supplier of synchro conversion equipment and a major supplier of high performance A/D and D/A conversion equipment. DDC's present capability encompasses diversity in the design and production of high quality discrete and hybrid data conversion components and systems.

DDC boasts a complete design engineering function integrated with a sophisticated manufacturing operation whose capability ranges from production quantities of standard components to custom circuitry requiring comprehensive engineering production and quality.

**Facilities.** DDC has its headquarters in Bohemia, Long Island, New York where it occupies 166,000 square feet in three buildings at the Airport International Plaza. These modern, air-conditioned premises contain an up-to-date, thick-film and thin-film hybrid manufacturing operation with its own environmental control system, qualifying it to meet high performance standards. DDC's facility is certified as a QPL supplier of SEM modules to MIL-M-28787, and meets other high quality and reliability standards, such as MIL-Q-9858A and MIL-STD-883C. DDC has also supplied equipment with the reliability levels required for manned space flight.

DDC is conveniently located next to Long Island MacArthur Airport which offers non-stop service to Boston, Washington, Pittsburgh and several other major east coast cities, and convenient transportation to New York City airports.

**Engineering.** DDC has assembled in its organization a staff of highly specialized engineers. Its capabilities

range from state-of-the-art analog and digital circuit design to design of monolithic components, computer interfaces and instrumentation. The staff is also responsible for data conversion system design, transformer design, and thick and thin-film hybrid design and packaging.

The Engineering Department performs initial design, breadboard fabrication and testing, prototype assembly and evaluation. Annually it also produces several million dollars worth of system and subsystem design, fabrication and testing.

**Product Assurance.** At DDC, the Product Assurance function is headed by a Vice President. He has sole responsibility for Product Assurance and reports directly to the President. This ensures independent actions thereby maintaining integrity of the Product Assurance (Quality, Reliability, and Maintainability) function.

The Quality Assurance program at DDC is fully compliant with MIL-Q-9858A and MIL-STD-45662. DDC's Workmanship Standards Manual complies with MIL-E-5400, MIL-E-16400, MIL-STD-883C, MIL-STD-454, MIL-STD-275 and MIL-STD-1772 as well as the particular requirements of current DDC customers.

**Manufacturing.** DDC's manufacturing capabilities are subdivided into the discrete and hybrid disciplines in which the company specializes. Each area is managed by a different team of specialists, under the direction of a single Vice-President of Manufacturing.

**Sales and Marketing.** Our Sales Department is composed almost exclusively of graduate electronic engineers. This is because the products that DDC sells are often modified to meet a specific customer's requirements. Only with marketing and sales personnel technically qualified in our product line can we accurately assess our customer's needs and translate those needs into documentation our engineering, manufacturing and quality assurance organizations can use.